SEM-Grid Prototype Electronics using Charge-Frequency-Converters

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Abstract

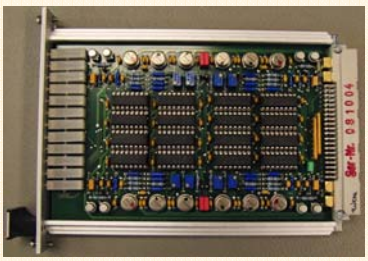
A prototype system using an ASIC equipped with 8 Charge-to-Frequency Converters (CFC) was developed in collaboration between the Beam Diagnostics and Experiment Electronics Department at GSI. The maximum sensitivity is 250fC per output pulse. It will serve as an economic alternative for the readout electronics of Secondary Electron Monitor (SEM) profile grids or comparable beam diagnostic devices like Multi-Wire Proportional Chambers (MWPC). The goal of this contribution is to report on a detailed performance test under real beam conditions at the GSI beam lines. A 32-channel electronics is connected to different beam profile SEM-grids at a LINAC beam line and tested with various beam conditions. Transversal beam profiles with a time resolution down to the microsecond range have been recorded successfully. Beam profiles recorded with the new CFC-board and the old standard trans-impedance amplifiers agreed well. Further measurements were done with a Multi-Wire Proportional Chamber. Therefore the prototype was extended to 64-input channels recently.

Present Beam Profile Electronics

- **Assembled with outdated electronics components (>20 years)**
  - Discontinuation of components expected (crucial OPA 111 has been 2 years ago)
  - Also not clear with purchasing of electro-mechanical components (price trends ?)
- **High purchase costs**
  - At present: ~30 k€ for one profile-grid analog instrument with 64 wires/inputs

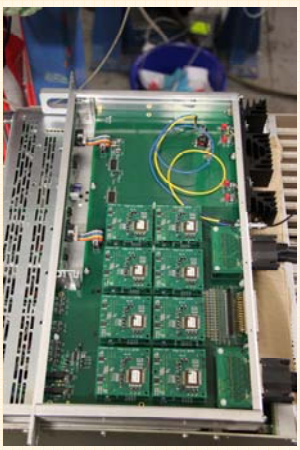
  ⇨ 1.5 k€ per 4-channel analog input card
  - Every input channel contains 3 items of OPA111, 25 € each

  ⇨ **75 € per channel**
- **Prolonged delivery times**

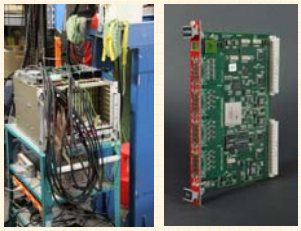


Current front-end amplifier board

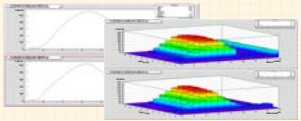
Hard- and Software



Prototype board with 8 CFC-ASICs



Hardware setup (VME-crate, left) and standard FPGA-I/O VME board (VUPROM, right)



Measurement analysis with GO4*

* **G**SI **O**bjected **O**riented **O**n-line **O**ff-line system

Main objective

- **Tests of CFC-ASICs under real beam condition**

  ⇨ Fast setup for tests possible ?

  ⇨ Use of existing parts possible ?

  ⇨ Different FPGA-I/O VME boards, modules and software tools for data acquisition does exist at GSI and were developed by Experiment Electronics department. This saved development time.

⇨ **Components of prototype**

Hardware

• RIO 2	(CPU and network connection)
• VUPROM	(FPGA, CFC-control unit)
• TRIVA	(Trigger module for MBS)
• LEVCON	(Signal level converter box)
• VME-crate	
• Motherboard	(CFC, external power supply)
• PC	

Software

• Go4*	(Program for online analysis)
• MBS	(DAQ - **M**ulti **B**ranch **S**ystem)
• C-program	(on RIO 2; setting CFC registers)
• Terminal prg.	(send CFC parameters)

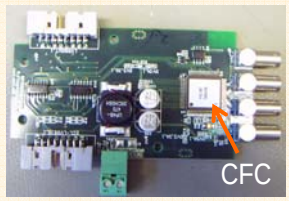
Description of function

- The CFC-motherboard is controlled by the VUPROM
- RIO 2 send the CFC-parameters to VUPROM-board and transfer the measured data to a PC
- Beam profiles are displayed via software Go4*
- CFC parameters are set via a terminal program
- TRIVA and LEVCON modules are necessary for the MBS trigger operation

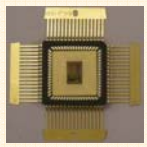
Technical parameter

- 2D and 3D plot possible with Go4*
- Ranges 10/100/1000/10000µA
- Up to 100 time slices possible
- Time slices selectable between 100ns and 86s in 20ns steps
- 120 dB dynamic at 10 or 100µA range level
- Resolution 450fC (±3σ)
- Control unit can operate with one or two CFC motherboard (32- or 64-input channels)

Charge to Frequency Converter (CFC)



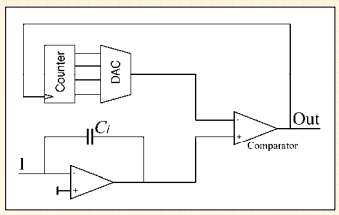
CFC-test board with I/O-drivers

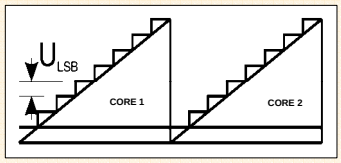


CFC-ASIC, core and device

- ASIC provides 2 ranges (0.25/2.5 pC/pulse)
- Large dynamic range (100) 300 fA …130 (180) µA
- Power supply 5V and 3.3V (ASIC)
- 4 analog inputs/ASIC (test module has 4 LEMO coaxial input jacks)
- 4 on-chip counters, 16bit
- Output frequency typical 40 MHz (10 or 100 µA)
- QFW has serial and parallel interface (test boards only serial port in operation)
- Test modules with additional drivers (LVDS and ECL compatible) available
- Offset correction via parallel interface possible
- Price: <50 €/ASIC

Working Principle of CFC





Block diagram of CFC-core

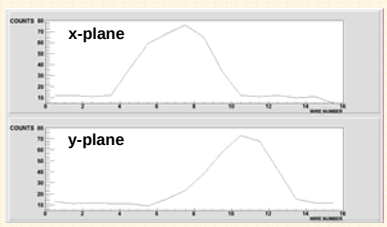
(with 4-bit DAC)

- 2 CFC-cores per channel
- Input current is integrated in active core #1
- Comparator increments DAC reference and compare integrator voltage with DAC value
- If comparator trips the counter is increase by one step (or LSB value)
- On overflow the integrator of core #1 is reset while core #2 gets activated
- The measured charge per step is defined by $dQ = U_{LSB} * C_i$
- The output frequency is linearly dependent of the input current: $f = I / dQ$

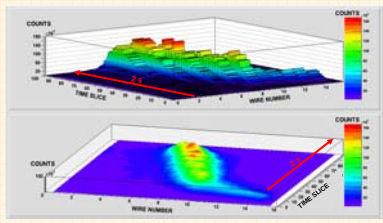
Results of Beam Profile Measurements

- Successful beam profile measurements at SEM-grid and MWPC
- Comparison between old and new electronics has shown a very good agreement (2D-plots)
- Good observation of time-dependant changes of beam pulses (3D-plots)

  ➔ Very helpful for accelerator operations. Not supported by the existing old electronic.



Original SEM-grid image of a $^{124}Xe^{21+}$ ion beam @ 4.773 MeV/u. The beam current is around 6µA and has a pulse length of 100µs. The horizontal beam profile (x-plane, 16-wire grid) as well as the vertical beam profile (y-plane, also equipped with 16 wires) are shown. This kind of images can prepare also the existing old hard- and software. An example with the new readout electronics is presented beneath.



Original MWPC images of an $^{40}Ar^{18+}$ ion beam @ 300MeV/u. Both figures show the vertical and time-dependent beam profiles from the first half of the MWPC x-plane (wire 1 to 16). The beam pulse length is around 1.8 s and each time slice length is 20ms. The ion beam was mis-matched knowingly to present the new feature of the prototype. Both diagrams present the same beam profile, but in a different graphical representation.

Outlook

After further promising beam tests with the new CFC readout electronics it is planned to develop a second prototype motherboard with 64-input channels. This new board will also host the counting FPGA and network communication electronics. At this step the VME-crate setup is no more necessary. The new compact development will be a cheap solution for future beam lines at GSI and FAIR. There are further plans to use this readout electronic in other setups, e.g. Faraday-cups, ionisation chambers and other beam diagnostic devices.

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