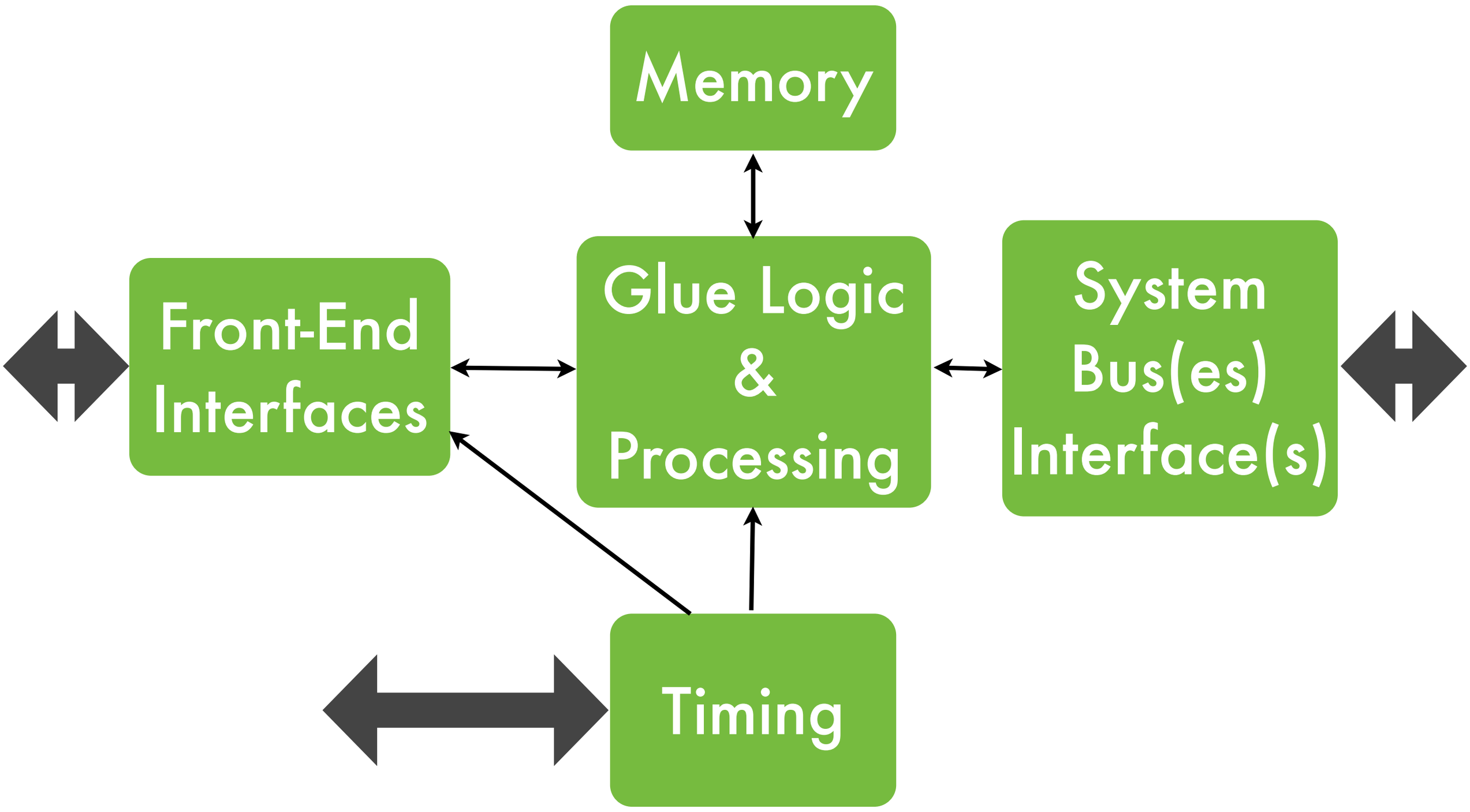
Options for Next Generation Digital Acquisition Systems

DIPAC 2011 - Andrea Boccardi

The generic architecture of a DAQ



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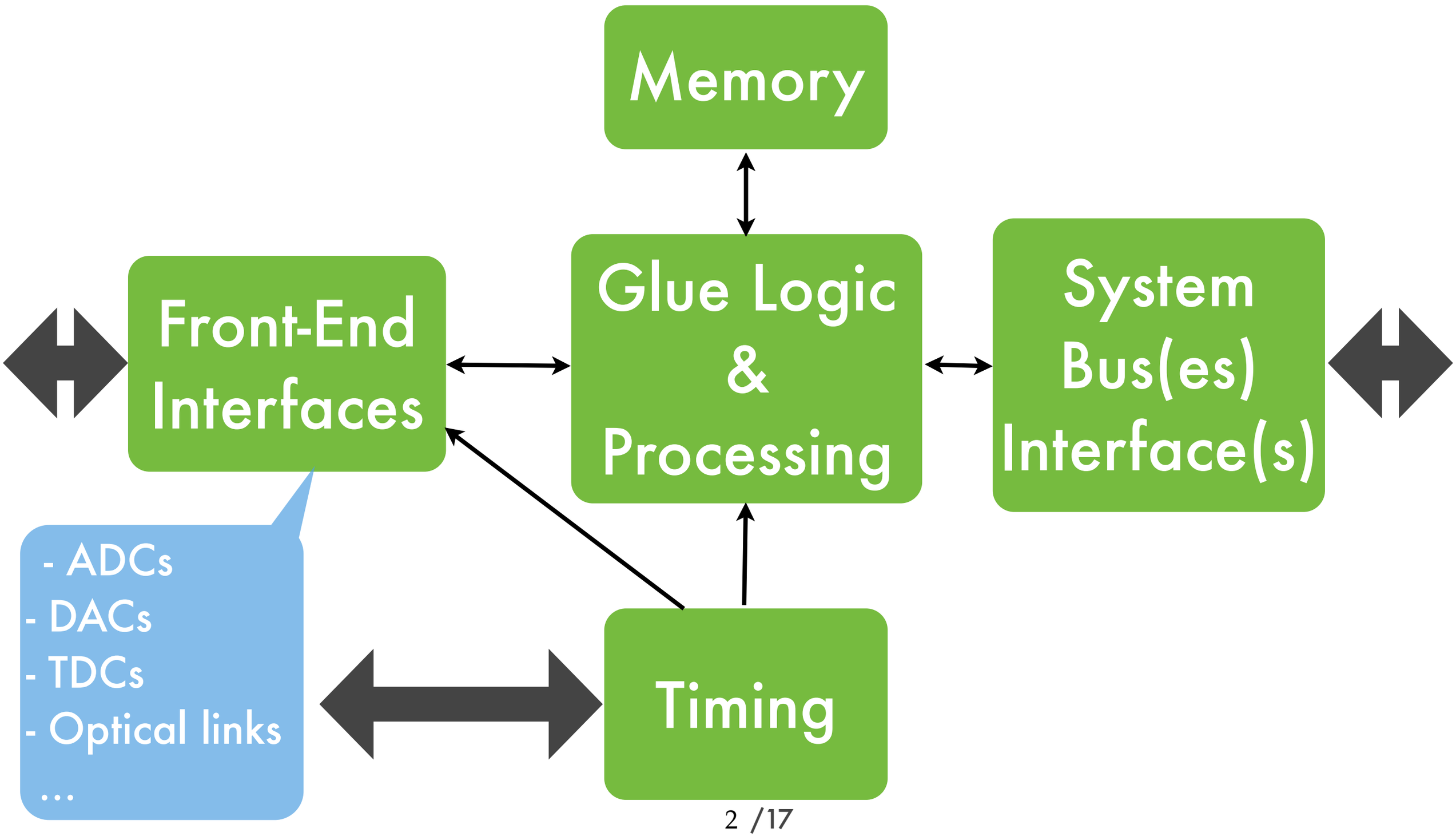

The generic architecture of a DAQ

- FPGAs
- DSPs + FPGA/CPLDs

Memory

Front-End Interfaces

Glue Logic & Processing

System Bus(es) Interface(s)

- ADCs
- DACs
- TDCs
- Optical links
- ...

Timing

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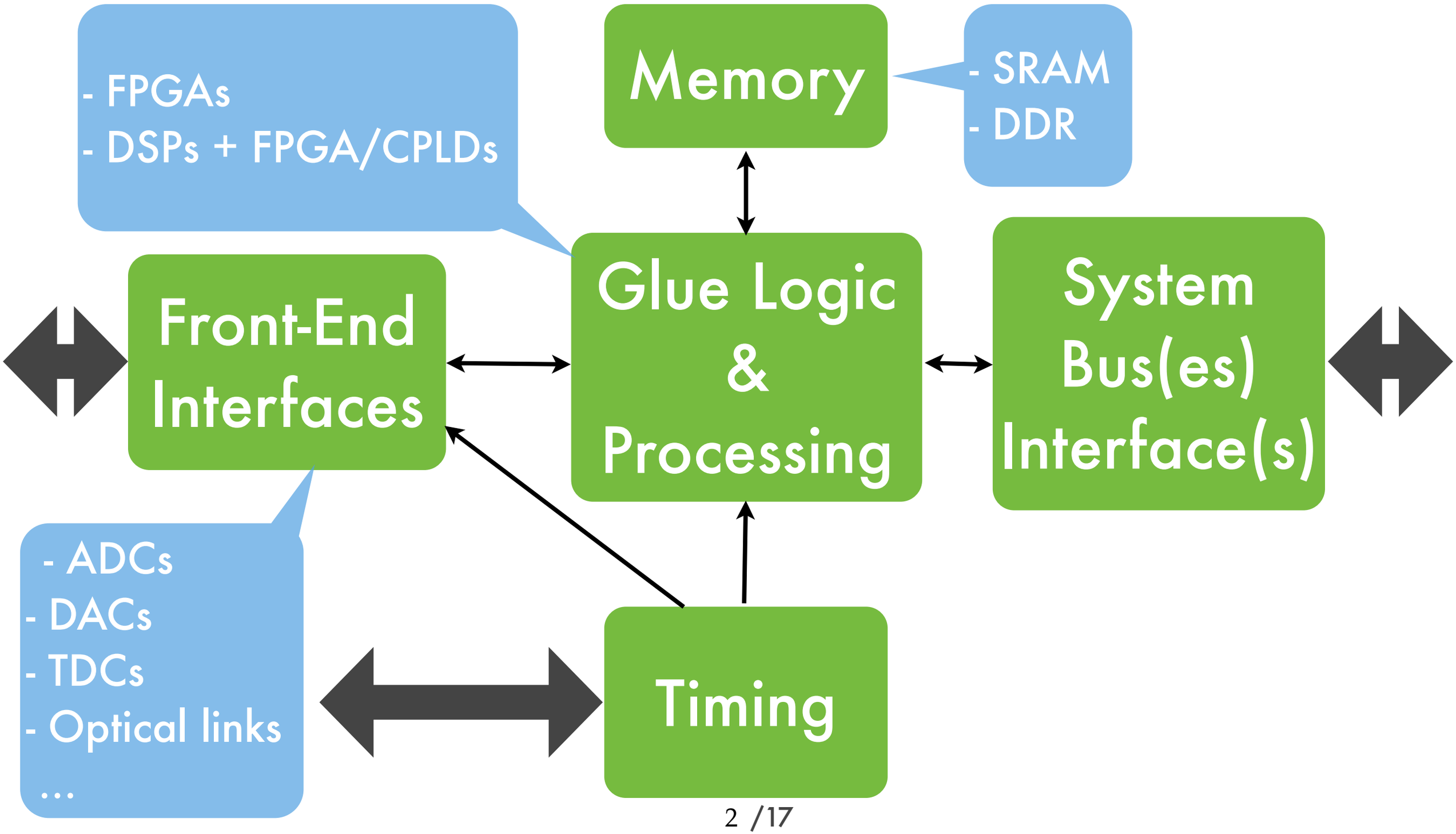

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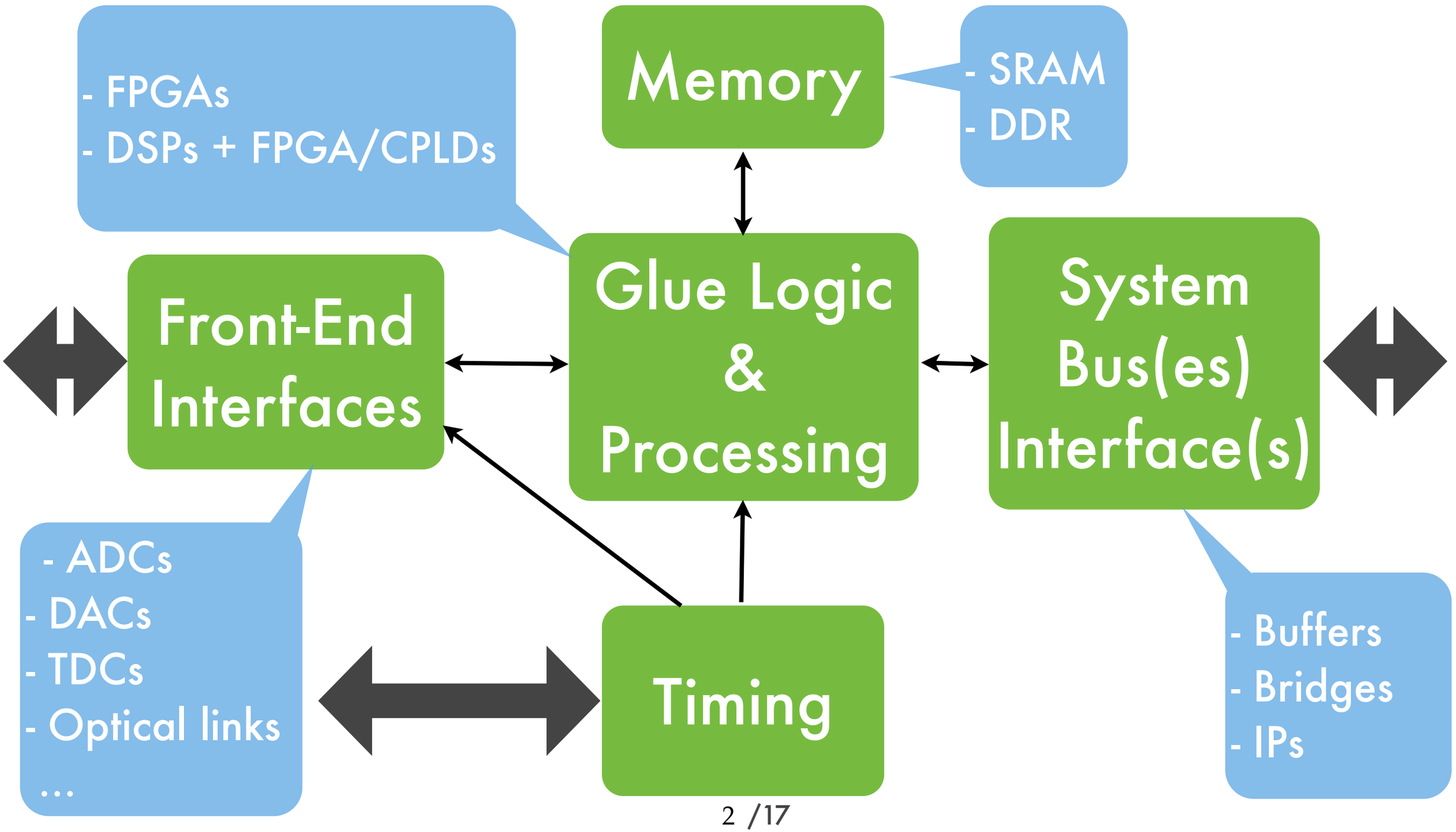

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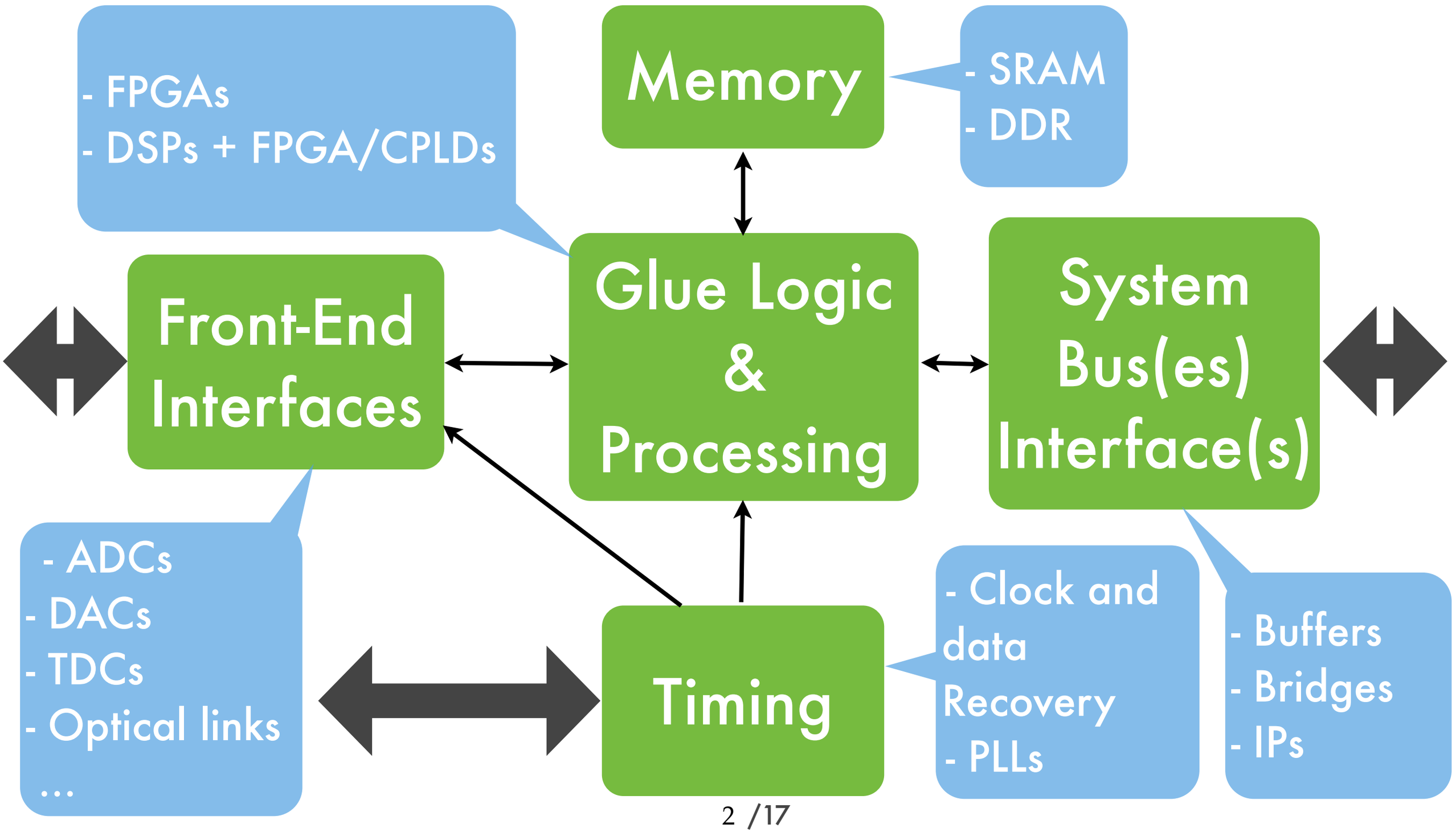
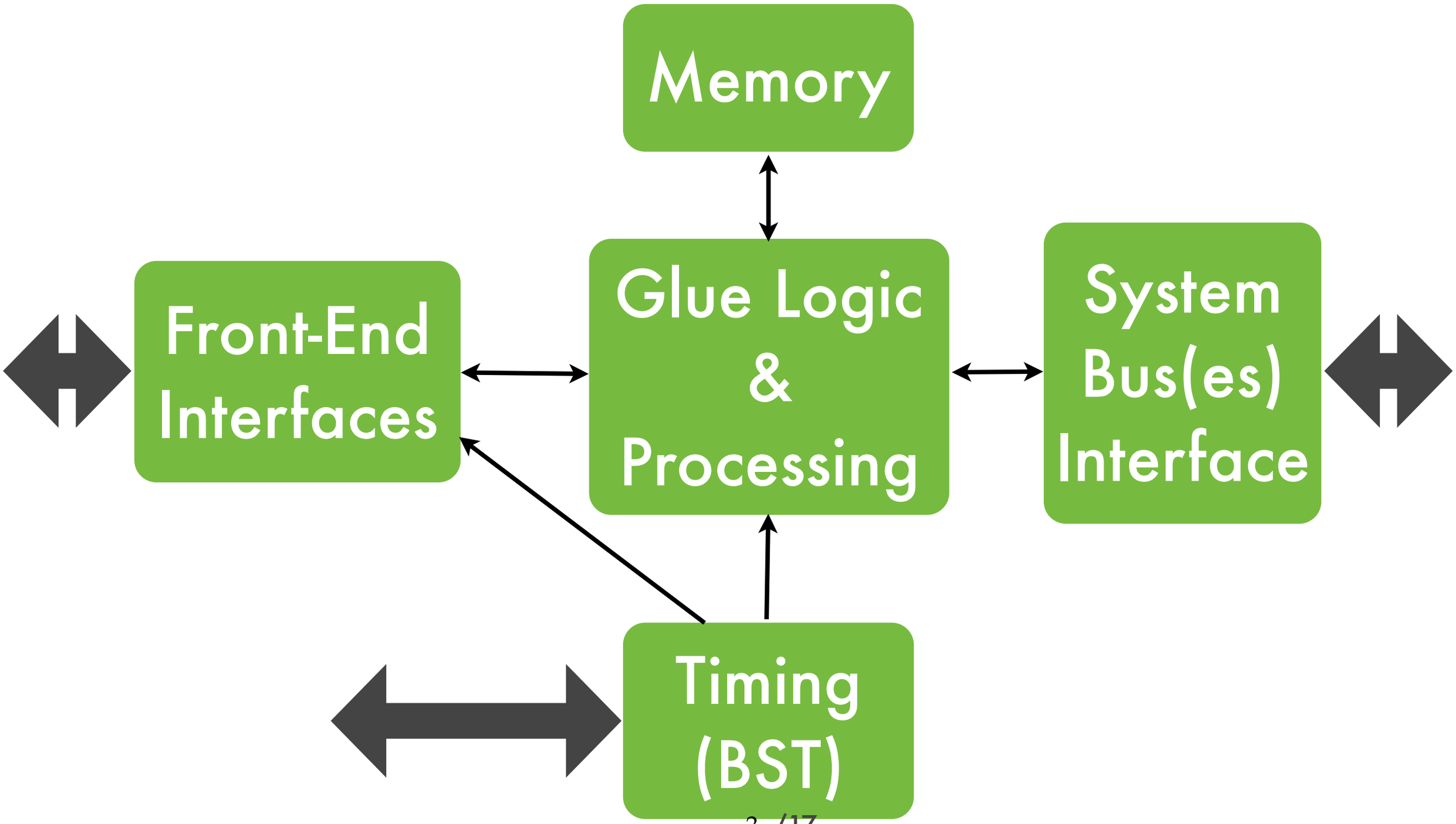


The Concept of Carrier/Mezzanine



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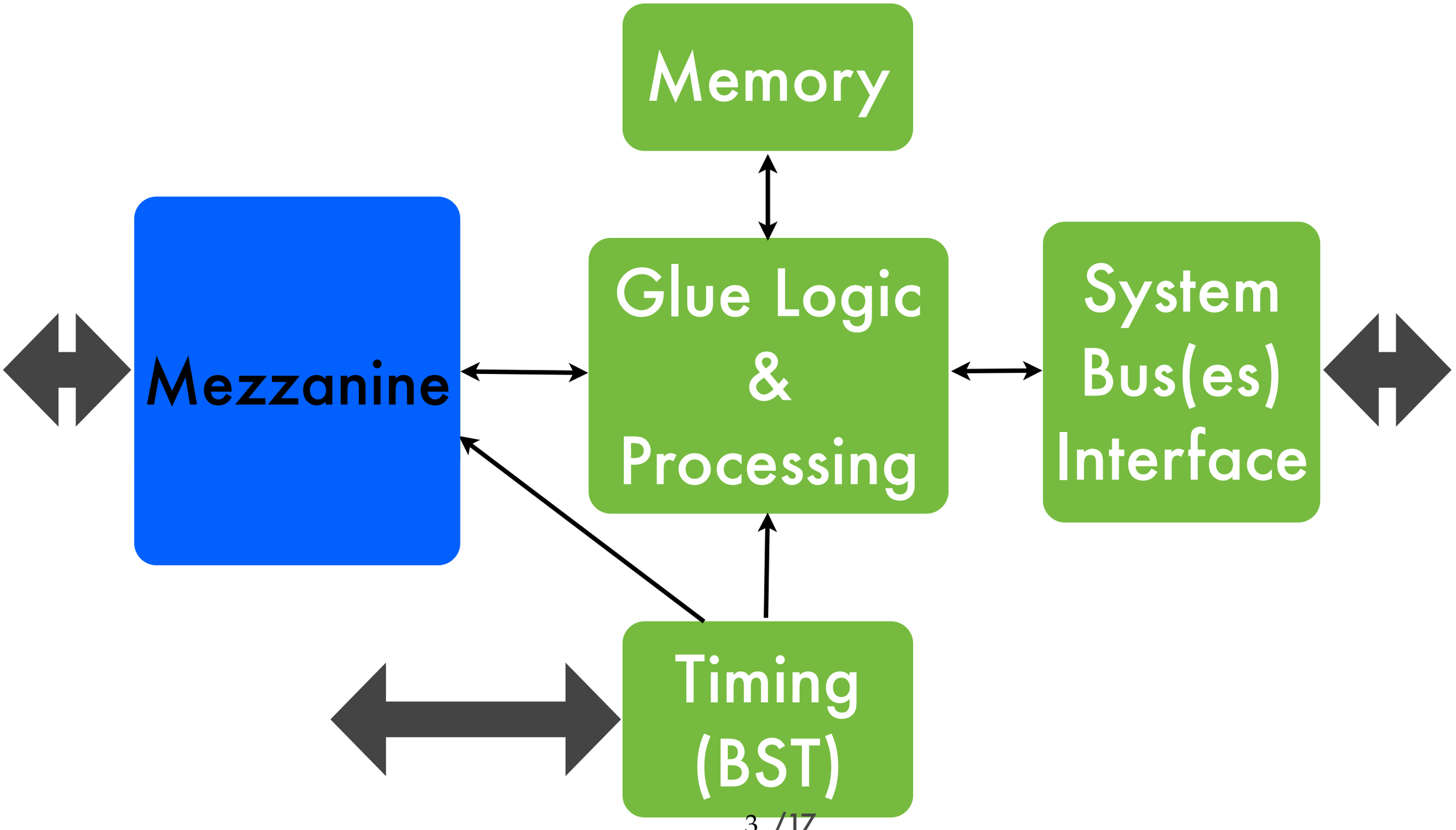

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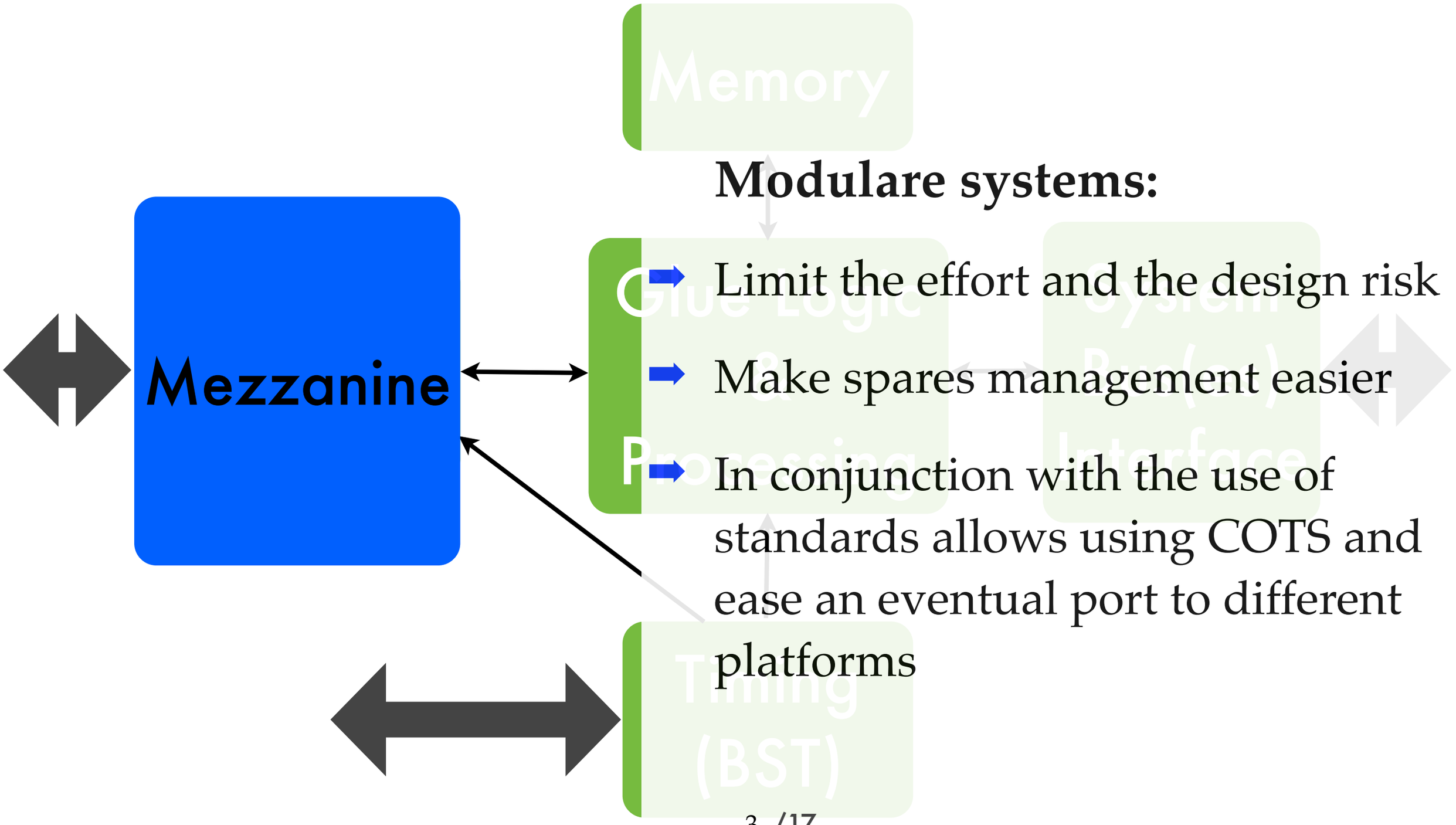
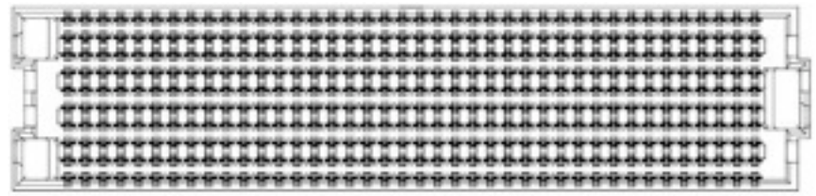


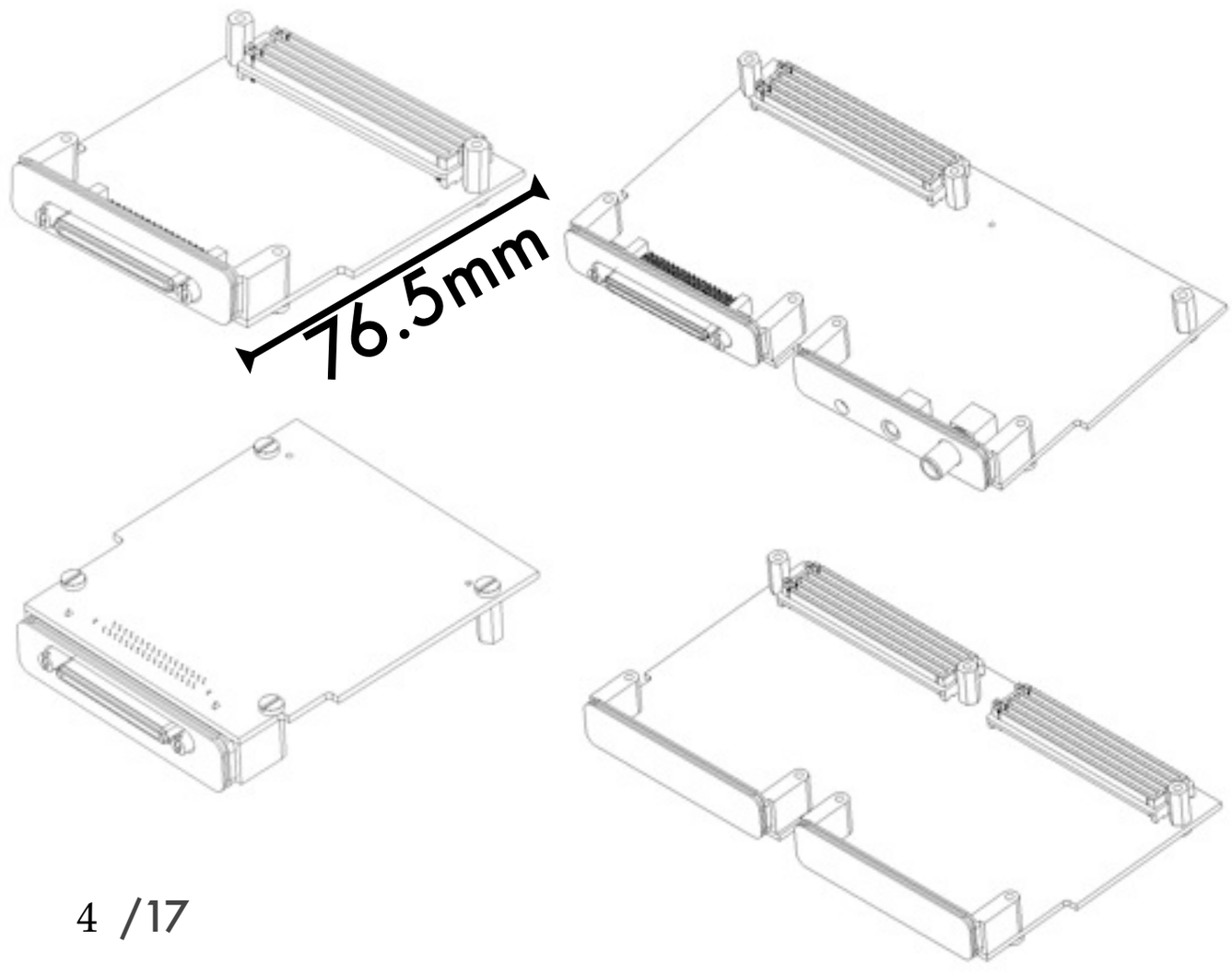
Modulare systems:

- Limit the effort and the design risk
- Make spares management easier
- In conjunction with the use of standards allows using COTS and ease an eventual port to different platforms

FPGA Mezzanine Card

- FMC is VITA 57
- 2 widths: single (69mm) and double (139mm)
- BGA style connector
- 2 connector densities: Low Pin Count (160 pins) and High Pin Count (400)





FMC standard

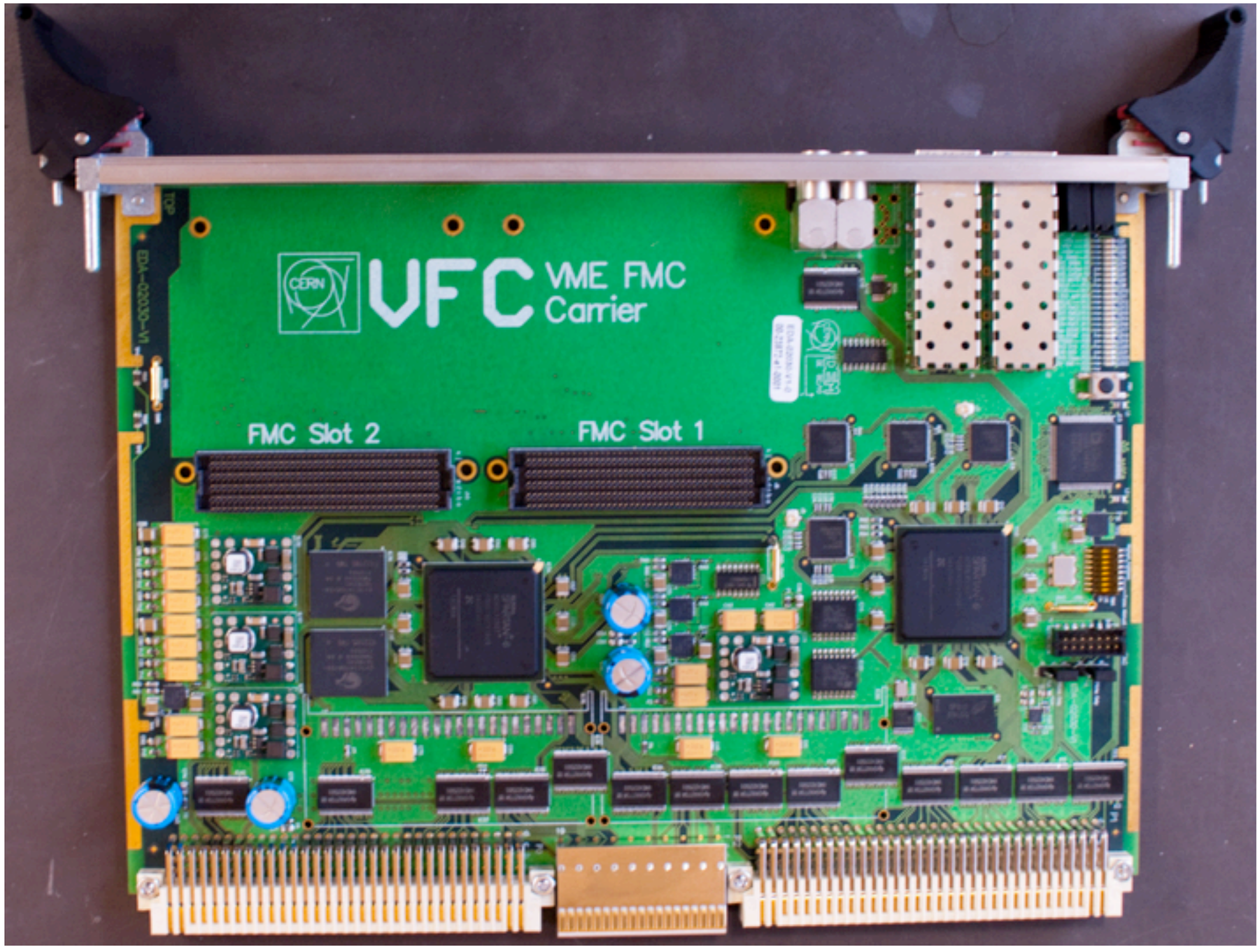
Pros:

- Very Flexible: pin function, direction and electrical standard are defined at FPGA configuration time
- Mezzanines can self identify via I2C can be performed before configuring the FPGA

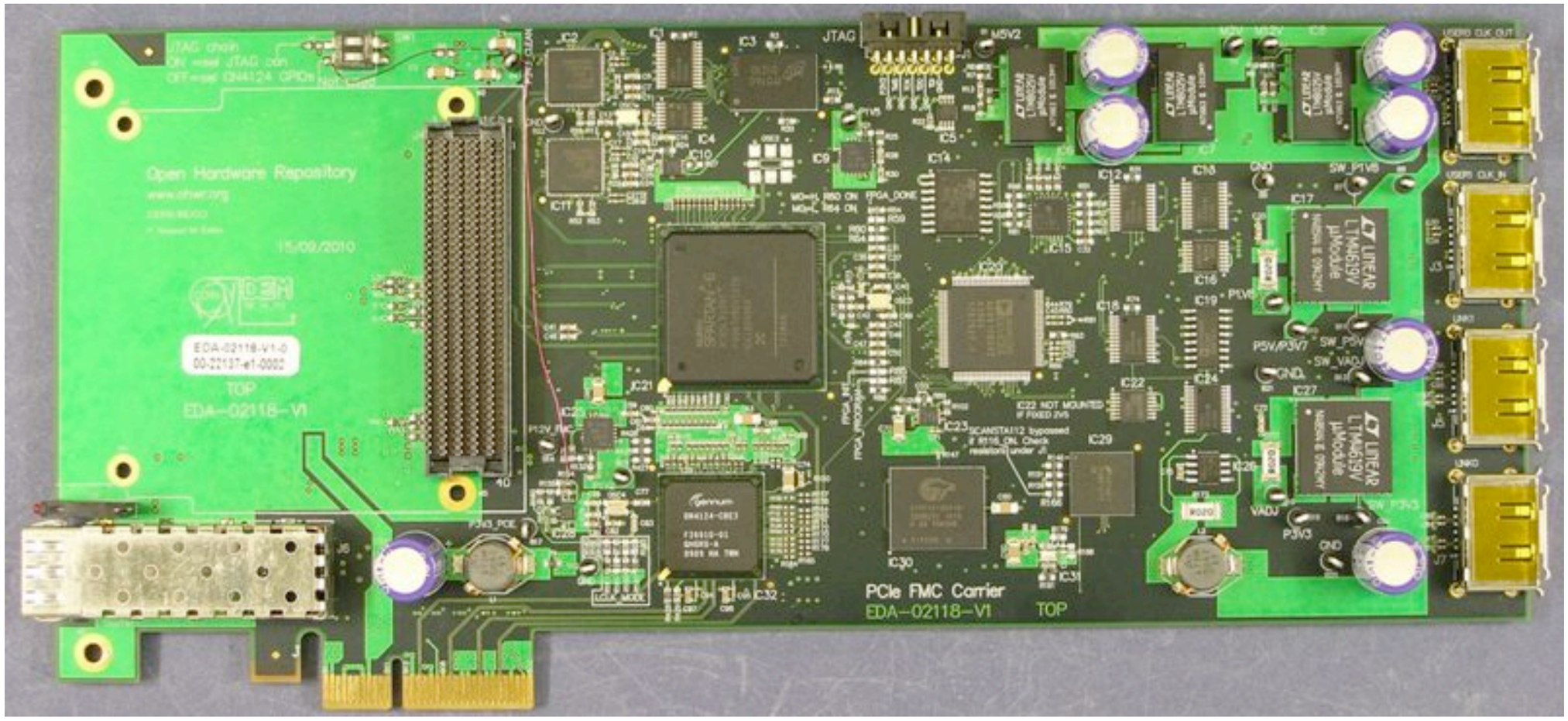
Cons:

- Real Estate
- Little attention paid to Carrier-To-Mezzanine clock distribution

VME FMC Carrier



PCIe FMC Carrier



- Designed in parallel to the VFC
- Effort in using the same components on the 2 carriers
- Almost seamless porting of the application code from one carrier to the other with the help of code wrappers

VME and PCIe comparison

VME64

- 80MB/s (320 with 2eSST)
- Up to 3 FMC (in 6U format) accessible on the front panel
- Possibility to have RTM
- Up to ~108W per board

PCIe

- Not a bus but a point to point link
- 250MB/s (PCIe 1.0) per lane (one LVDS pair per direction) and up to 32 lanes
- 1 FMC accessible on the front panel
- 10, 25 or 75W per board

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They both lack board to board fast links

VME switched serial (VXS)

- VXS is VITA-41
- It re-defines the P0 (middle connector) to have 16 differential pairs (10GHz) and 31 reserved pins
- The protocol of the differential pairs is defined by sub-standards (PCIe, Ethernet are just 2 examples)
- System management based on IPMI (I2C) but only as a recommendation
- Backplane can have star, double-star (both requiring a switch) or mesh topology
- Backward compatible with old VME64 (2esst) boards*
- Not many ongoing projects

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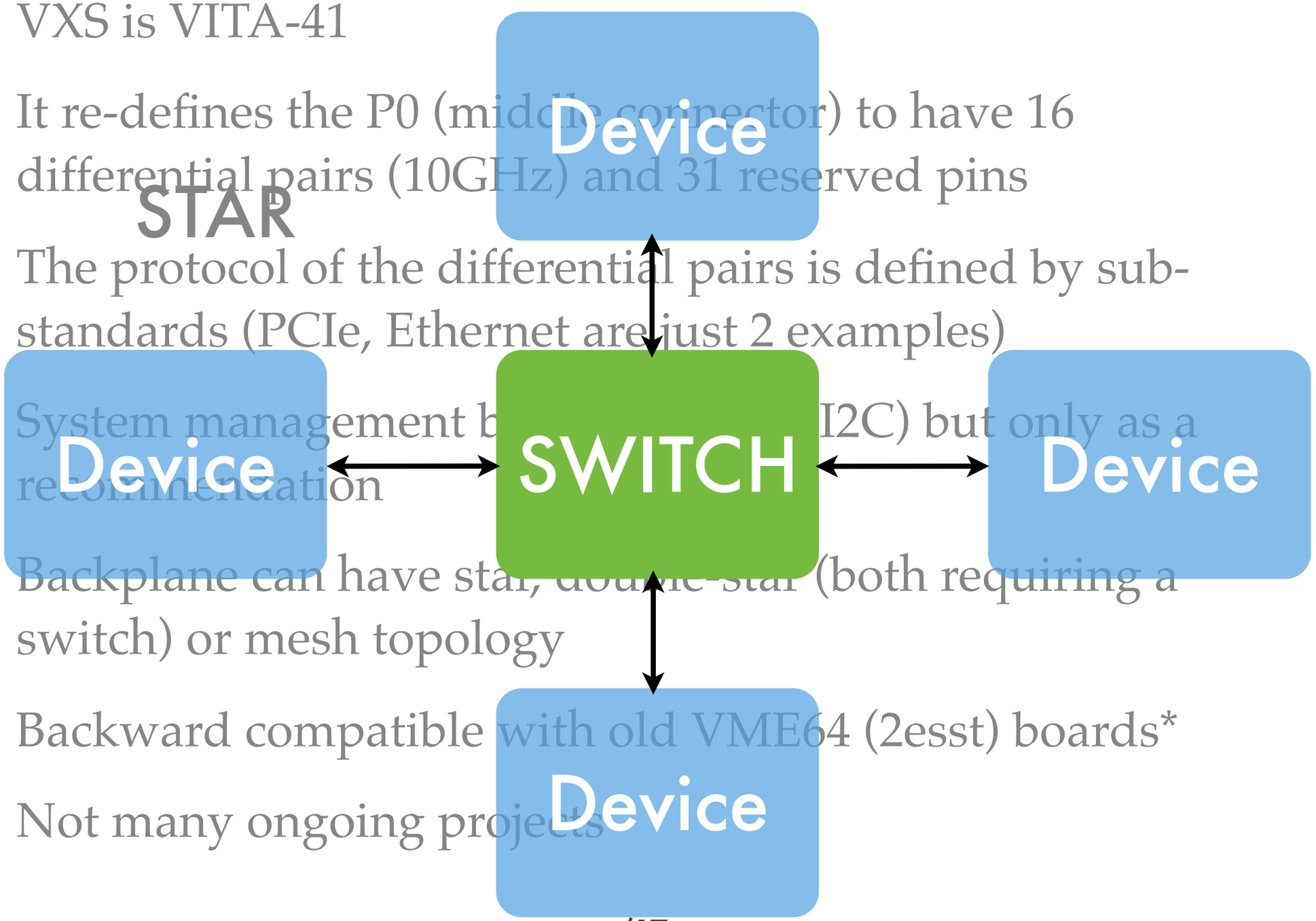

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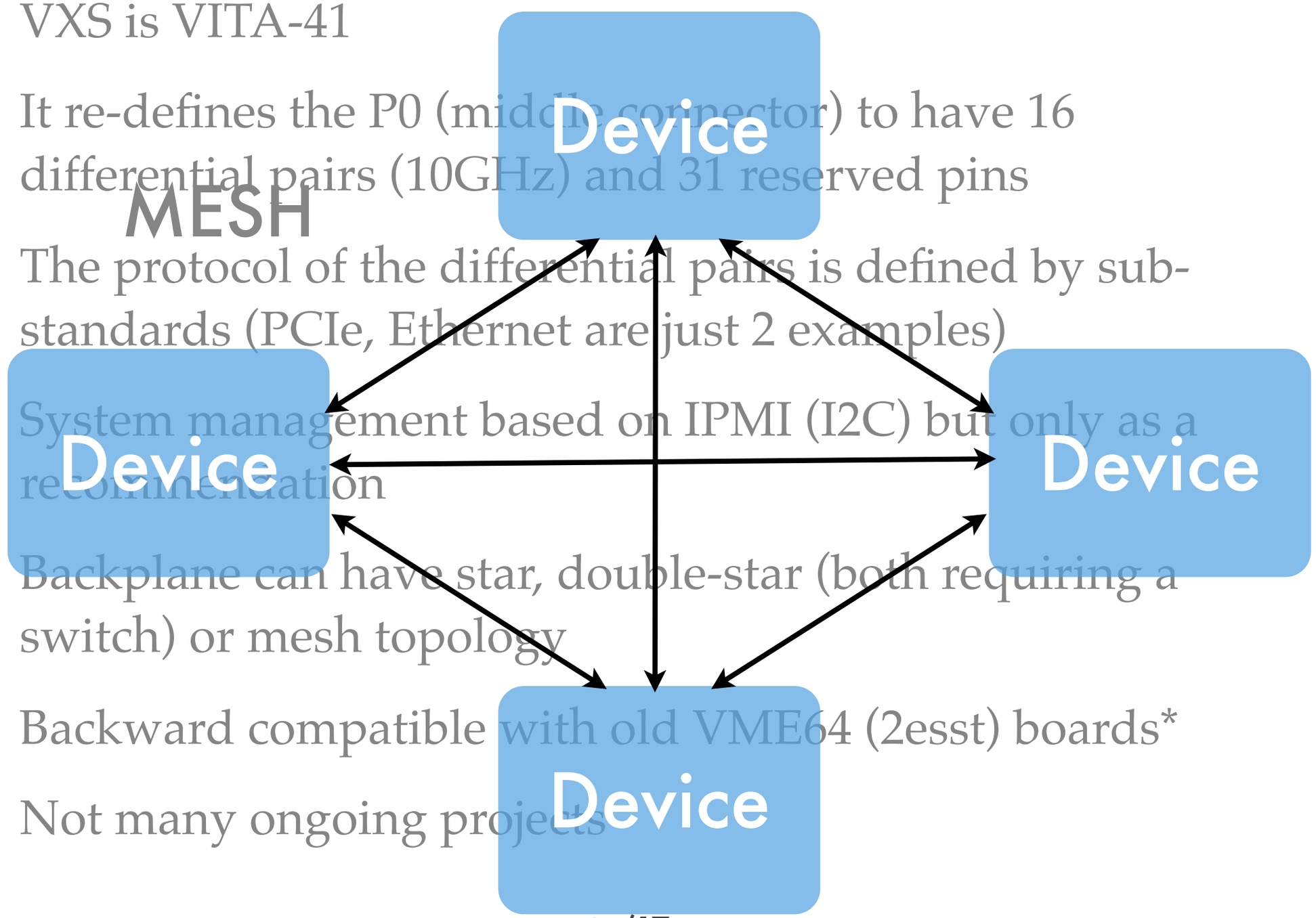

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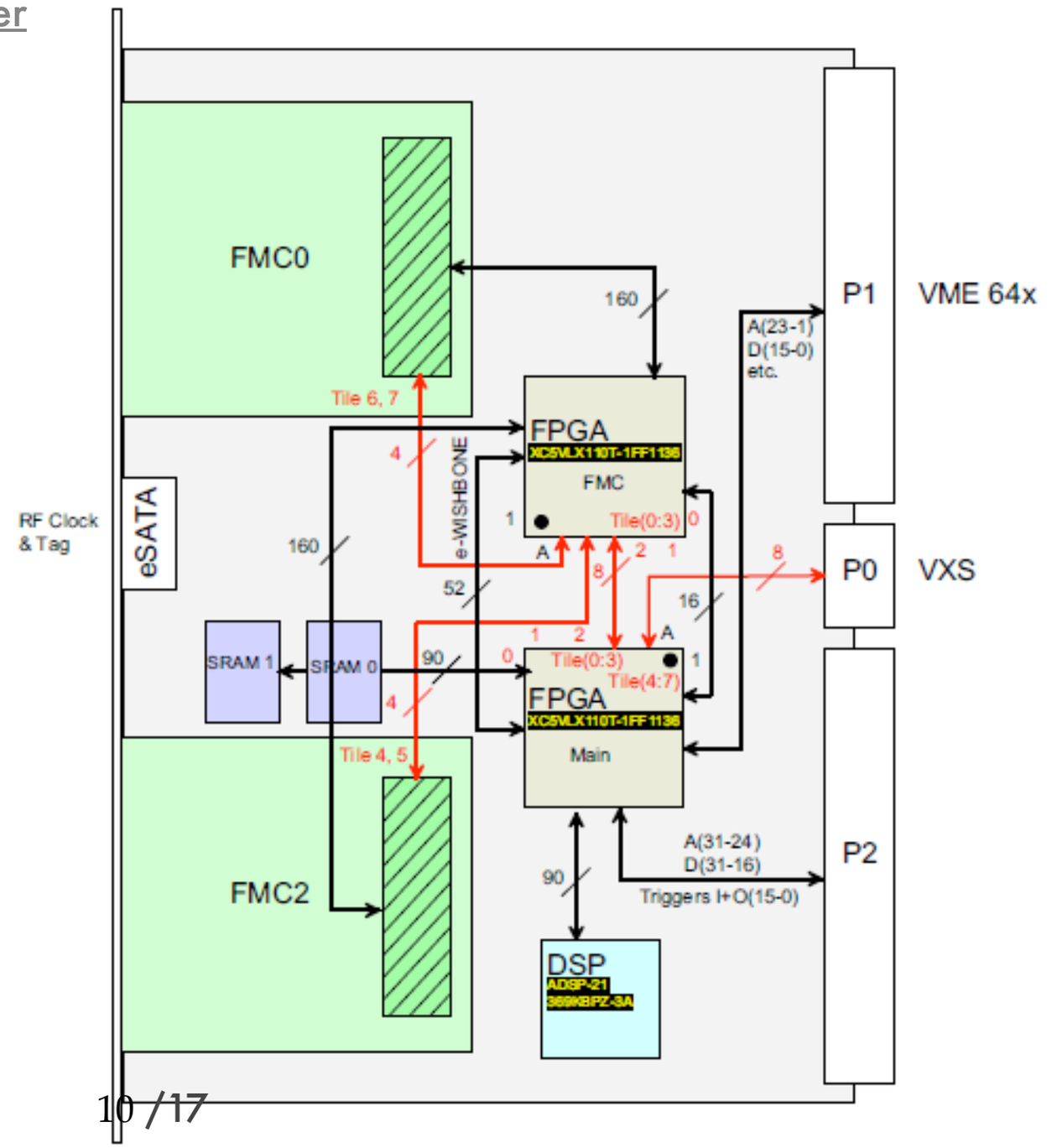
VXS DSP FMC Carrier

http://www.ohwr.org/projects/vxs-dsp-fmc-carrier

- Currently being developed by the RF group of CERN
- 8 full duplex Gbit links on the VXS connector
- 2 HPC FMC mezzanines
- Foreseen to be used with a RTM



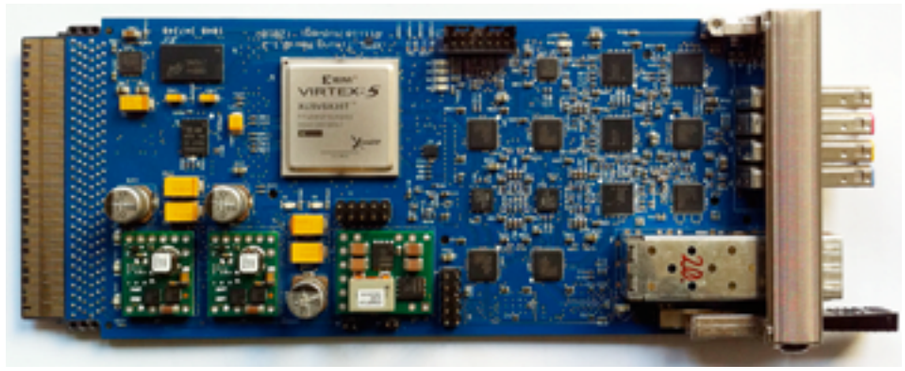
From ATCA to uTCA

- ATCA stands for Advanced Telecommunications Computing Architecture
- ATCA is PICMG 3.X
- Boards are in 8U format
- Possibility to have RTM in 8U format with user defined connections
- Supply voltage -48V (DC-DC conversions on board) with a max of 200W per card
- Has 3 connectors' zones: Power & System management, Data Transfer (up to 5 connectors), User defined connector for rear I/O
- Up to 200 differential pairs, among which 6 dedicated to clock synchronization
- System management based on IPMI

ATCA board

From ATCA to uTCA

- The Advanced Mezzanine Card (AMC) was originally a hot-swappable mezzanine for ATCA carriers
- It exists in 6 form factors (all 180mm deep):
  - 74 or 149 mm wide
  - 13, 18 or 28 mm deep

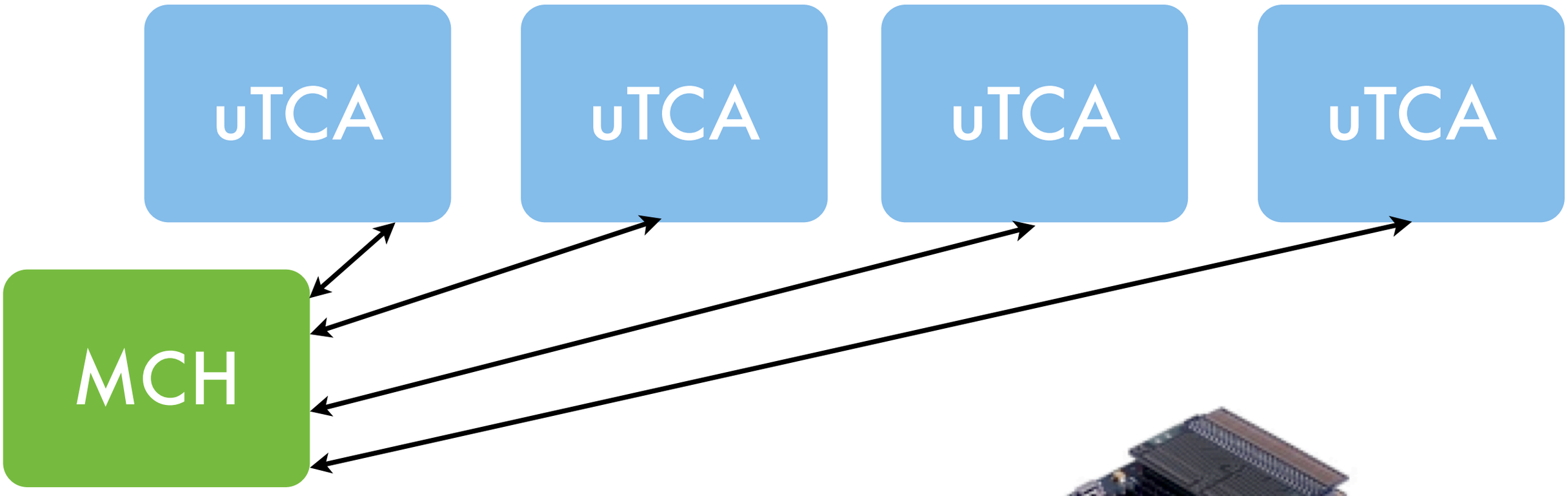


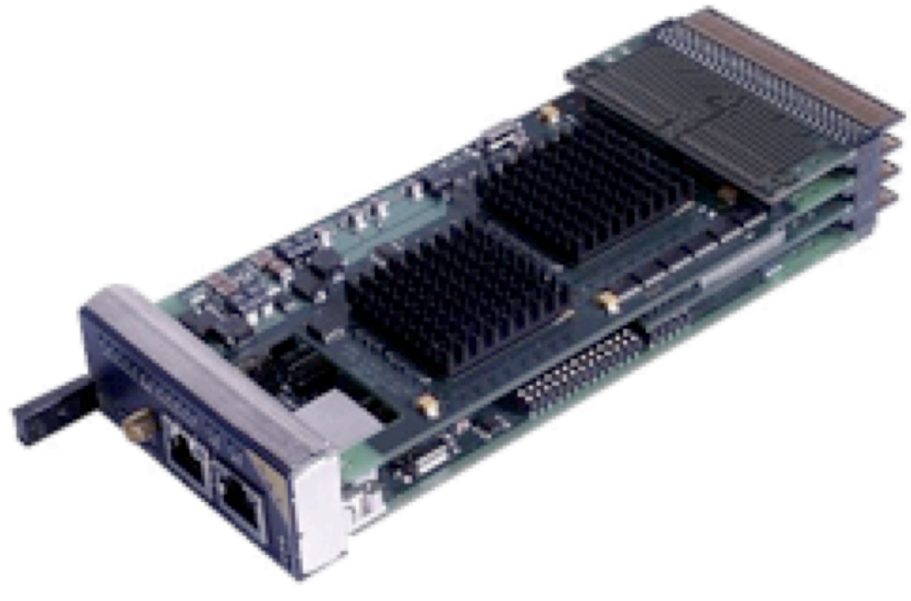
- 80W per board on 12V
- 20 LVDS lanes (Eth, PCIe being the most common protocols used)
- Dedicated clock lines
- Board management based via IPMI
- It is powerful enough to be a stand alone system and so uTCA started

uTCA

- Standardized in 2006 by PICMG
- Min signaling speed is 3.125 GHz
- It requires MCH board (Micro TCA Controller Hub) with up to 7 AMC per MCH
- Possibility to have redundant MCH
- Up to 8 LVDS pairs for data transfer trough the switch (fat pipes)
- Protocol not defined but Ethernet and PCIe are the most common
- In single width can have 1 FMC per board on the front panel (2 in double width)
- Each AMC need a MMC implementing IPMI

uTCA





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Some uTCA products

- 19” rack mountable
- Dual star backplane
- Up to 10 AMCs
- External AC->DC PSU required

- 2U / 19” chassis
- Slots for up to 12 AMCs
- Cooling dimensioned for 40W per slot

MCH

- Fat-pipe mezzanines for:
  - PCIe
  - 10GB-Eth
  - Serial RapidIO
  - Clocks

- 19” rack mountable
- 8 full size and 4 compact size AMC slots
- For 3rd party power supply modules

- 6 mid size (single or double width) AMCs
- AC or DC PSU
- Single star backplane

Slide from Markus Joos (CERN)

Some uTCA products

Some interoperability issues have been noted between products from different vendors due to ‘grey zones’ in the IPMI Standard

https://twiki.cern.ch/twiki/bin/view/XTCA/WebHome

- 19” rack mountable
- 8 full size and 4 compact size AMC slots
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- 6 mid size (single or double width) AMCs
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Put pipe mezzanines for:

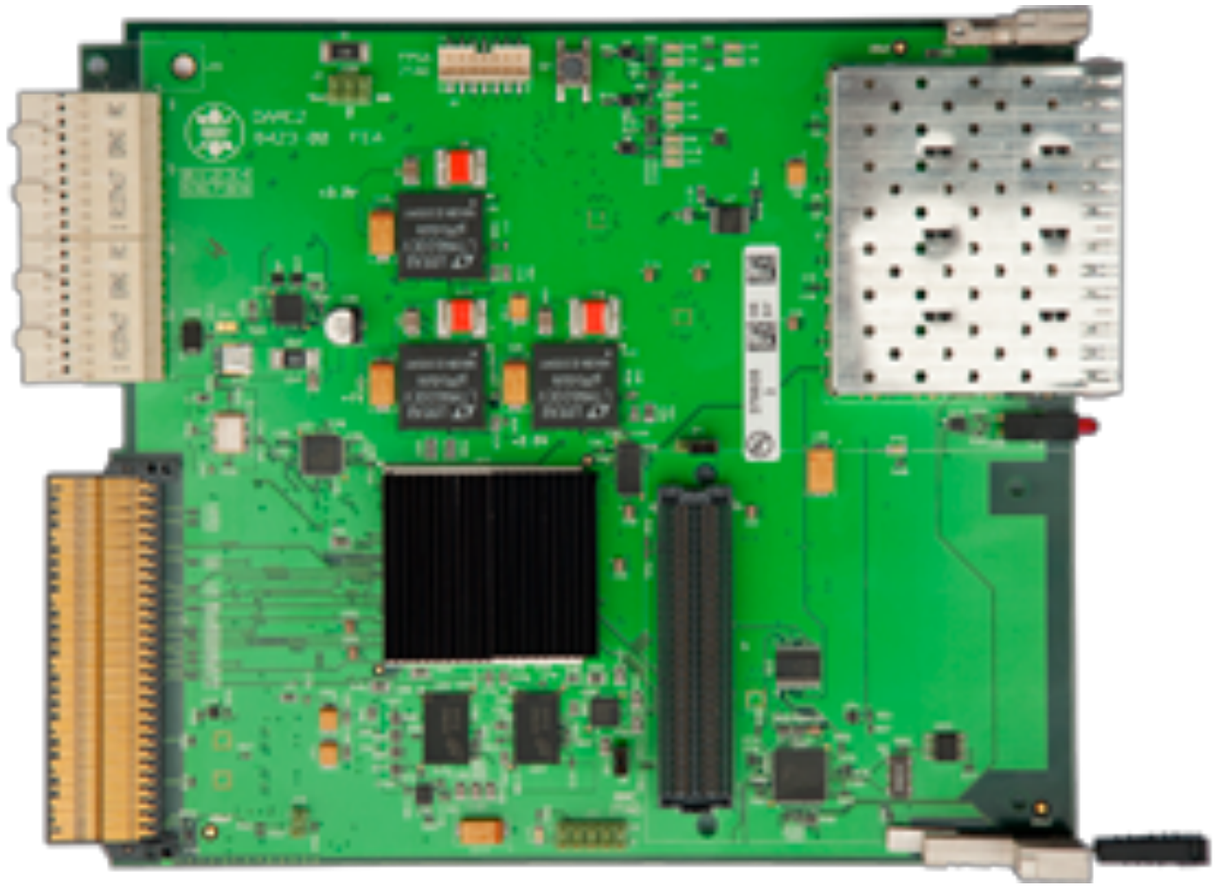
- PCIe
- 10GB-Eth
- Serial RapidIO
- Clocks

Slide from Markus Joos (CERN)

MTCA.4 (uTCA for Physic)

- Under ratification process
- Reduce a bit the freedom of uTCA to simplify and standardize the use of synch signals
- PCIe is the strongly reccomended protocol for the communication
- It introduces the possibility to have an RTM of the same size (MTCA + RTM adds up to a real estate of about 125% of a 6U VME board)

MTCA.4 example



- Carrier for 1 FMC
- 4 SFP on the front panel
- Many ongoing RTM designs

http://tesla.desy.de/doocs/doocs.html

So many options….

- Which one to choose may depend on technical or historical reasons
- Try to communicate, even if we are using different busses we can still share alot
- Dropping a bit of freedom we might end up with more synergies: try to share your design and be ready to get external inputs/ requirements
    - the Open Hardware Repository (www.ohwr.org) is a good place to start
- Most systems are based on FPGAs.
    - Lets try to use the same architecture: the use of the same internal bus simplify code exchange
    - Lets try to use as much as possible free and vendor independent modules (www.OpenCores.org)

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Thanks for your attention