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DESIGNING ELECTRONICS FOR USE IN RADIATION ENVIRONMENTS

10th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators, DIPAC2011, Hamburg, Germany, May 16th—18th, 2011

Introduction

System errors or even failures due to ionising radiation has become common in accelerators

- More accurate acquisitions and more data are requested:
  - more electronics closer to the beam
  - higher performance devices used
- Technology has shrunk and packed more transistors per cm^2

LHC 2011 - latest news

Day	Summary
Labour day	• Overnight fill lost at 5:30 to BLM communication problem (~30 pb-1) • Access for QPS and vacuum (insulation vacuum triplet L5) • Head for 768 physics, into stable beams at around 19:00, initial lumi around 8e32 • Fill lost around 20:30 to collimator position interlock - possible SEE • Access required for QPS controller reset
Saturday 30th April	• Lost ramp for physics around 2:30 - vacuum spike - R2. • Back in physics 06:40, fill lost to octupole power converter trip 08:20. • Back in physics 13:30
Friday 29th April	• reasonable fill in overnight (25 pb-1) • dumped at 11:00, access for QPS reset (SEU)... • quick look at Abort Gap Keeper in the afternoon • Around 17:00 - major power glitch - 6 sectors & Atlas down • Beam back around 21:30, dynamic correction of b3 trial plus test ramp in shadow of Atlas ramp-up
Thursday 28th April	• 09:00 overnight fill lost - slow beam loss - vacuum spike • Access - QPS reset (SEU) • Stable beams briefly - fill lost to controls rack crash • Back in stable beams around 22:00
Wednesday 27th April	• 07:10 Fill 1739 dumped - cryo problem - cooling • Access for Atlas. • Injection 624 bunches, problem with fill pattern • injection 624 bunches, ramp squeeze, lumi, stable conditions
Tuesday 26th April	• 04:50 Cryo problem in point 2. End of fill 1736 • 08:00 Cryo recovered. • Various accesses - including energy extraction fix in S34. • Lost ramp - BPM communication • Switched LHCb polarity • Access for cryo - filter problem • 23:00 Fill 1739 - **5.2 x10^{32} cm^{-2} s^{-1}** (ATLAS)
Monday 25th April	• **12:00 150 pb^{-1} in 2011** • 13:30: dump fill 1735, 20 pb-1 integrated luminosity. • 16:20: Stable beams fill 1736, 480 b/72b per injection. Initial luminosity up to **~4.3x10^{32} cm^{-2} s^{-1}** (ATLAS)/**~4x10^{32} cm^{-2} s^{-1}** (CMS). • 20:40 Beam dump due to losses induced by vacuum spike on vacuum gauge close to triplet R8. End of fill #1736 • 23:45 Stable beams fill 1736, 480 b/72b per injection. Initial luminosity up to **~4.8x10^{32} cm^{-2} s^{-1}** (ATLAS)/**~4.4x10^{32} cm^{-2} s^{-1}** (CMS).

Outline

- Radiation to Electronics Jargon
- Physics Background
- Mitigation techniques in FPGAs
- Planning and Irradiation

Single Event Effects (SEE)

- Single Event **Upset** (SEU)
  - State change, due to the charges collected by the circuit sensitive node, if higher than the critical charge (Qct)
  - For each device there is a critical Linear Energy Transfer (LET) value
- Single Event **Functional Interrupt** (SEFI)
  - Special SEU, which affects one specific part of the device and causes the malfunctioning of the whole device
- Single Event **Latch-up** (SEL)
  - Parasitic PNPN structure (thyristor) gets triggered, and creates short between power lines
- Single Event **Gate Rupture** (SEGR)
  - Destruction of the gate oxide in the presence of a high electric field during radiation (e.g. during EEPROM write)
- Single Event **Burnout** (SEBO)
  - Destructive; occurring in power MOSFET, BJT (IGBT) and power diodes

Definitions and Units

- Flux:
  - Rate at which particles impinge upon a unit surface area,
  - given in particles/cm^2/s
- Fluence:
  - Total number of particles that impinge upon a unit surface area for a given time interval,
  - given in particles/cm^2
- Total dose, or radiation absorbed dose (rad):
  - Amount of energy deposited in the material (per mass)
  - 1 Gy = 100 rad
- Linear Energy Transfer (LET):
  - The mass stopping power of the particle,
  - given in MeV*cm^2/mg

Definitions and Units

- Cross-section (σ):
  - The probability that the particle flips a single bit,
  - given in cm^2/bit, or cm^2/device
- Failure in time rate (in 10^9 hours):
  - FIT/Mbit = Cross-section*Particle flux*10^6*10^9
- Mean Time Between Functional Failure:
  - MTBFF = SEUPI*[1/(Bits*Cross-section*Particle flux)]

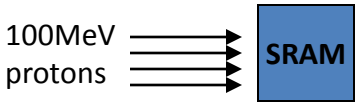
Example: SEU cross-section calculation

- Sensitivity of a circuit to SEU is characterized by a cross-section
- The cross-section contains the information about the probability of the event in a radiation environment

Example:

What is the error rate of an **SRAM** in a beam of 100MeV protons of flux 10^5 p/cm^{2}s?

1. Take the SRAM and irradiate with 100MeV proton beam. To get good statistics, **use maximum flux available**
(unless the error rate observed during test is too large, which might imply *double errors* are not counted => error in the estimate)



2. **Count the number of errors** corresponding to a measured fluence (=flux * time) of particles used to irradiate

Example:
N of errors = 1000
Fluence = 10^{12} p/cm^2

Cross-section (s)= N/F = 10^{-9} cm^2

3. Multiply the cross-section with the **estimated flux** of particles in the radiation environment to be used. The result is directly the error rate, or number of errors per unit time.

If (s) = 10^{-9} cm^2

and flux = 10^5 p/cm^{2}s

Error rate = 10^{-4} errors/s

e.g. In a system with 1000 SRAMs: 360 errors/hour to be expected

Example: Failure rate calculation

- Example:
  - FIT/Mb = 100
  - Configuration memory size = 20 Mb
  - FIT = FIT/Mb * Size = 2000,
  - i.e. 2000 errors are expected in 1 billion hours

  Note: fluence above is 14 n/hour

- Expected fluence: 3×10^{10} n/10 years
  - # of errors in 10 years =
    $2000 \times (3 \times 10^{10} / 14 \times 10^{9}) = 4286$

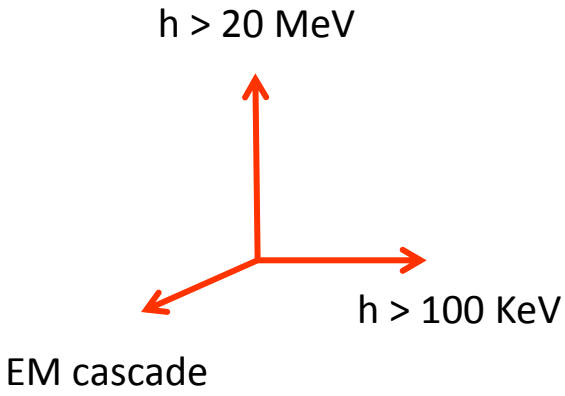
- Taking into account the SEUPI factor:

  Note: SEU Probability Impact = 10 for conservative or 100 for relaxed
  - # of errors in 10 years =
    $4286 / 10 = 428$

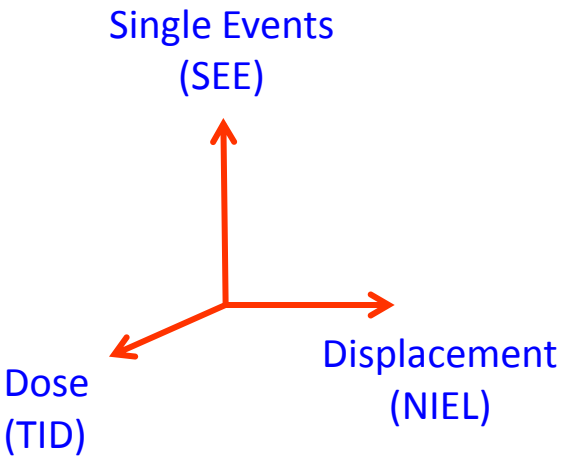
PHYSICS BACKGROUND

Radiation Engineering

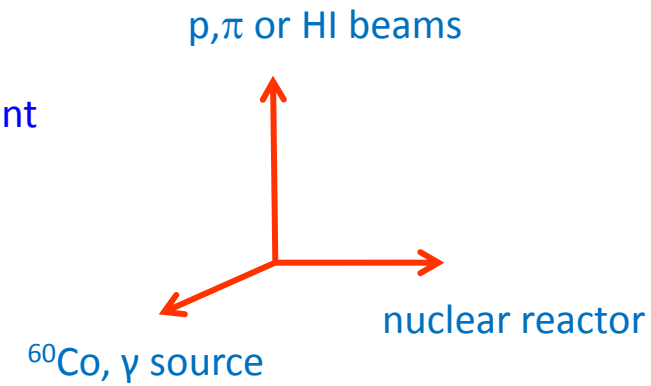
The effects are different for the different radiation impacts, meaning also different testing is needed for each case.



nuclear cascade



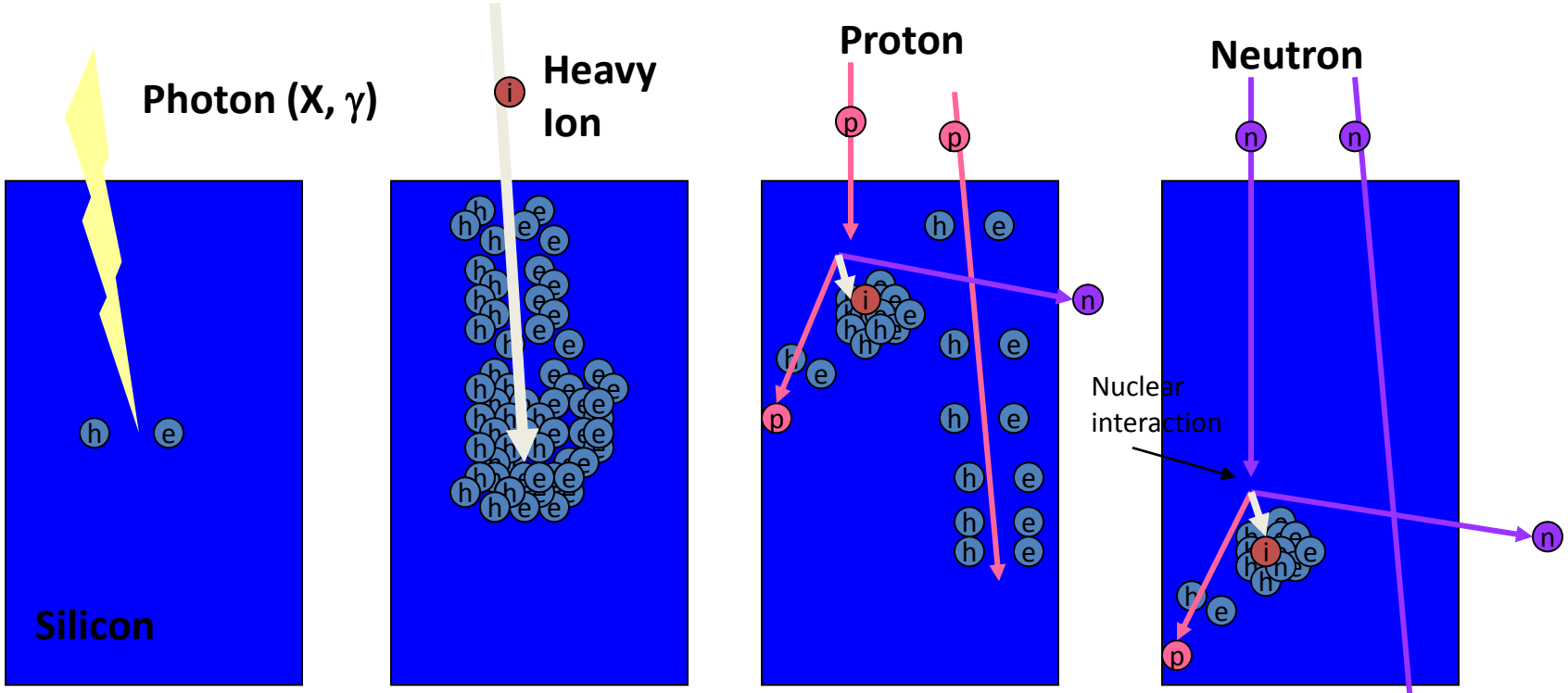
radiation damage semiconductors



Radiation Testing

Ionization from different radiation

- Traceable to the energy deposition initiated by one single particle, in a precise instant in time. Due to its stochastic nature, this can happen at any time – even at the very beginning of the irradiation
- Which particles can induce SEEs? In the figure below, a schematic view of **the density of electron-hole pairs created by different radiation** is shown.



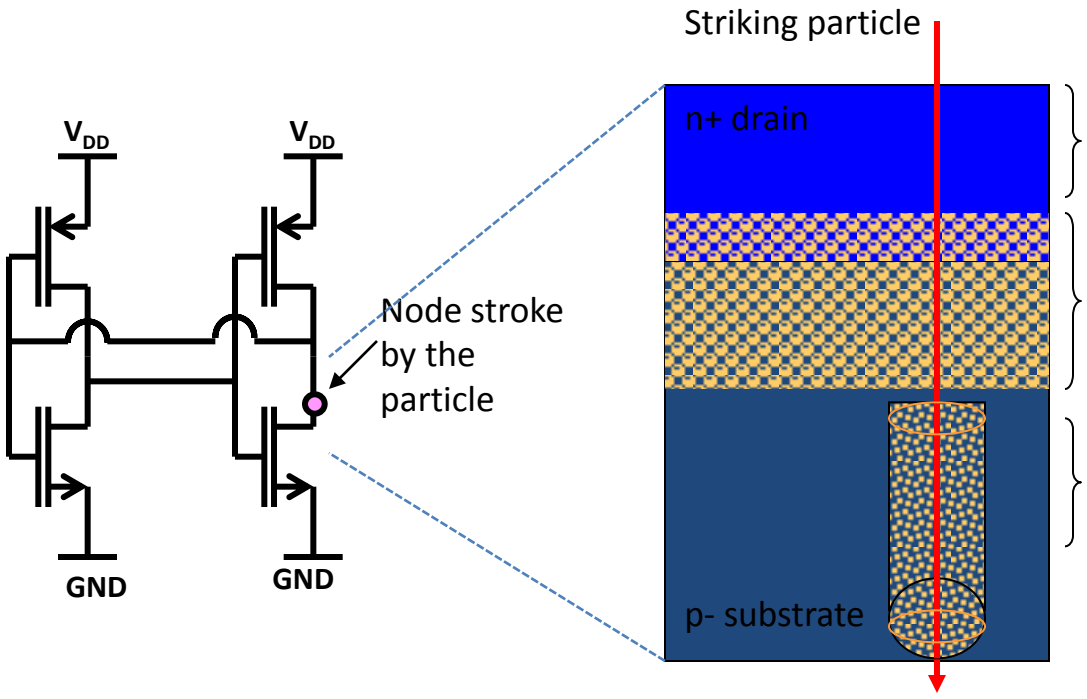
Small density of e-h pairs

Large density of e-h pairs

Small (proton) or no (neutron) density for direct ionization. Possible high density from Heavy Ion produced from nuclear interaction of the particle with Silicon nucleus.

Single Event Upset (1)

The electron-hole pairs created by an ionizing particle **can be collected by a junction** that is part of a circuit where a logic level is stored (logic 0 or 1). This can induce the "flip" of the logic level stored. This **event is called an "upset"** or a "soft error" and typically happens in memories and registers. The following example is for an SRAM cell.



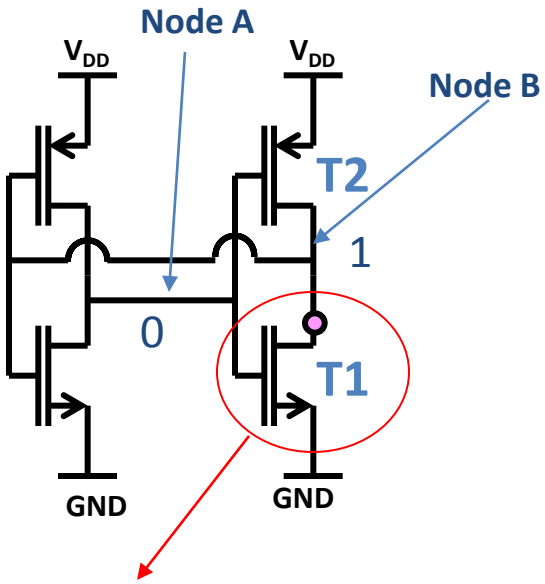
e-h pairs in this region recombine immediately (lots of free electrons available in this n+ region)

Depletion region: e-h pairs are collected by n+ drain and substrate => those collected by the drain can contribute to SEU

High density of e-h pairs in this region can instantaneously change effective doping in this low-doped region, and **modify electric fields**. This is called "**funneling**". Charge can hence be collected from this region to the n+ drain, although a portion of it will arrive "too late" to contribute to SEU

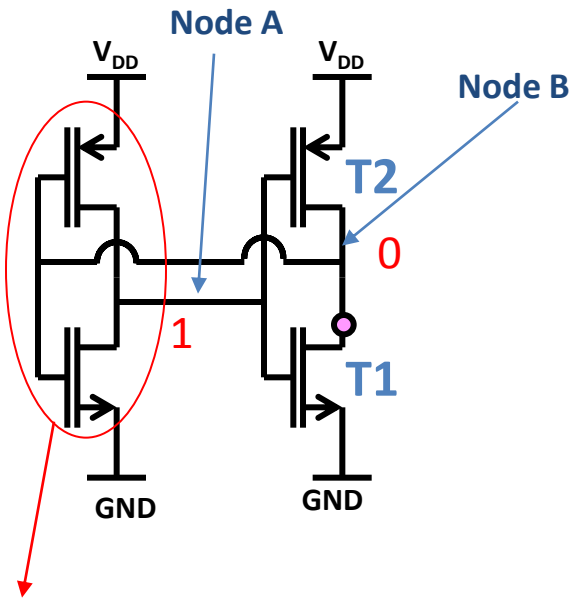
Single Event Upset (2)

1. Initial condition (correct value stored)



Charge collected at the drain of NMOS T1 tends to lower the potential of the node B to gnd. PMOS T2 provides current from Vdd to compensate, but has a limited current capability. If the collected charge is large enough, the voltage of node B drops below Vdd/2

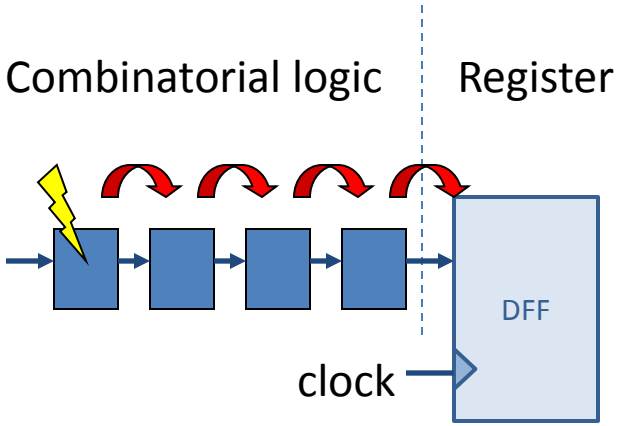
2. Final condition (wrong value stored)

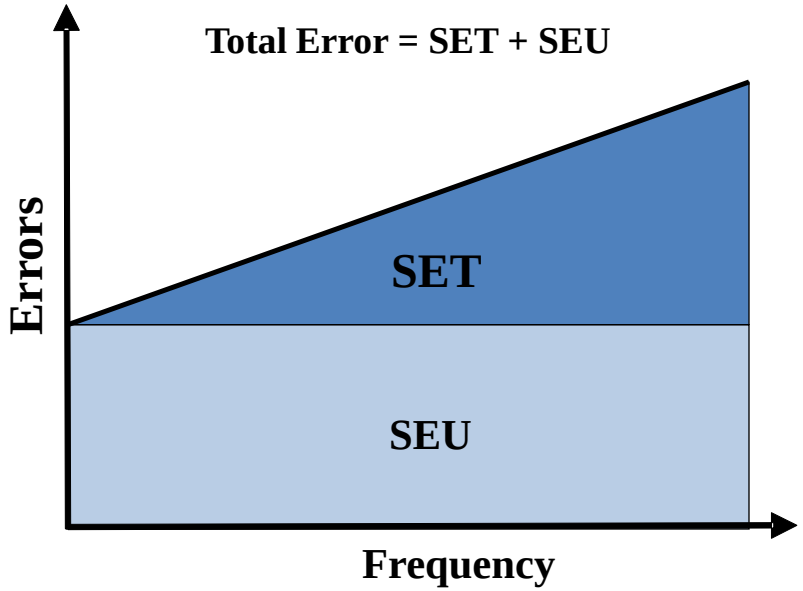


When node B drops below Vdd/2, the other inverter in the SRAM cell changes its output (node A) to logic 1. This opens T2 and closes T1, latching the wrong data in the memory cell.

“Digital” Single Event Transient (SET)

- Particle hit in combinatorial logic: with modern fast technologies, the induced pulse can propagate through the logic until it is possibly latched in a register
- Error latching probability proportional to clock frequency
- Linear behaviour with clock frequency is observed

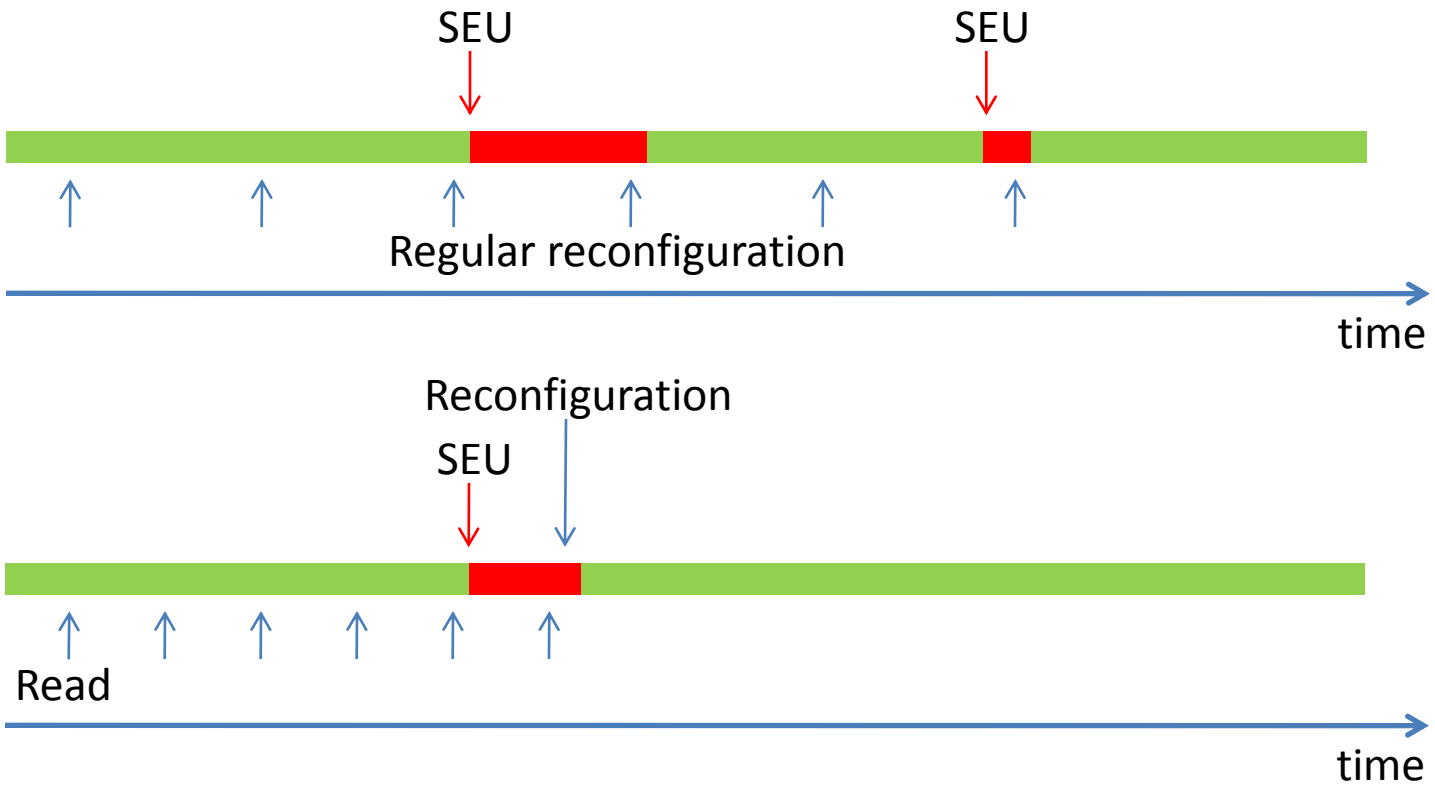




MITIGATION TECHNIQUES IN FPGA

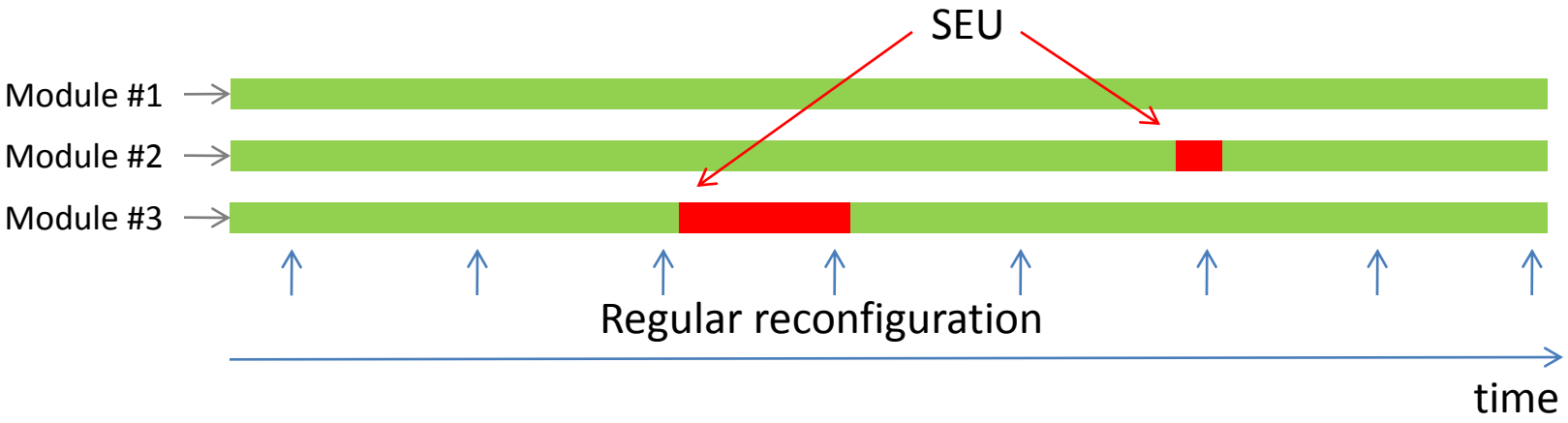
Configuration management

- Two main reconfiguration strategies:
  - On regular intervals
  - On SEU detection



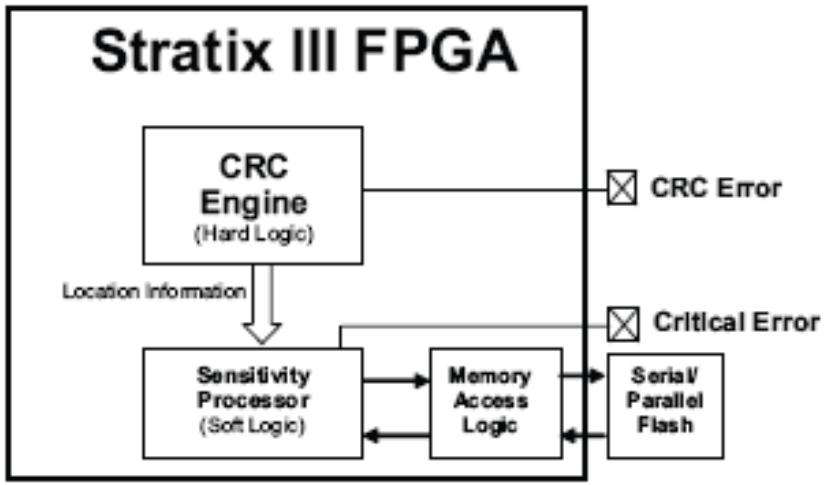
Reconfiguration: Xilinx

- Full configuration can refresh everything
  - Interruption of operation
- Partial reconfiguration (a.k.a. **scrubbing**) on regular intervals
  - The system remains fully operational
  - Some parts of the device cannot be refreshed (e.g. “Half-latch”)
  - Combine with redundancy to reduce error rate



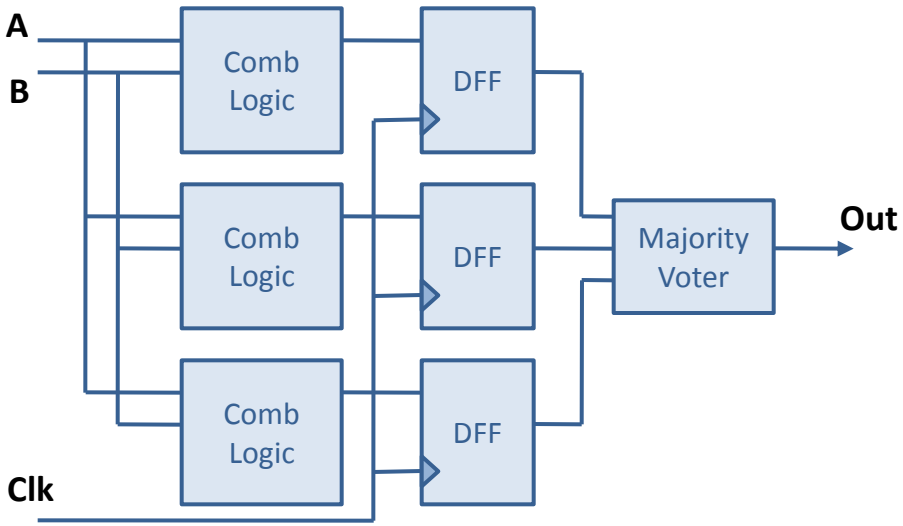
Reconfiguration: Altera

- Continuous built-in CRC detection reports changes in the configuration memory
- Location information can help to filter out the “don’t care” changes and to act upon critical errors only
  - Increase availability



- Next generation (Stratix V) will include scrubbing and reload in the background (i.e. uninterrupted operation)

Triple-module redundancy (TMR)



- It works, if the SEU
  - stays in one of the triplicated modules, or
  - on the data path
- It fails, if the errors
  - accumulate, and two out of the three modules fail, or
  - the SEU is in the voter

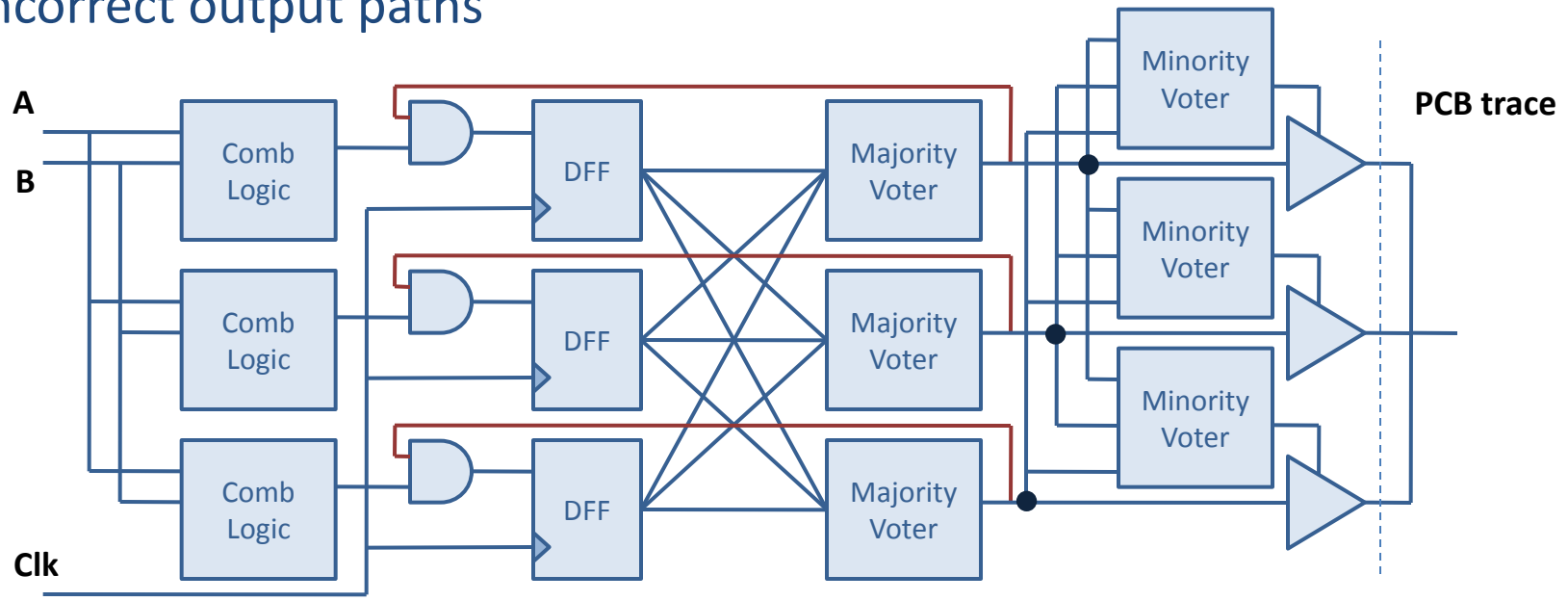
Functional TMR (FTMR)

- VHDL approach for automatic TMR insertion
- Configurable redundancy in combinatorial and sequential logic
- Resource increase factor: 4.5 – 7.5
- Performance decrease
  - more elements
  - longer paths

Ref.: Sandi Habinc http://microelectronics.esa.int/techno/fpga_003_01-0-2.pdf

Improved TMR by Xilinx

- Triplicates all inputs including clocks and throughput (combinational) logic
- Triplicates feedback logic and inserting majority voters on feedback paths (e.g. sync redundant state machines)
- Triplicates all outputs, using minority voters to detect and disable incorrect output paths



Supported by the XTMR Tool from Xilinx

State-machines

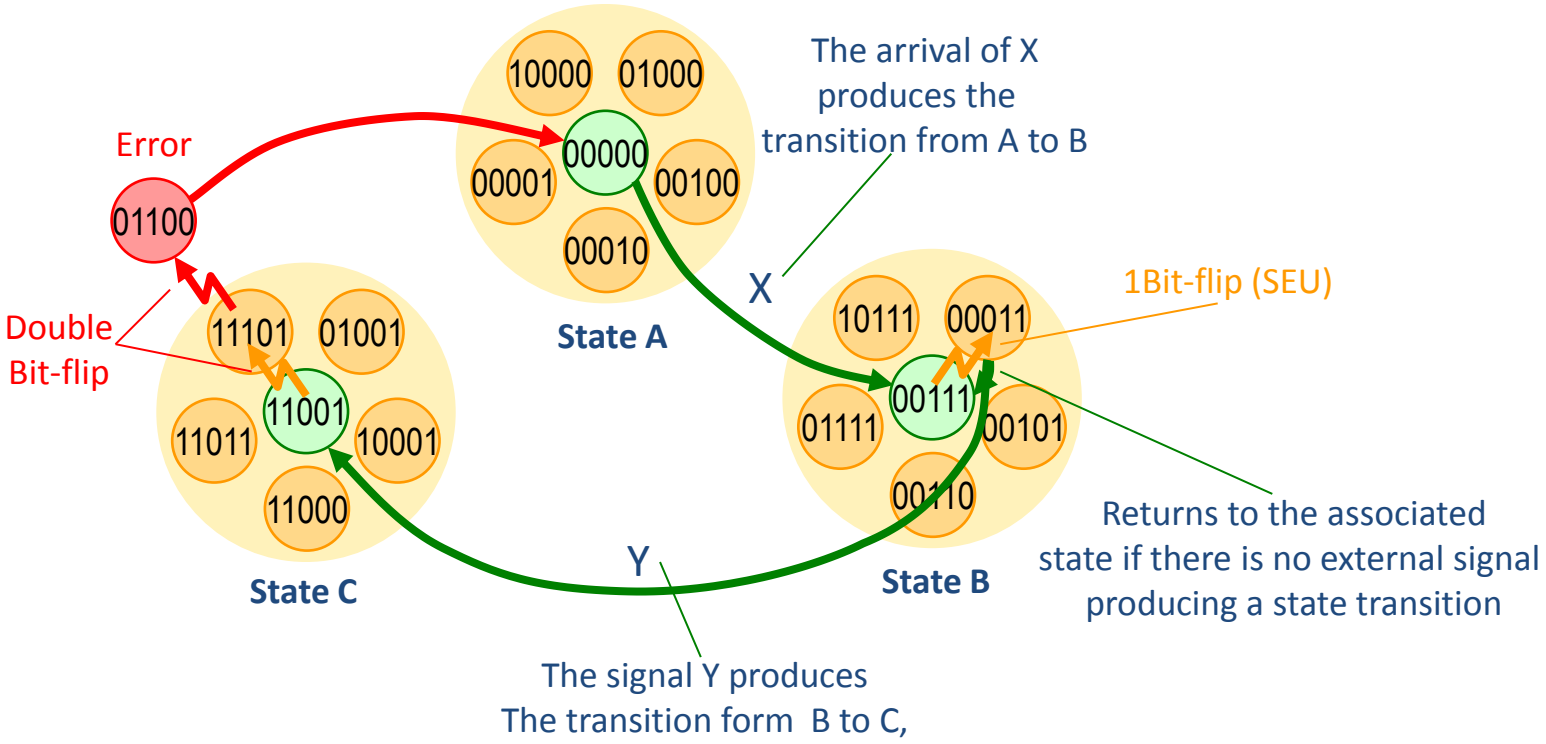
- Used to control sequential logic
- SEU may alter or halt the execution
- Encoding can be changed to improve SEU immunity
  - WARNING: be careful with synthesiser optimizations

SM type	Speed	Resources	Protection
Binary	Fast	Smallest	None
One-hot	Slow	Large	Poor
Hamming 2	Good	Moderate	Fair
Hamming 3	Slowest	Largest	Good

Ref.: G. Burke and S. Taft, “Fault Tolerant State Machines”, JPL

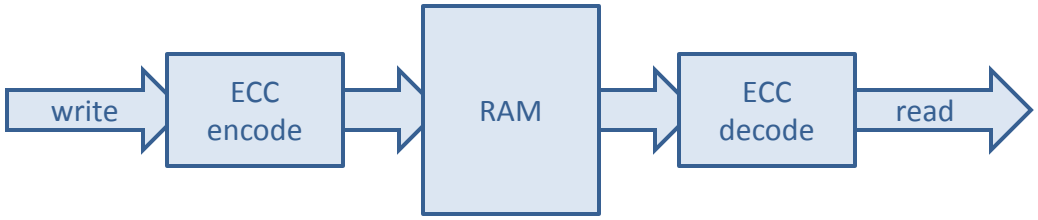
Hamming encoded FSM

- Basic principle of Hamming encoded FSM

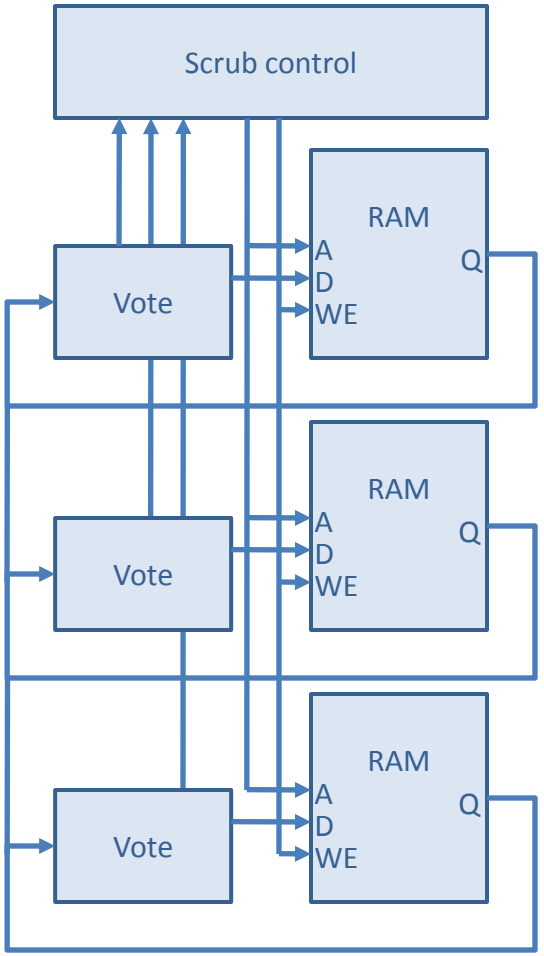


FPGA Embedded User Memory

- Very sensitive resource
  - Optimized for speed/area
  - Low Qcritical
- Errors can easily accumulate
- Mitigation techniques
  - Parity, ECC, EDAC, TRM, scrubbing
- Mitigation costs
  - Additional delay and resources

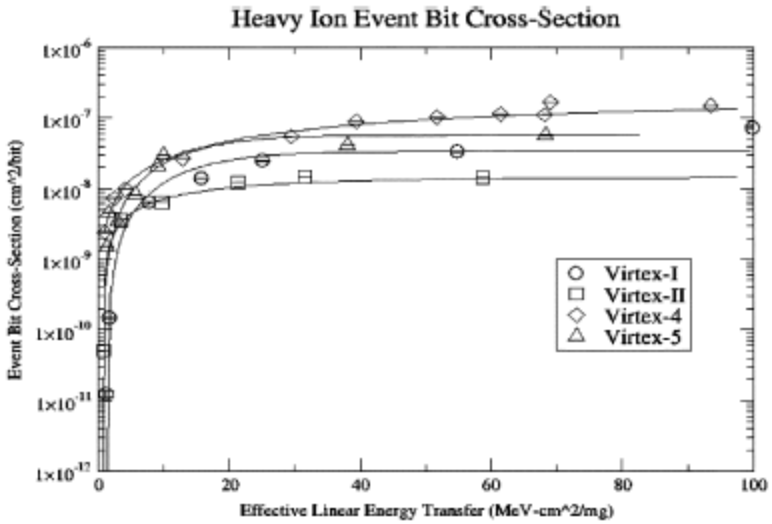


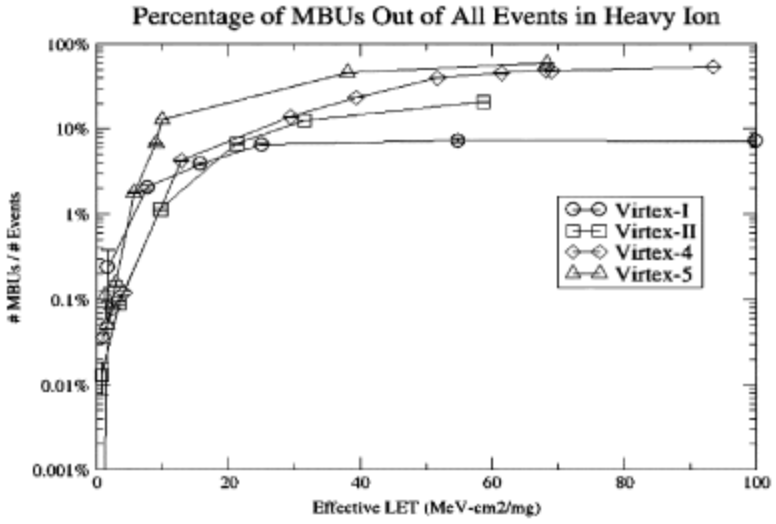
INFO: new generation FPGAs provide some of the error correction techniques as embedded cores.



Multiple-Bit Upsets

- MBUs due to single event are becoming more common in newer device families due to the decreasing CMOS transistor feature sizes
  - the critical stored charge in memory elements decreases and
  - the transistor densities increase
- The probability of defeating SEU mitigation schemes increases

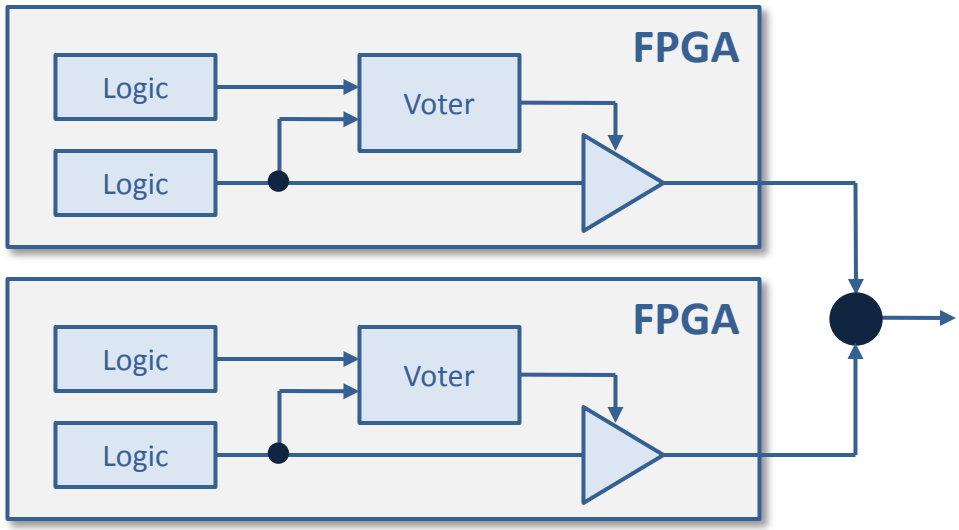




Ref.: H. Quinn et al, "Domain Crossing Errors: Limitations on Single Device Triple-Modular Redundancy Circuits in Xilinx FPGAs"

Logic Duplication

- In the case where the design is less than half the size of the total device, an alternative to logic partitioning is logic duplication.
- If logic is duplicated and outputs are compared, whenever one set of outputs differ an SEU or SEFI has been detected.
- An advantage to this method is that it is a form of device redundancy without the need for any external mitigation devices.
  - in the case of a **device failure** the redundant device would continue processing.



SRAM-based, flash-based, Antifuse (one-time programmable)

KNOWN TOLERANT FPGA DEVICES

Altera HardCopy devices

- SRAM-based FPGA is used as prototype
  - Using a HardCopy-compatible FPGA ensures that the ASIC always works
- Design is **seamlessly** converted to **ASIC**
  - No extra tool/effort/time needed
- Increased SEU immunity and lower power ☺
- Expensive ☹ and not reprogrammable ☹
  - We loose the biggest advantage of the FPGA

Xilinx Aerospace Products

- Virtex-4 QV and Virtex-5 QV
  - **SRAM-based configuration**

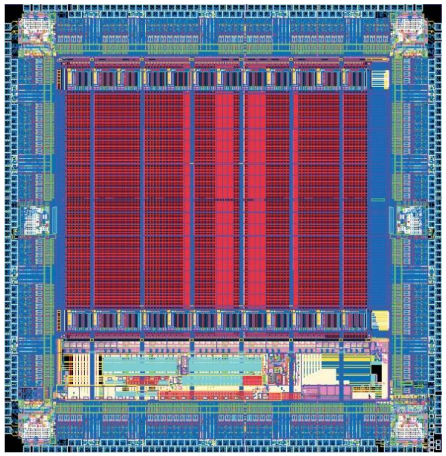
  For Virtex-4 QV:
  - Total-dose tolerance at least 250 krad
  - SEL Immunity up to LET > 100 MeV*cm^2/mg

- **Characterization reports** (SEU, SEL, SEFI):
  http://parts.jpl.nasa.gov/organization/group-5144/radiation-effects-in-fpgas/xilinx/

- **Expensive** ☹, but **reprogrammable** ☺

Actel ProASIC3 FPGA

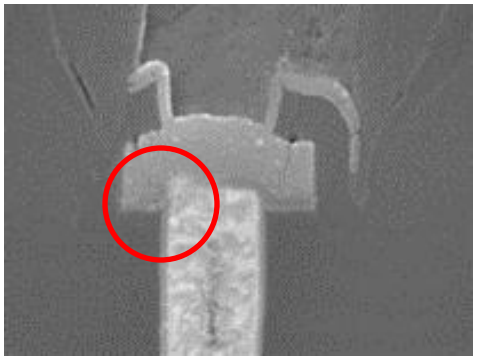
- **Flash-memory based configuration**
- 0.13 micron process
- SEL free[1]
- SEU immune configuration[1]
- Heavy Ion cross-sections (saturation)
  - 2E-7 cm^2/flip-flop
  - 4E-8 cm^2/SRAM bit
- Total-dose
  - Up 15 krad (some issues above)
- **Not expensive** ☺ and **reprogrammable** ☺



Note 1: Tested at LET = 96 MeV*cm^2/mg

Actel Antifuse FPGA

- **Non-volatile antifuse technology (OTP)**
- 0.15 micron process
- SEU immune configuration
- SEU hardened (TMR) flip-flop
- Heavy Ion cross-section (saturation)
  - 9E-10 cm2/flip-flop
  - 3.5E-8 cm2/SRAM bit (w/o EDAC)
- Total-dose
  - Up to 300 krad
- **Expensive** ☹ and **not reprogrammable** ☹



INFO: There is also available a non radiation certified low cost version

PLANNING AND IRRADIATION

Project Planning

- Define clear system **objectives**
  - avoid all parts/functions outside the scope
  - **functional specs should freeze** before design starts.
- Define the **criticality** of the system
  - e.g. what are the consequences if the system fails?
- Define the required **availability**
  - e.g. how downtime affects operations?
    Could a power-cycle be done in the *shadow*?

to determine needed effort

- Remove unnecessary external **dependencies**
  - e.g. is machine timing/synchronisation really needed?
- **Partition** system in a way that **minimises** electronics in radiation environment
  - e.g. use fast links and process the data further away

Radiation Tolerant Equipment

- Express required **tolerance**
  - in terms of TID, SEE cross section and NIEL
- Decide : off-the-shelf (COTS) or custom design
- **Irradiate** prototypes to check behaviour for:
  - Single Event Errors
  - Total Dose
  - 1 MeV neutrons
- Adequate in-situ testing with **online measurement** of key parameters plus recovery after exposure
  - indicative of dose-rate effects
- SEU testing for each **part** and **complete** system.
- Produce series with components from the same **production batch** as prototypes and pre-series

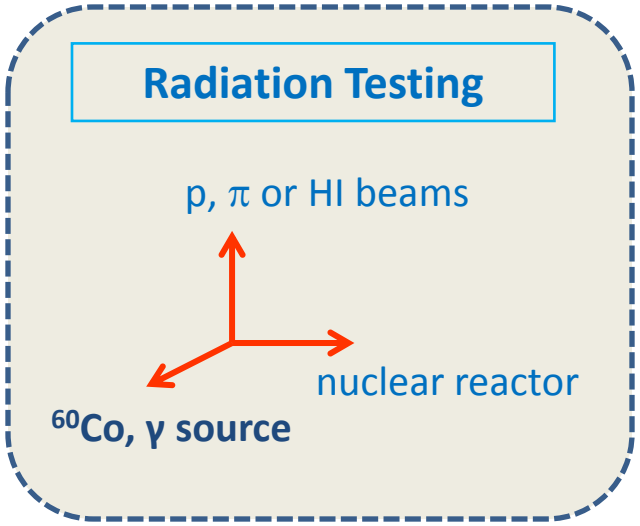
FPGA Designs

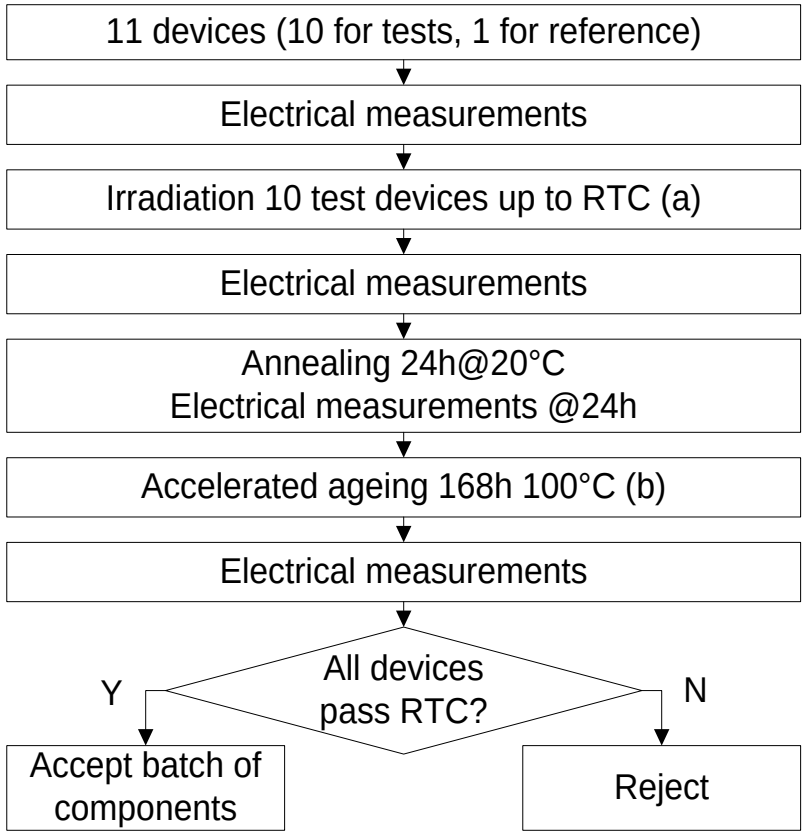
- When dealing with FPGAs, evaluate the appropriate level of **upset mitigation** needed:
  - None: if rate is acceptable and application is *NOT critical*
  - Detection only: reconfigure upon an upset
  - Full mitigation: design-level triple modular redundancy (TMR) and configuration scrubbing
- When the appropriate level of upset mitigation is selected, choose an appropriate implementation for **detection** or **scrubbing**:
  - Internal: still requires, at least, an external watchdog timer
  - External: upset-hardened application-specific integrated circuit (ASIC) or one-time programmable (OTP) FPGA

Example: Tests procedures

TID test method for qualification of batches of CMOS components

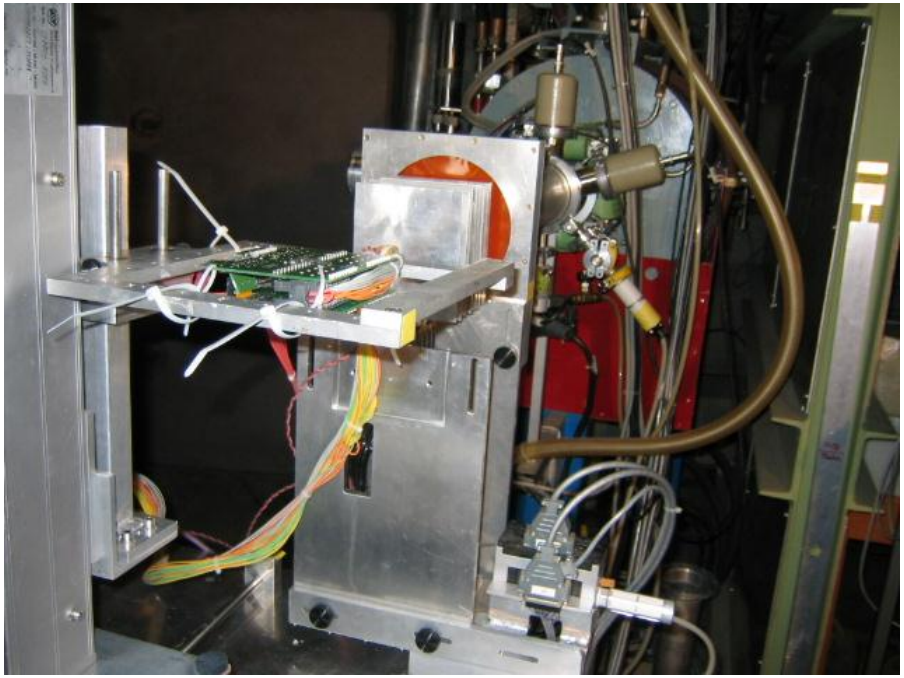
ATLAS Policy on Radiation Tolerant Electronics

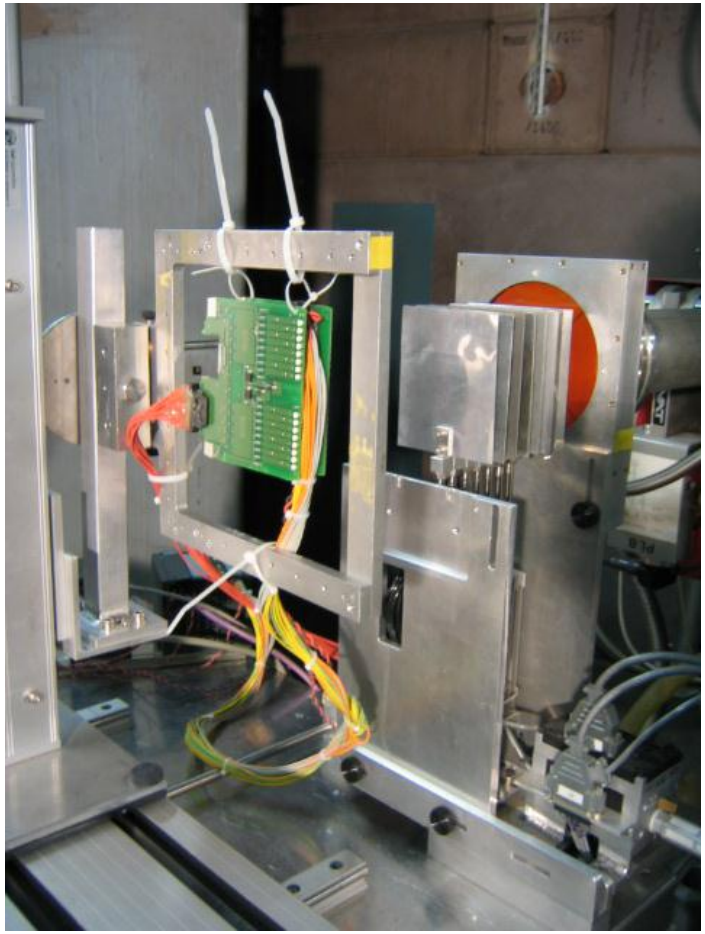




(a) RCT = Radiation Tolerance Criteria
(b) Alternatively, use appropriate safety factor and skip this step

Example: SEE testing (proton beam)





Notice:

- Angles tested
- Cables for monitoring

FURTHER READING AND ACKNOWLEDGEMENTS

Further reading

- Report on “Suitability of reprogrammable FPGAs in space applications” by Sandi Habinc, Gaisler Research
  http://microelectronics.esa.int/techno/fpga_002_01-0-4.pdf
- Assessing and Mitigating Radiation Effects in Xilinx FPGAs
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Acknowledgements

- CERN Radiation to Electronics (R2E) workgroup (www.cern.ch/R2E)
  - Federico Faccio
  - Csaba Soos
  - Thys Wijnands

Several slides from their material

Very good contacts if questions

- Altera, Xilinx, Actel documentation

THANK YOU