DIGITAL LLRF FOR IFMIF-EVEDA

Angela Salom, Alejandro Arriaga, Julio Calvo, Igor Kirpitchev, Purificación Méndez, David Regidor, Moisés Weber (CIEMAT, Madrid), Alban Mosnier (CEA/IRFU, Gif-sur-Yvette), Francis Perez (CELLS-ALBA Synchrotron, Cerdanyola del Vallès)

Abstract

The IFMIF-EVEDA project aims to build a prototype accelerator (deuteron, 9MeV, 125mA) to be located at Rokkasho, Japan, for design validation of the IFMIF Accelerator. CIEMAT from Madrid, Spain, is in charge of providing the RF systems for this prototype accelerator. The LLRF will adjust the phase and amplitude of the RF drive and the resonance frequency of the cavities. This paper summarizes its main characteristics and Control System integrated in EPICS. The hardware is based on a commercial FPGA board, an analog front end and a local timing system. Each LLRF system will control and diagnose two RF chains and it will handle the RF fast Interlocks (vacuum, arcs, reflected power and multipacting). A specific LLRF will be developed for the special case of the RFQ cavity, with one Master LLRF and three Slave LLRFs to feed the 8 RF chains of the cavity. The conceptual design and other capabilities of the system like automatic conditioning, frequency tuning for startup and field flatness of the RFQ, etc, will be shown in this paper together with the first low power test results of the LLRF prototype and the performance of the Control System.

RF SYSTEMS INTRODUCTION

The RF Systems of the IFMIF-EVEDA accelerator are composed of 18 RF plants working at 175MHz. Each chain is composed of a solid state amplifier (predriver: 400W) and two tetrodes: the driver tetrode (16kW) and the final tetrode (up to 220kW). 8 chains will be used to power an RFQ cavity (200kWx8), 2 of them will power two buncher cavities and the last 8 plants will power 8 super conducting cavities of the drift tube linac (105kWx8).

The LLRF System is based on the ALBA LLRF. It has been developed to control the three different types of cavities and each LLRF will control two RF chains. The specifications of the loops are summarized in Table 1. Some extra loops have been also added for the specific case of the RFQ cavity, as described in the following points.

Table 1: LLRF Loops Specifications

Loop	Resolution	Dynamic Range
Amplitude	< 0.5% rms	30dB
Phase	< 0.5 º rms	360 º
Tuning	< 1 º	± 90 º

LLRF HARDWARE

The main hardware components of the LLRF System are two digital commercial FPGA boards provided by Lyrtech (VHS-ADAC) plus a Windows Host PC, a front end and local timing system as depicted in Figure 1

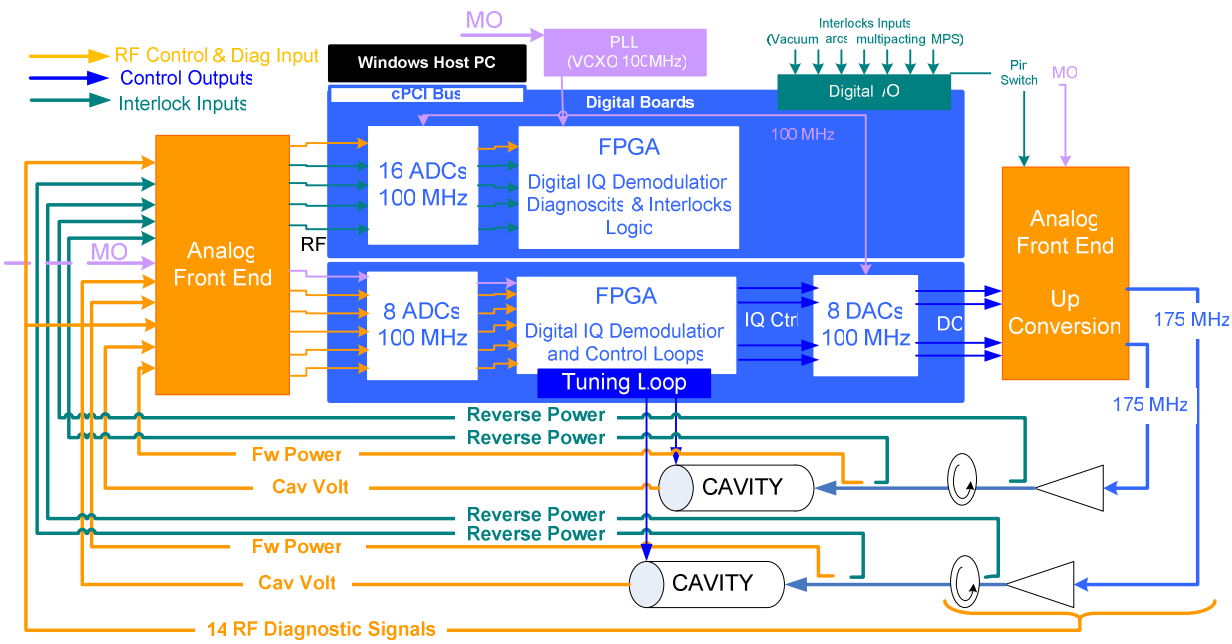

Figure 1: LLRF Hardware and Signals.

Digital Boards and Host PC

Each LLRF system employs two digital commercial boards (cPCI format) with Virtex-4 FPGA. The Loops Board has 8 ADCs (14 bits, 105MHz), 8 DACs (14 bits, 480MHz) and 128MB RAM, while the Diagnostics/ Interlock Board has 16 ADCs, no DACs and 128MB RAM

The two boards are allocated in a cPCI chassis and controlled by a Windows Host PC where the EPICS server IOC is running and taking care of the communications between the LLRF and the general control system.

Local Timing System

The local timing system consists on a PLL Board from Texas Instruments (CDC7005-EVM). It has a VCXO running at 100MHz that provides the clock for the digital board, which should be locked with the Master Oscillator input (175MHz)

Front End

The Control Outputs of the digital board are upconverted to RF using a quadrature IQ modulator. Besides this, all the RF inputs/ outputs are connected to directional couplers, whose coupling outputs are sent to BNC connectors of the Front Panel to be used as test points when required.

LLRF FIRMWARE

Undersampling + IQ Digital demodulation

The RF inputs of the LLRF are directly fed into the ADCs. These signals are undersampled at 100MHz and then they are digitally IQ Demodulated and filtered.

Amplitude and Phase loops

The outputs of the demodulation are sent to equivalent PI loops to compute the I&Q Control outputs, which will be later upconverted to RF in the front end. The gains of the loops can be adjusted by the operator to make the response of the loop faster or slower depending on the operation requirements, as well as the set points.

Mechanical Tuning Loop

The Cordic Algorithm is employed to calculate the phase difference between the Forward Power and the Cavity Voltage. A train of pulses is sent from the digital board to a motor controller to move the plunger inwards or outwards the cavity body to keep this phase difference constant and the resonance of the cavity.

A tuning deadband is also implemented to avoid oscillations of the plunger around the equilibrium point. Besides this, the tuning loop gets disabled when the Forward Power is below a given threshold that can be adjusted by the operator. This will prevent the movement of the plunger when there is no power in the cavity due to a trip in the system.

Fast and Slow Diagnostics

All the I&Q components of the RF inputs and PI Loops signals are stored in a circular buffer of 128MB at 100MHz rate, which corresponds to 335ms of operation. This information is sent to the Host PC of the System when an interlock happens and it will be used for post mortem analysis and for fast transient analysis.

On the other hand, these signals are filtered, decimated and stored in registers of the FPGA accessible by the Local Control System at 1Hz rate for slow trend analysis and archiving purposes.

Fast Interlocks

The LLRF will also control a pin diode switch that will get open when a fast interlock occurs. The interlocks controlled by the LLRF are: Reflected power of the cavity, vacuum pressure, arcs and multipacting. Besides, the Machine Protection System will be also connected to the Fast Interlock utility of the LLRF to switch off the RF Drive when required.

Beam Loading Compensation

IFMIF-EVEDA will be a continuous wave machine. In normal operation, the beam loading will be compensated by the mechanic tuning loop, which will move the plunger to recover the resonance state of the cavities.

However, to avoid high radiation levels during the commissioning of the machine, the accelerator will be tested in pulse mode. In this case, the tuning loop will also move the plunger to have the cavity on resonance when there is beam. When there is no beam, the cavity will be out of tune. In order to fill the cavities when there is no beam and thus, when the resonance frequency of the cavity is different from MO frequency, the RF Drive output of the LLRF will be modulated, i.e., the frequency will be changed to follow the resonance of the cavity and when the beam comes into the cavity, the frequency will be changed back to the MO.

Figure 2 and 3 show the simulations of he buncher cavity when it is filled with frequency modulation (Self Excited Loop (SEL)) and without frequency modulation (Generator Driven Resonator (GDR)). Beam comes into the cavity at t = 0s.

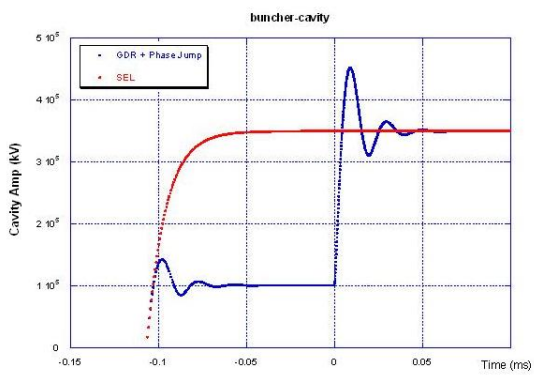

Figure 2: Cavity Voltage Amplitude with and without frequency tuning modulation during cavity filling.

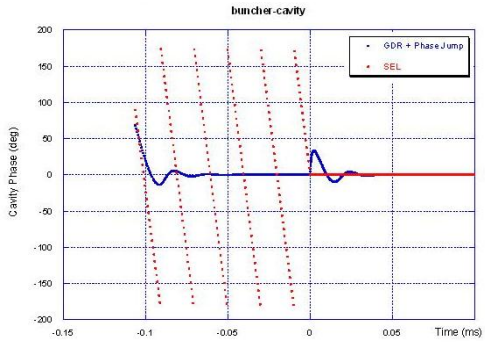

Figure 3: Cavity Voltage Phase with and without frequency tuning modulation during cavity filling.

Automatic Conditioning

The Automatic Conditioning Mode consists of a square modulation of the RF Drive, where the frequency and duty cycle of the pulses can be adjusted. When the vacuum level is below certain limits, the amplitude of the pulses is increased at a given rate defined by the operator. If the vacuum pressure increases above the upper threshold, the amplitude of the RF remains constant until the vacuum goes down below the lower limit. When this happens, the amplitude is increased again.

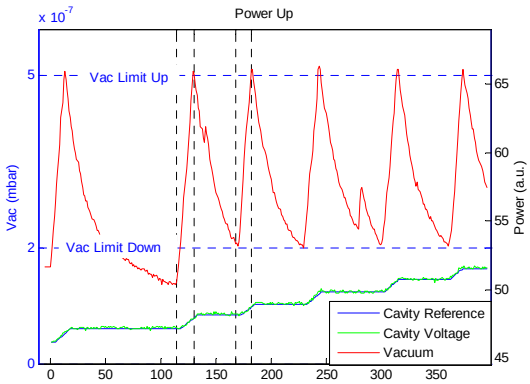

Figure 4: Automatic Conditioning of ALBA Dampy Cav.

RFQ Cavity Specific Case

The RFQ Cavity will be fed with 8 RF plants. All the cavity inputs should have same phase and amplitude to avoid mismatches and reflections. To ensure this, the RFQ LLRF is composed of one Master System, which provides the Master RF Drives and 3 more LLRF systems providing the Slave RF Drives. The Master RF Drive is obtained measuring the voltage of the cavity and using a standard PI loop. The Slave RF Drives are computed measuring the Cavity Forward Power of the slave RF chains and comparing these values with the Master Forward Power of the Cavity. A specific PI loop will keep always constant the phase and amplitude ratio between the Slave and the Master Forward Power of the cavity.

RFQ Field Flatness

There are several pick up loops to measure the voltage of the RFQ Cavity. Four of these signals will be sent to the LLRF to check the field voltage distribution in the cavity in an accurate way. This information will be sent through EPICS to the local control system of the RFQ to adjust the temperature of the sections of the cavity in order to make the field distribution as flat as possible.

Frequency Tuning for RFQ Start-up

Once the RFQ has achieved steady operation, the resonance frequency of the cavity will be adjusted keeping constant its temperature.

However, during the start-up of the cavity the cooling system will not be able to get rid off the extra heat load while powering up the cavity. This will detune the cavity and it will produce reflected power. To prevent this situation, the frequency of the Master Oscillator will be modulated by the LLRF to always follow the resonance frequency of the cavity. Once the temperature comes back to steady values, the MO frequency will be set again to operation values.

LOCAL CONTROL SYSTEM

The Local Control System of the LLRF is based on EPICS and it runs in the Windows host PC of the LLRF System. A server IOC and a Device Support have been already developed to configure the Digital Boards and to access and monitor the main parameters and signals of the LLRF

The GUI of the Local Control System has been developed using CSS (Control System Studio) and its main functionalities have been also tested.

The communications between the Local Control System and the General Control System will be done through Ethernet.

FIRST TEST RESULTS AND NEXT STEPS

The first LLRF Prototype has been already assembled and tested. The resolution of the loops at low power is within specifications (0.47% amplitude resolution and 0.08º phase resolution).

Some extra features have been also tested like the frequency tuning for startup of the RFQ and the automatic conditioning.

The second LLRF unit is ready to be assembled and next year the series production of all the systems will start. The first high power tests of the system will be done also next year to condition the cavity couplers in Madrid.

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