DIGITAL POWER SUPPLY CONTROLLER DEVELOPMENT BASED ON FPGA

R. N. Xu, W. F. Wu, S. Q. Tan, R. Li, D. M. Li, C.L.Guo, SINAP, Shanghai 201800, China
S. Li, J. S. Gou, Double-electric, Chengdu 610503, China

Abstract

A digital power supply controller developed by SSRF (Shanghai Synchrotron Radiation Facility) adopts advanced FPGA and precision ADC as core unit and data acquisition unit. The controller, which is embedded in the power supply case, is composed of FPGA and ADC cards. The controller can communicate with IOC by optical fiber with one of the Ethernet, Manchester or RS-232 mode. The parameters can be easily changed to achieve high stability and repeatability. The long-term current stability is better than 20ppm and the resolution is better than 5ppm with a 300A/60V power converter. And now there are about 300 cards used at SSRF power supplies.

HISTORY AND MOTIVATION

Shanghai Synchrotron Radiation Facility (SSRF) is in operation since May 2009. More than 650 sets of magnet power supplies were installed on the linac, booster and the storage ring. In addition, nearly 100 sets of correction power supplies were used on the insertion devices. All the power supplies work with digital power supply controllers designed by PSI or SINAP. The SINAP controllers are compatible in Hardware and control interface to the PSI controllers. Now the PSI controllers are used mainly on the large and medium power supplies, include the ring dipole and sextuplole power supplies and the booster ramping power supplies. The SINAP controllers are used on the crate power supplies, including the fast correction power supplies. The SINAP controllers are putting in use on the storage ring quadrupoles, cell to cell, in place of the PSI controllers.

The PSI controllers used in SSRF is the first generation cards and is now stop producing. The new project has special requirements on the power supplies and its controllers. Some requirements are not satisfied with the SINAP controllers used now in SSRF. Based on FPGA, a new generation digital power supply controllers with more functions and higher specifications are in developing. Hare is an introduction to the hardware and software of the controllers and the preliminary test results as well.

HARDWARD DESCRIPTION

Block Diagram

The digital power supply controller SDYK-1201 is composed of two cards, FPGA card as Figure 2 and ADC card as Figure 3.

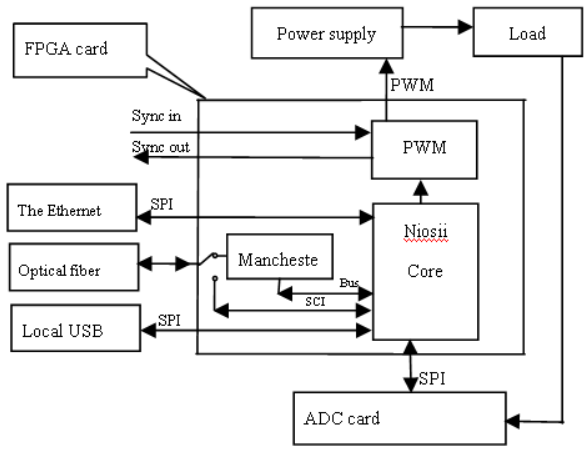

Figure 1: Block diagram.

Main Function

ADC card is used to sample the load current, load voltage and DC-link voltage.

FPGA card is used to fulfill the PID algorithm，the PWM waveform generation, digital I/O control, local communication and remote communication.

The remote controller can communicate with IOC by optical fiber via the Ethernet, Manchester or RS-232 port.

The parameters of adjusting power supply can be easily changed via local USB controller to achieve high stability and repeatability.

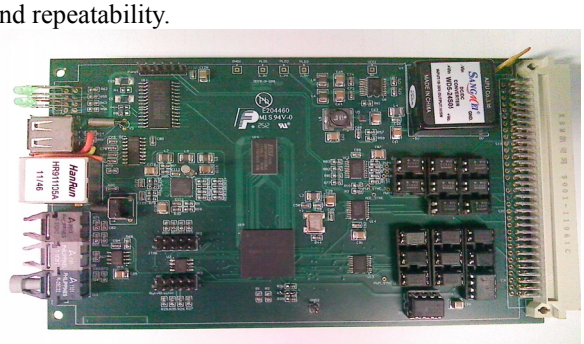

Figure 2: FPGA card.

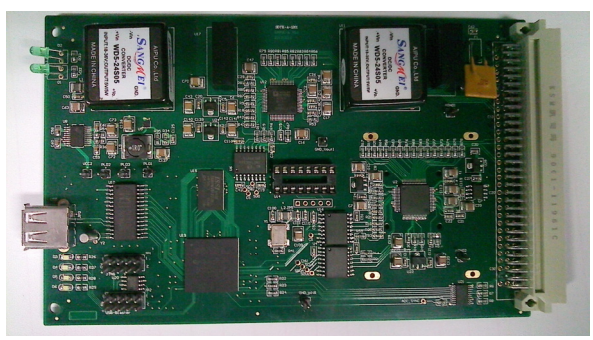

Figure 3: ADC card.

CHIP SELECTION

Control Chip

The Altera EP4CE15F17C8N has 14400 logic elements, 504Kb memory, 56 multipliers, 4 phase-locked loops, 165 pins. These resources will be sufficient to meet our requirements. To improve the computational speed and accuracy, and increased the controller's flexibility, Nios-II is used as kernel hardware floating-point arithmetic.

Flash

The Altera EPCS16 has 16Mb memory, it can be used to store the preparation of documents, procedures, power output waveform and so on.

RAM

The ISSI IS61WV51232BLL are high-speed, 16M-bit static RAMs organized as 512K words by 32 bits. It is fabricated using ISSI's high-performance CMOS technology.

Network Chip

The W5200 chip is a Hardwired TCP/IP embedded Ethernet controller that enables easier internet connection for embedded systems using SPI (Serial Peripheral Interface).

Current Sampling Chip

The ADI AD7608 has 8-channel 18-bit ADC, bipolar input, built-in benchmark, sample rate is 200 KSPS.

Voltage Sampling Chip

The ADI AD7606-4 has 4-channel 16-bit ADC, bipolar input, sampling rate is 200ksps, with programmable digital filtering. The chip can use the simultaneous sampling of the input voltage and output voltage.

FEATURES

I/O Ports

8-channel isolated Inputs
8-channel isolated Outputs

ADC Resolution

< 5 ppm

ADC Long-Term Stability

< 20 ppm

PWM Frequency

10 kHz ~ 100 kHz

PWM Mode

Chopper, H-Bridge, Phase Shift, Full Bridge

PWM Synchronization

external

Communication Function

Local Communication: USB
Remote Communication: Ethernet, Manchester, RS-232

Waveform Function

Waveform Storage
Multipoint Trigger

PID ALGOITHRM

PID algorithm is fulfilled in FPGA card, the load current is filtered and compared with the reference value for PID control. The DC-link voltage is filtered for power supply protection and/or for feed forward control. The output is passed to PWM modulator for PWM signals. Figure 4 shows the PID algorithm.

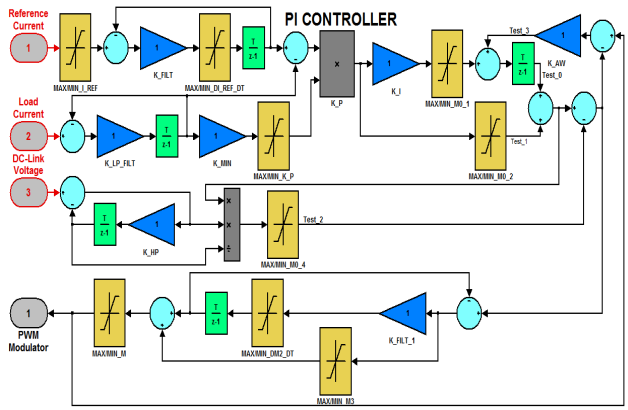

Figure 4: PID algorithm,

RESULTS

The controller is mainly used in middle power supplies in SSRF, and it could accord with all the technical requirements of the facility.

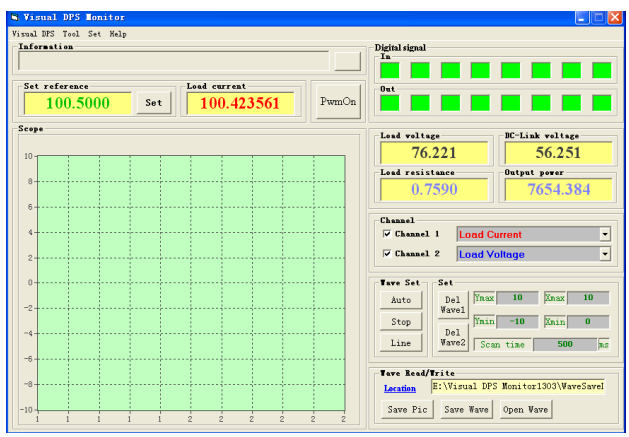

Figure 5: Local control menu.

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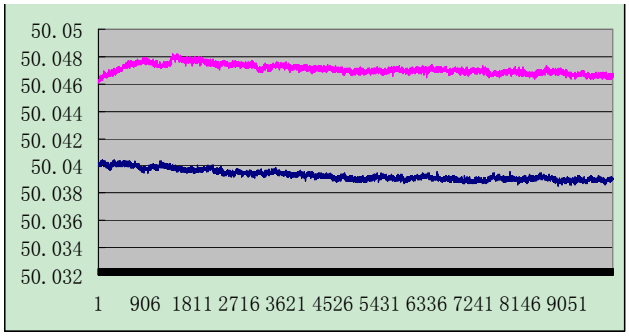

Figure 6: Long term stability at 50A.

Long term stability better than 20 ppm.

CONCLUSION

The controllers are based on FPGA and have many new features. The controller cards are manufactured and are in testing and commissioning: ADC resolution, the temperature coefficient, control interface, waveform function, and so on. The test and commissioning is expected to be finished by the end of this year.

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