A METHOD OF IMPLEMENTING HIRFL-CSR CHOPPER CONTROLS

Kewei Gu, Shi An, Xiaojun Liu, Wei Zhang, IMP, Lanzhou, China

Abstract

A method of implementing controls of chopper for HIRFL-CSR (Heavy Ion Research Facility of Lanzhou and Cooler Storage Rings) is introduced. This method is based on an ARM and DSP co-operation system structure. The control algorithm of this method is based on a data structure which is defined and implemented in the DSP module. Output data is created by the control algorithm and the actually pulse output is triggered by a timer which is achieved through a logic circuit actualized in a FPGA chip. The results show that the method is flexible and the control system matches the chopper regulating requirements.

MOTIVATION

HIRFL-CSR (Heavy Ion Research Facility of Lanzhou and Cooler Storage Rings) was built up in 1988 [1,2]. It is now one of the world large heavy ion accelerators. As the beam requirements of experiment terminators have become more and more critical, many improvements have been carried out to increase beam time and beam efficiency. One of these improvements is time-sharing [3]. It means that experiment terminators make use of beam in their time slices. Chopper is the main device to achieve time-sharing, also it controls transformation of work modes [4]. The control of chopper is implemented by an ARM and DSP co-operation system. Its goal is to produce real-time single or continuous pulses which meet the requirements specified by control parameters.

HARDWARE PLATFORM

The chopper control system is based on an ARM-DSP hardware platform. The arm board is connected with DSP board via VME bus [5]. They apply to different functions. The ARM board acts as an interface to control terminators. It receives commands or data via internet and sends them to DSP board through HPI bus also it sends back messages to control terminators to indicate current states. The DSP board analyses the received data， which contain control parameters, generates the needed data accordingly and outputs it. So when the trigger events come, the DSP board outputs the required pulses and controls the chopper to work properly. The structure of hardware platform is shown in Fig. 1.

CONTROL DATA STRUCTURE

The control algorithm is based on a control data structure. It defines such parameters as:

Single pulse time.
Single pulse delay.
Periodic pulses time.
Periodic pulses period.

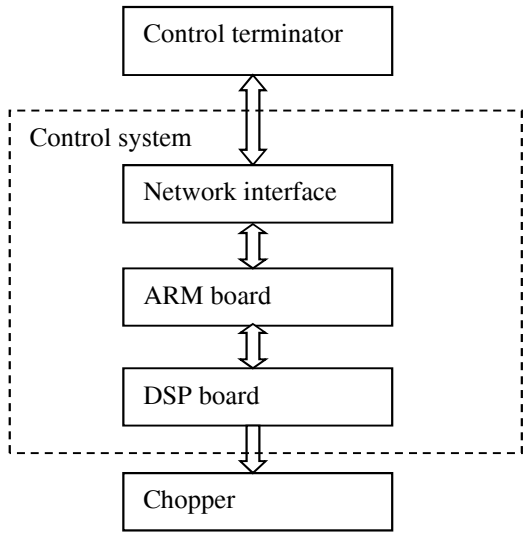

Figure 1: Structure of hardware platform.

These four parameters give requirements. When ARM board transforms them to DSP board, it writes them to the memory where the control data structure is allocated. It also sets a flag to indicate parameters updated. There is a timer interrupt service routine which checks the flag periodically. When it detects flag set, it accesses the control data structure, reads control parameters, and produces output data. The output data is stored in another memory area. The output data is produced by the algorithm shown in Fig. 2.

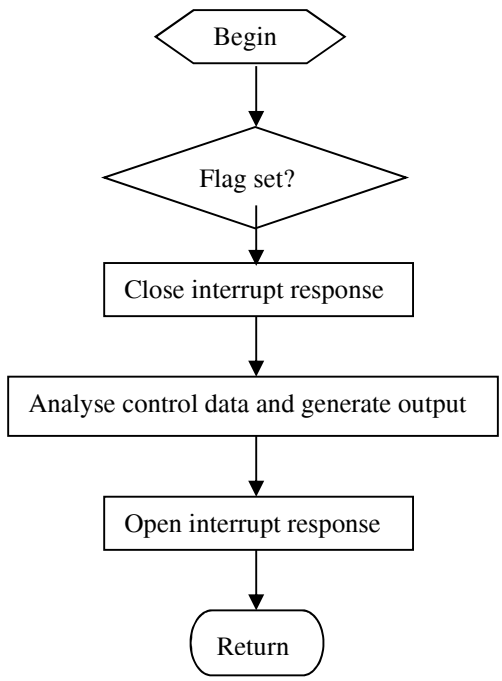

Figure 2: Algorithm of generating output data.

ISBN 978-3-95450-122-9

DATA OUTPUT

The generated output data is stored in a fixed memory area. The data is prepared for being transmitted to a DAC. Between DSP module and DAC module, there is a FPGA module, which routes output data to DAC module. Also, it receives trigger events which comes from an event generator. When the output event comes, it produces an interrupt to DSP and the corresponding interrupt service routine then writes output data to the FPGA buffers. The DSP's work is completed by now. The last step of the output is transmitting output data to DAC, and it is achieved by FPGA. The FPGA module not only transmits data to DAC but also does some signal-processing works to smooth output. So the satisfying output wave is achieved. Figure 3 shows the output algorithm.

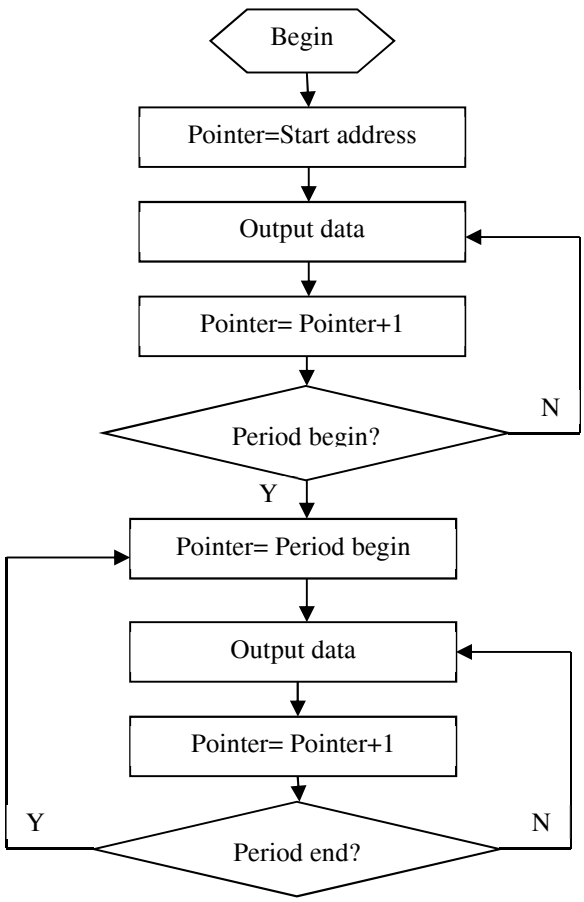

Figure 3: Algorithm of data output.

RESULT

The DSP chip is TMS320C6713, the development environment is CCS 2(Code Composer Studio 2). Code Composer Studio extends the capabilities of the Code Composer Integrated Development Environment (IDE) to include full awareness of the DSP target by the host and real-time analysis tools.

The data transmission is time critical for the FPGA output is real-time and the speed is 1MS/s. The length of FPGA buffer is 16 words. Because the FPGA also does some signal-processing works to smooth output, the maximum theory time that output interrupt service routine can consume is 32 us. The CPU clock consumed by this routine is shown in table 1. So it can be concluded that the output interrupt service routine consumes 14.1us at maximum and 14.0 us at minimum, and that means the output interrupt service routine can meet the requirement of output time.

Table 1: Functions Analysis

Functions	Code Size	Incl Max	Incl Min
Int_dac()	392	2823	2803

Given parameters as:
Single pulse time = 100us.
Single pulse delay = 200us.
Periodic pulses time = 100us.
Periodic pulses period = 200us.

The output wave is shown in Fig. 4. It matches the control parameters.

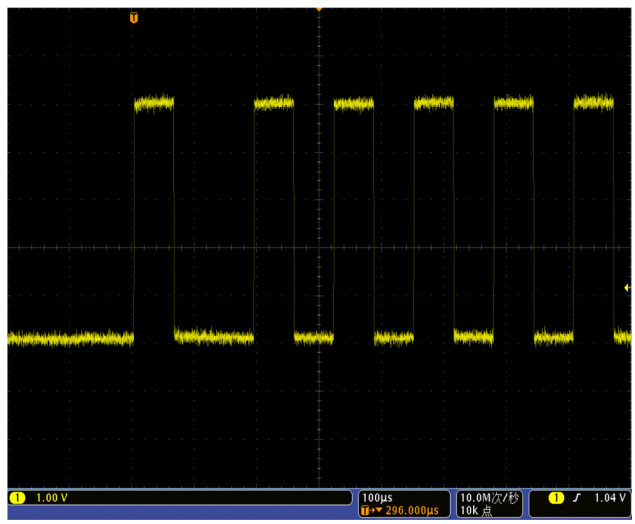

Figure 4: Output wave.

REFERENCES

[1] Xiao Guoqing, Li Zhenzhong, "Heavy ion research facility in Lanzhou", Bulletin of Chinese Academy of Sciences, 2009. 24(1). 97-101.
[2] Xia Jiawen, Zhan Wenlong, Wei Baowen, "Heavy ion ring project in Lanzhou", Nuclear Physics Review, 2001. 18(1).35-38.
[3] Zhu Kun, Zhang Jianquan, "New beam distribution system", High Energy Physics and Nuclear Physics, 2003.27(8). 731-734.
[4] Ziyun Jiang, Wei Zhang, "Chopper mode analysis of beam distribution based on time in HIRFL", High Power Laser And Particle Beams, 2011. 23(8). 2183-2186.
[5] JI Peng, Qiao Weimin, Jing Lan, "Power Supply Control System of CSRm Based on ARM and DSP", Nuclear Electronics and Detection Technology", 2008.28(4). 728-730.