REGAE LLRF CONTROL SYSTEM OVERVIEW

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Abstract

The linear accelerator REGAE (Relativistic Electron Gun for Atomic Exploration) at DESY delivers electron bunches with a few femtosecond duration for time-resolved investigation of material structures in a pump-probe configuration. To achieve a sub-10fs resolution, the Low Level RF controls for the normal conducting S-band cavities, must provide field stability of .005% in amplitude, and of .005° in phase. To achieve these demands, the recently developed LLRF control modules based on the Micro-Telecommunications Computing Architecture (MTCA.4) platform will be used.

For precise field detection and control, a rear transition module (DRTM-DWC8VM1) housing 8 down-converters and 1 vector-modulator has been developed. The down-converted signals are transmitted to low-noise ADCs on an advanced mezzanine card (SIS8300L) with two high speed DACs driving the vector-modulator. The on-board FPGA device runs the advanced control algorithms with minimum latency. Shot-to-shot learning feed forward and ultra-fast analog and digital feedbacks are applied. In this paper, the new hardware platform is described and the proposed algorithm is discussed.

INTRODUCTION

The linear accelerator REGAE (Relativistic Electron Gun for Atomic Exploration) at DESY delivers electron bunches with a few femtosecond duration for time-resolved investigation of material structures, in a pump-probe configuration. The electrons of a pC bunch charge are emitted by impinging picosecond laser pulses onto a photo-cathode mounted in a 1.5-cell S-band RF-gun. The emitted bunches with 5 MeV energy are compressed by velocity bunching where a 4-cell S-band buncher cavity imprints the required energy chirp. By recording the electron diffraction pattern, the target is probed by the ultra-short electron bunches with an atomic spatial and a femtosecond temporal resolution. For pump-probe experiments, the laser system generating electron bunches is also used to excite targets at adjustable time delays. However, the achieved temporal resolution of the pump-probe experiments is defined by the relative timing jitter between the pump-laser pulses and the electron bunches at the target. Since the electron bunch arrival timing strongly varies with the amplitude and phase of the RF cavities, the low level RF controls have to provide phase and amplitude stability below 0.005° and 0.005% respectively, to allow for the sub-10fs pump-probe resolution. The laser to RF synchronization scheme has beed described in [1].

Current LLRF setup at REGAE shares components with the ones designed for Free electron LASer (FLASH) and European X-ray Free Electron Laser (XFEL) in Hamburg [2]. The lower quality factor of normal conducting cavities and therefore higher system bandwidth, demands low latency processing within the digital feedback loop to achieve reasonable gain margins, with respect to super-conducting applications. In addition to signal processing algorithms execution time, the data transfer between the digital chips using Low Latency Links (LLL) adds an important contribution to the overall processing delay. The architecture of the system designed with parallel processing of 100+ RF channels of a multi-cavity cryomodule supplied by one Klystron in mind, introduces additional overhead and extra cost for smaller systems. Nevertheless, a jitter of 55fs has been achieved using feedforward mode only [3]. An optimized platform for systems having one power source and up to 8 RF signals has been proposed.

RF SYSTEM

The Master Oscillator (MO) provides a reference signal of frequency equal to the cavities resonant frequency (3 GHz). This signal is modified in amplitude and phase by the Vector Modulator (VM), amplified by a power amplifier, and drives a high-power klystron. The power of a single klystron is divided by the power divider, such that 75% of the power goes to the RF gun cavity and 25% to the buncher cavity. A remotely controlled waveguide phase shifter is used for setting the phase difference between these two cavities (see figure 2). The RF signals of accelerating cavities, amplifier, and klystron are down-converted to an Intermediate Frequency (IF) by multichannel down-converter module (DWC). The IF signals are analog-to-digital converted by a digitizer module, and controller algorithm running on a FPGA computes the desired modulation signals, closing the signal loop.

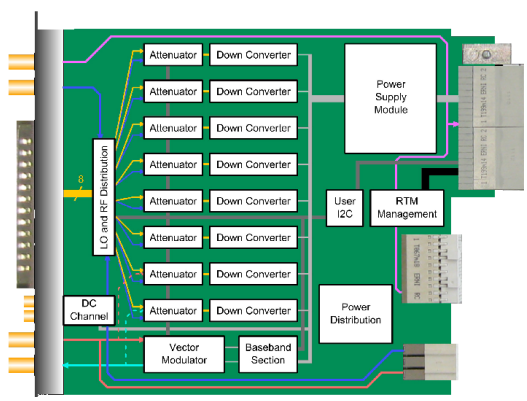

Figure 1: Block diagram of the DRTM-DWC8VM1 board.

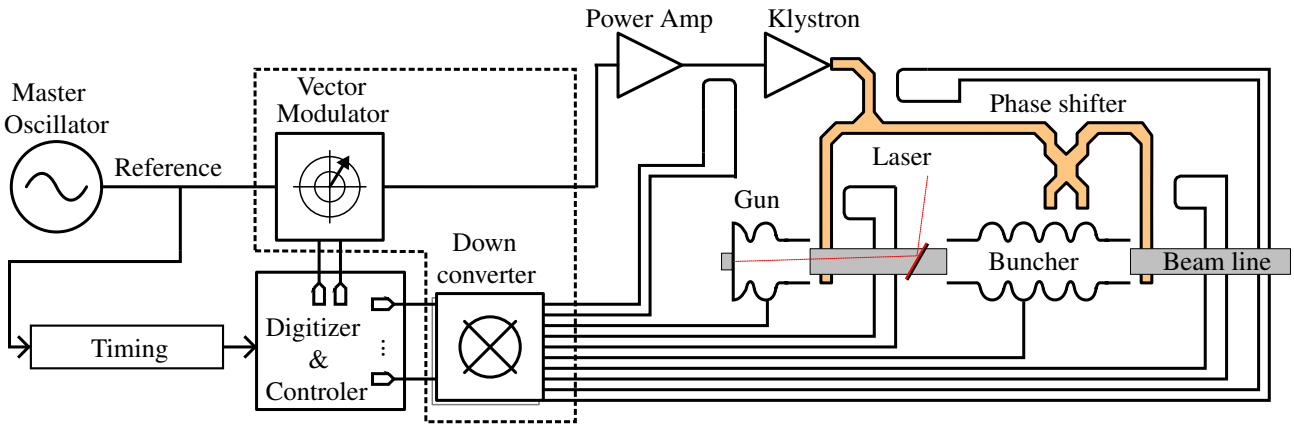

Figure 2: REGAE low level and high power RF systems block diagram

The DRTM-DWC8VM1 is a analog front-end board performing a down- and up-conversion of probe and drive signals, respectively (see figure 1). Input RF signals are detected at an intermediate frequency of 25 MHz, and output signal is a modified (using a microwave IQ modulation chip) reference signal.

The SIS8300L AMC is a FPGA-based (Xilinx Virtex6 series) digitizer / signal generator card. Maximum 10 input channels digitized by ADCs and 2 output signals generated by a dual DAC can be used. Converters and the FPGA are operating synchronously at 125 MHz frequency. Data aquisition and control are performed by an in-crate CPU which communicates with the controller card using a PCI Express bus.

To avoid distortions the timing system delivers trigger signals to the LLRF system near mains 50 Hz signal zero crossing.

CONTROL LOOP

The LLRF control loop can measure up to 10 different RF input signals. In particular, for the REGAE facility there are following input signals:

- RF gun: forward, reflected and probe,
- Buncher cavity: forward, reflected and probe,
- Reference,
- and VM feedback

The level of input signals is conditioned using digital programmable attenuators before down-conversion. Advanced signal processing algorithms are performed by a powerful FPGA on digital signals. The existing architecture of the control loop has been optimized to minimize the overall processing delay in particular for normal conducting cavity applications. Fast internal processing is achieved by lowering the data throughput, shortening pipe-lining length, and increasing the operating frequency of individual blocks. The generated analog output signal drives the modulator circuit. An outline of the control loop is given in figure 3. In the following, the idividual steps of the processing path are described in detail.

Input signal conditioning

Input signals are first provided to an adjustable delay block, which provides temporal alignment in finite steps of 8 ns.

The synchronous sampling allows an implementation of the digital demodulation scheme. The In-phase (I) and Quadrature (Q) components are calculated from IF signals, and IF to sampling frequency ratio of 1/5 improves the measurement linearity.

The magnitudes and the phases of the two output signals are scaled. A special calibration procedure determines scaling coefficients, which reflect physical relations of the signals amplitudes and phases. A drift compensation module similar to the one designed for the XFEL [2] is foreseen to be used in future. I and Q components are filtered using a configurable second order IIR filter.

Matrix

Linear signal processing of multiple signals can be realized in the FPGA using a general purpose computation matrix. Possible applications include

- modification of measurements signals
- signal correction, crosstalk compensation
- preprocessing of individual signals

The matrix has one output signal dedicated for feedback loop, which must be optimized for latency. All the other signals are monitored and acquisited for measurement and analysis purposes. A sparse version of the matrix can be used when hardware resources are insufficient.

The parameter space is limited by the defined digital words' bit width, requiring appropriate input signals conditioning to avoid overflow.

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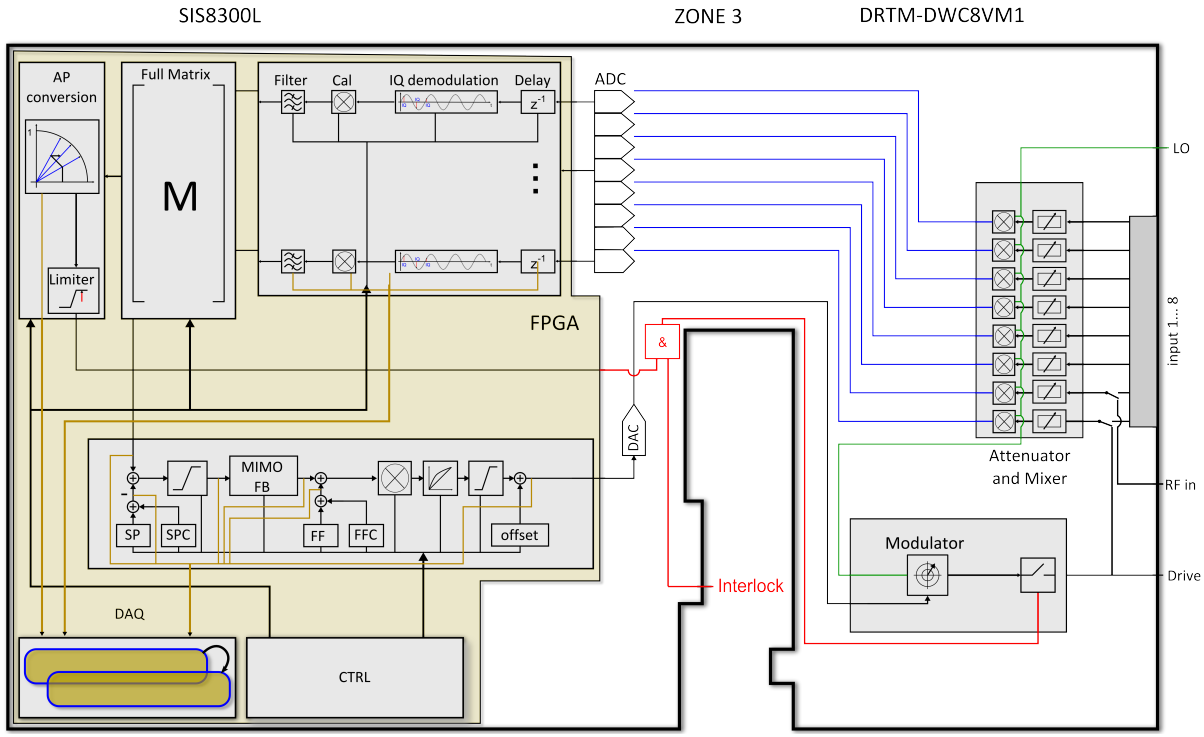

Figure 3: Hardware and firmware block diagram of the LLRF controls

Feedback

Combined buncher cavity and RF gun probes signal processed by the computational matrix is used as an input. The I and Q values are compared with set point table, and error signals are fed to a digital controller. This Multiple Input Multiple Output (MIMO) complex controller processes the error signals and generates correction signals, which are added to the sum of feedforward and feedforward correction tables. Signal is then scaled and rotated to compensate for slow drifts of the system, providing the controller with constant operating conditions. The IQ gain equalization is performed at this stage, improving the linearity of a modulator chip operation. Strong nonlinearity of a klystron is compensated using scaling based on inverted transfer characteristic of the high power RF system. The output signal is limited for reliability and safety reasons, and offset compensation is performed as a last step. Total minimal firmware delay has been estimated to be 500 ns and an additional delay of 150 ns is caused by the converters internal pipelining and buffering.

Interlocks

Accroding to MTCA.4 standard an interlock signal is distributed over an AMC backplane. On the SIS8300L this signal is conjuncted with enable signals from the MMC and the FPGA. When exception condition is met (e.g. a reflected power amplitude limit is hit) the interlock signal send to an RTM module can be asserted, and the output gate opened.

Software

Waveforms gatherd by the controller during RF pulses are sent to the CPU module. The data is initially preprocessed and transmitted to the display and storage servers. The system performance is evaluated and monitored for fault indicators such as reaching drive signals limits or ADCs overflowing. Locally an off-line shot-to-shot analysis is performed by iterative learning control algorithms calculating feedforward correction tables.

From basic operator settings software generates setpoint, feed-forward, and feedback gain tables as well as IIR filter coefficients, feedback parameters and rotation matrices.

OUTLOOK

It is planed to implement the proposed concept, and perform first tests, before the end of 2013.

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