

# A 4 GSA/S INSTABILITY FEEDBACK PROCESSING SYSTEM FOR INTRA-BUNCH INSTABILITIES\*

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## Abstract

We present the architecture and implementation overview of a proof-of-principle digital signal processing system developed to study control of Electron-Cloud and Transverse Mode Coupling Instabilities (TMCI) in the CERN SPS. This system is motivated by intensity increases planned as part of the High Luminosity LHC upgrade. It is based on a reconfigurable processing architecture which samples intra-bunch motion and applies correction signals at a 4GSa/s rate, allowing multiple samples across a single 3.2ns SPS bunch. This initial demonstration system is a rapidly developed prototype consisting of both commercial and custom-designed hardware that implements feedback control on a single bunch. It contains a high speed ADC and DAC, capable of sampling at up to 4GSa/s, with a 16-tap FIR control filter for each bunch sample slice. Other system features include a timing subsystem to synchronize the sampling to the injection and the bunch 1 markers, the capability of generating arbitrary time domain signals to drive the bunch and diagnostic functions including a snapshot memory for ADC data. This paper describes the design, construction and operational experience of this system.

## INTRODUCTION AND MOTIVATION

With the requirements for increased beam luminosity in the LHC, e-cloud and TMCI driven transverse motion of single bunch beam instabilities within the SPS are an area of concern [1]. The existing transverse feedback system within the SPS does not contain sufficient bandwidth to control these intra-bunch instabilities. In order to achieve higher luminosity, a research and development effort is underway to achieve transverse beam stabilization by means of feedback techniques.

To date, this work has involved a modelling effort to help estimate and understand the system dynamics, along with a series of measurements performed at the SPS using a single bunch [2]. An important part of this effort has been the development of an excitation system [3] that allows us to stimulate a bunch with an arbitrary time domain excitation signal in the SPS. The information gained from these measurements [4] was fed back into the simulation model. The next step in the progression of our efforts has been the design, construction and operation of a single-bunch feedback demonstrator system. This system has allowed us to drive a bunch into instability and then stabilize it using feedback.

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## SYSTEM OVERVIEW

The feedback system is part of a larger setup that includes the excitation system. A block diagram of the overall system is shown in figure 1.

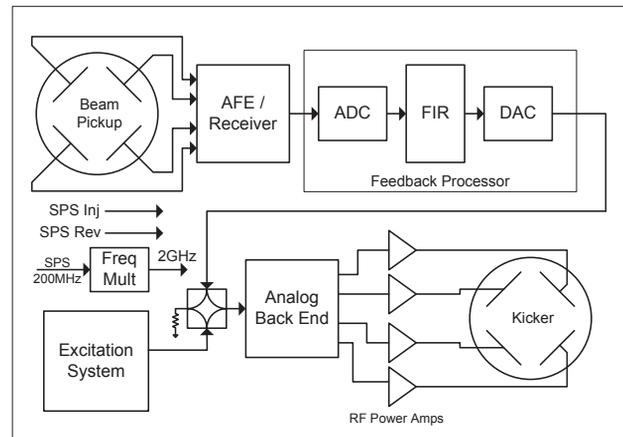


Figure 1: System Block Diagram.

The system consists of an exponentially tapered stripline pickup, an Analog Front End Receiver (AFE), the Feedback Processor channel (containing the data converters and filter), an Analog Back End, which drives four RF power amplifiers, which in turn drive the stripline kicker structure. The processed analog feedback signal is summed via a hybrid with the excitation system output.

## System Timing

The system receives three signals from the SPS Low Level RF and timing system: the 200MHz RF clock, which is input to a frequency multiplier, producing the 2GHz high speed sample clock for the whole system. This clock is effectively doubled by the ADC and DAC to achieve the full sampling rate. The system is designed to run at 4GSa/s, but can be run at any  $n \cdot 200\text{MHz}$  harmonic. For ease of synchronization with the SPS, initial commissioning was done at 3.2GSa/s. The other two signals are the injection marker, signifying the start of an injection cycle into the SPS (periodicity of several seconds) and a bunch 1 or revolution marker (23 $\mu\text{s}$  period), indicating the very first bunch in the train. Both of these signals are used to select the desired bunch and initiate the sampling, processing and correction output operations.

The pickup, feedback output and excitation signals must be properly timed relative to the sampling clock and the beam bunch. The feedback and excitation systems include adjustable timing delays with a 4ns granularity

allowing individual bunches to be selected. A finer resolution delay adjustment is necessary align the signals to within less than one bunch length. To accomplish this, three high bandwidth adjustable analog commercial (Colby Instruments) delay lines are added to the ADC input, the feedback DAC and the excitation outputs. These units have a delay resolution of 10ps per step.

### Analog Front End Receiver

The Analog Front End Receiver takes the four stripline pickup signals and produces a signal representing the vertical displacement of the beam. It sums the upper and lower pickup plate pairs using RF combiners and passes these summed pairs to a hybrid which produces a delta signal of the pairs. The delta signal is then passed into a processing chain containing an equalizer [5], which compensates for amplitude and phase distortions introduced by the pickup and cabling. The equalized signal is then passed to a wideband RF amplifier and then onto an 800MHz low-pass Bessel anti-aliasing filter before input to the ADC.

### Analog Back End

The Analog Back End receives the combined DAC output signals from the hybrid and drives the high power stripline kicker structure. It consists of a preamp which drives a hybrid, producing in-phase and  $\pi$  outputs which drive the opposite pairs of plates in the kicker. The hybrid outputs are split using 1:2 RF power dividers, which drive four 80W, 0.02 to 1GHz RF power amplifiers. It should be noted that the bandwidth of the existing kicker is about 200MHz and limits our ability to control modes higher than order 0 and 1. A new kicker is being designed to overcome this limitation [6].

## THE FEEDBACK PROCESSOR

The feedback processor is architected as a general-purpose, reconfigurable signal processing channel with an ADC, processing element (implemented in an FPGA) and a DAC. The vertical displacement signal from the AFE is digitized by two Maxim Semi MAX109, 8-bit 2GSa/s ADCs. These operate in interleaved mode giving an effective sampling rate of 4GSa/s. The sampling process produces 16 samples, or slices across the bunch.

The samples are passed into the FPGA, which performs all of the data processing. The samples are de-interleaved and mapped to a bank of 16, 16-tap FIR filters. There is one filter per slice. The FIR filters follow the relation:

$$y(n) = \sum_{k=0}^{15} h(k)x(n-k)$$

With the coefficient  $h(k)$  multiplied by the  $(n-k)^{\text{th}}$  sample and summed. There are two loadable coefficient sets (swappable in real time) of 8-bit filter coefficients, with the selected set applied to all 16 filters simultaneously. The FIR produces a 20-bit result, which must be scaled to fit the 8-bit DAC sample window. This is accomplished

with a programmable shift gain block, which also detects and notifies saturation conditions.

The gain-shifted FIR data is then passed into the DAC output logic block which arranges the data into four, 1GSa/s 8-bit streams for input to the DAC. The DAC, a Maxim Semi MAX19693, is a 12-bit device being used in 8-bit mode. This device uses both edges of the 2GSa/s sample clock to produce a 4GSa/s output. Besides feedback, the DAC can run in excitation mode, where a memory is loaded with arbitrary patterns and played out.

The raw, pre-filtered ADC data can be selectively captured in a special snapshot memory and read out for analysis. The system also contains general-purpose digital and analog I/O for support of ancillary functions. Communication is via a USB 2.0 interface.

All system dataflow, timing and sequencing of operations is handled by a set of state machines, synchronized to the RF clock and sequenced by the injection and bunch crossing markers. The processing dataflow pipeline operates in a bursty manner, with short periods of high dataflow and processing (initiated by the bunch 1 marker) separated by quiescent periods before the correction signal is sent out, at the next bunch 0 marker. All data processing happens on edges of the RF clock.

### Implementation

The design implementation is modular and based around a commercial FPGA motherboard (Dini Group DNMEG\_V6HXT), containing a Xilinx XC6VHX565T, Virtex-6 FPGA. This board was chosen because it contains two high-speed, high-density connectors, facilitating the connection of daughterboards. All FPGA code is written in VHDL.

The DAC subsystem is implemented on a custom designed daughterboard. In addition to the DAC, this board also contains clocking circuitry, the input trigger circuitry, the general-purpose digital and analog I/O circuitry and the USB interface.

The ADC subsystem, originally intended to be a custom daughterboard, was instead (due to resource limitations) implemented with two Maxim Semi MAX109EVM ADC evaluation boards. These were used in conjunction with a custom designed high-speed cable assembly that mates with the motherboard connector. This cable assembly was developed in collaboration with Samtec Corporation and contains 78 pairs of length matched 100 ohm differential micro-coax cable.

The entire feedback processor system is packaged in a 19-inch rackmount chassis. In addition to the boards described above, the chassis also contains the ADC input board, which splits the ADC signal into two and adds a delay equal to one 4GHz clock tick (for interleaving) to one of the signal legs. In addition, it houses the sample clock RF Amplifier and splitter, and a switch-mode power converter for supplying DC power. All signal I/O is via the front panel which also contains system status and power indicator LEDs.

## System Software

The system control and data transfer software is GUI based and developed in Microsoft Visual Basic 2010. The GUIs interface with the system over USB using driver calls. A suite of Matlab-based applications have been developed to facilitate configuration of the feedback mode, generation of excitation data files, design of the FIR filters, and analysis and display of the ADC snapshot data. Transfer between Visual Basic and Matlab is done using text based configuration and data files, generated automatically by the SW.

## OPERATIONAL EXPERIENCE

The system was designed and assembled in less than a year and shipped to CERN in Nov-2012. It was used in SPS Machine Development measurements between Nov-2012 and Feb-2013. A large amount of data was collected and is currently being analyzed. Preliminary results indicate that we were successfully able to control mode 0 instabilities with feedback in the SPS [7]. Higher order modes were observed as well. Figure 2 shows the effect of an unstable beam. The feedback is increasing the drive signal based on the motion in the beam. The left plot shows a Gaussian bunch signal over 40 turns from the ADC snapshot memory. The right plot shows processed output correction signal over 40 turns from the DAC. The gain between input and output is visible. Both plots are over the full 16 sample slices.

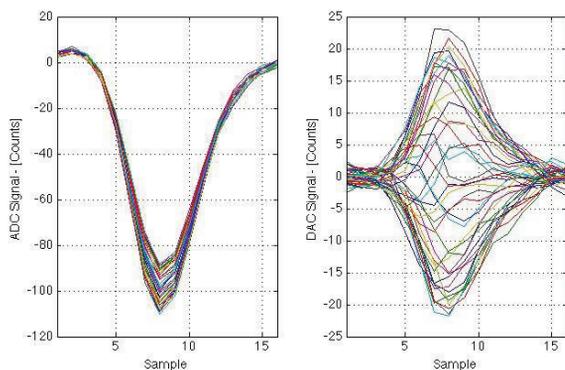


Figure 2: Feedback system input and output signals.

Characterization of the ADC and DAC performance are very close to datasheet specifications. An FFT of the ADC with a single tone (bypassing the AFE) at 400MHz produces a Spurious Free Dynamic Range (SFDR) value of 60dB, which is in near agreement with the 61dB datasheet value. Other FFTs of the snapshot ADC data show a frequency line that is believed to be an artefact of the switching power converter. A recognized limitation is that the ADC limits the vertical beam orbit offset in the pickup area to  $\pm 1.2\text{mm}$ , for a bunch with  $1.1\text{E}11$  protons and a length of  $3.2\text{ns}$  (4 sigma).

## SUMMARY AND FUTURE DIRECTION

The system has performed in its capacity as a proof-of-principle demonstrator. A wealth of data has been collected from the SPS and is being analyzed. Preliminary results indicate feedback control of mode 0 instabilities. During the CERN long shutdown, we plan on adding improvements and enhancements to this demonstrator system. These include: processing and control of multiple bunches, an orbit offset removal mechanism, individually (per filter basis) settable FIR coefficients, the inclusion of cross-terms from adjacent filters and an Ethernet interface.

This platform provides a very high speed re-configurable signal processing platform that could serve other accelerator applications. It should be noted that this demonstrator system is a proof-of-concept and is not the final solution. With the techniques developed and information learned from it, it provides a path towards a final solution for the SPS, with possible expansion to the PS and LHC.

## ACKNOWLEDGMENTS

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