Karlsruher Institut für Technologie

Ultra-Ultra-Fast Data Acquisition System for *Coherent Synchrotron Radiation* Based on Superconducting Terahertz Detectors

4th International Particle Accelerator Conference, 12-17 May 2013. Shanghai

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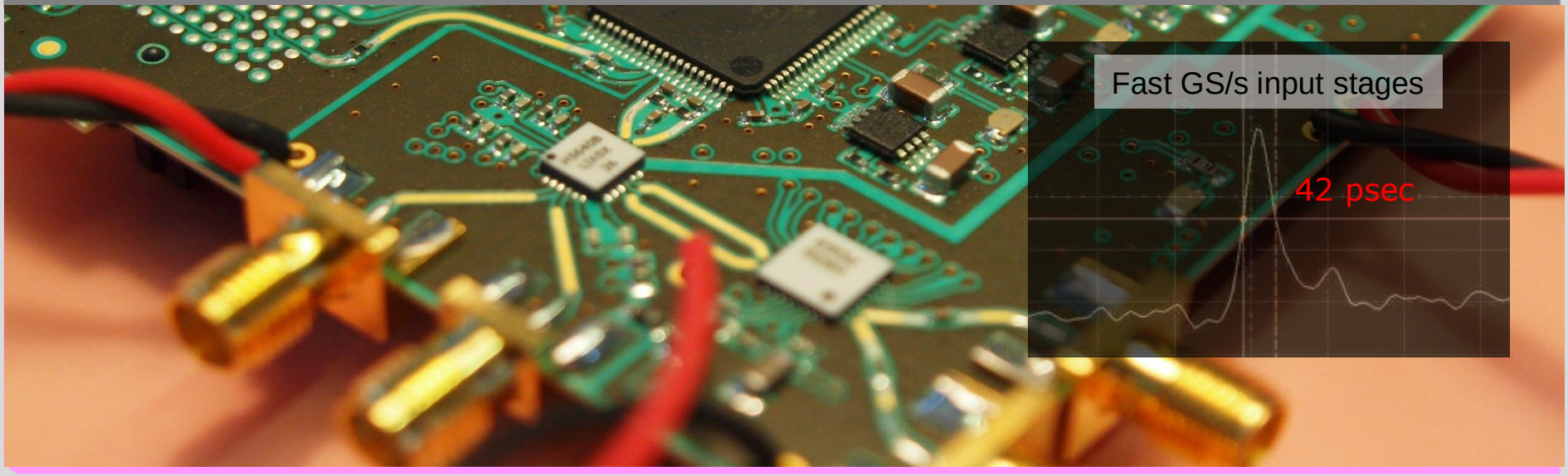
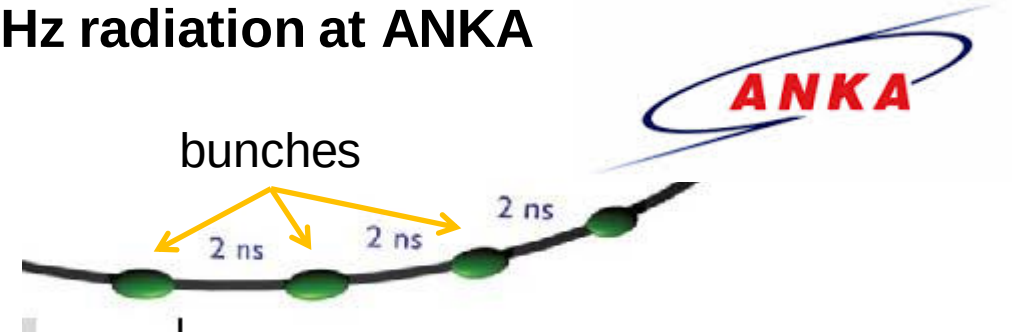
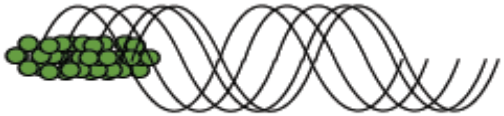
KIT, Institut für Prozessdatenverarbeitung und Elektronik
M. Caselle



THz radiation at ANKA



Normal mode



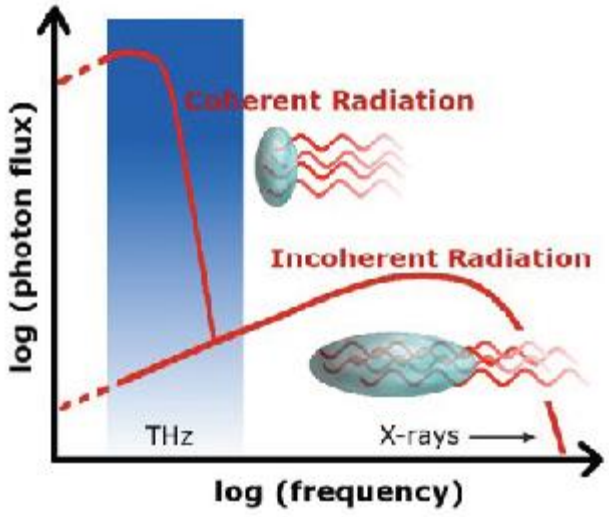
X-ray incoherent radiation

Low alpha mode

THz coherent synchrotron radiation (CSR)

ANKA parameters:

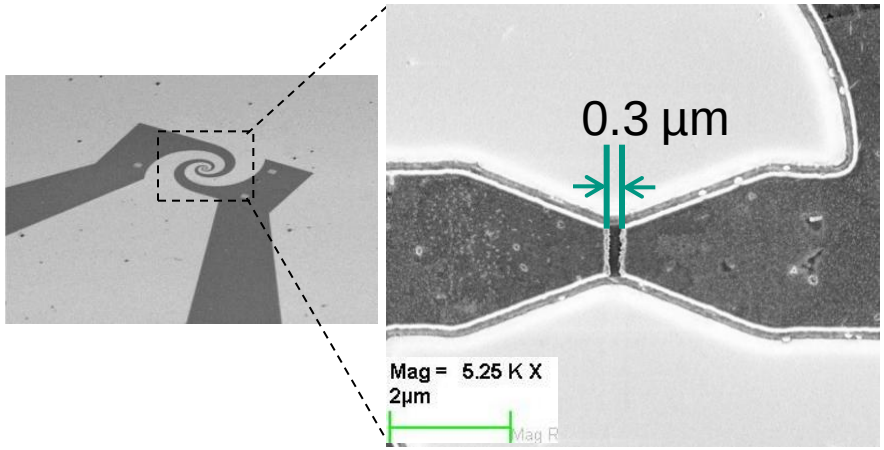
- Circumference: **110.4 m**
- RF-system: **500 MHz**
- Revolution time: **368 ns**
- Harmonic number: **184**
- Revolution frequency: **2.71MHz**
- Beam energy: **2.5 GeV**
  - low alpha mode: **1.3GeV**
- Bunch length (low alpha mode): few **ps**
- Bunch spacing: **2ns**



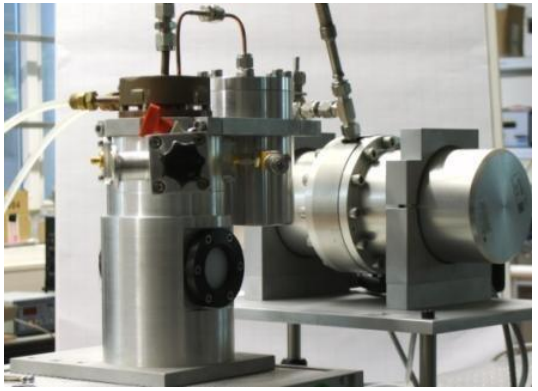
Reference:
***A.-S. Müller, et al*. MOPEA019, these proceedings**

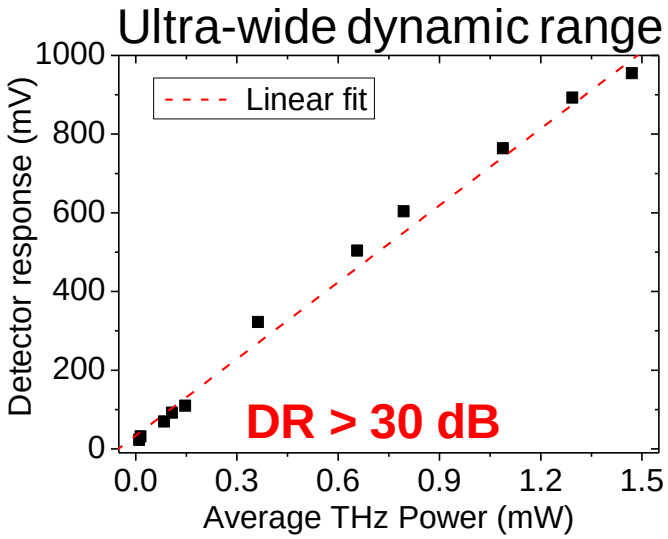
A.-S. Müller, et al. Observation of Coherent THz Radiation from the ANKA and MLS Storage Rings with a Hot Electron Bolometer. (TU5RFP027), 2009. 23rd Particle Accelerator Conference PAC09 Vancouver, Canada.

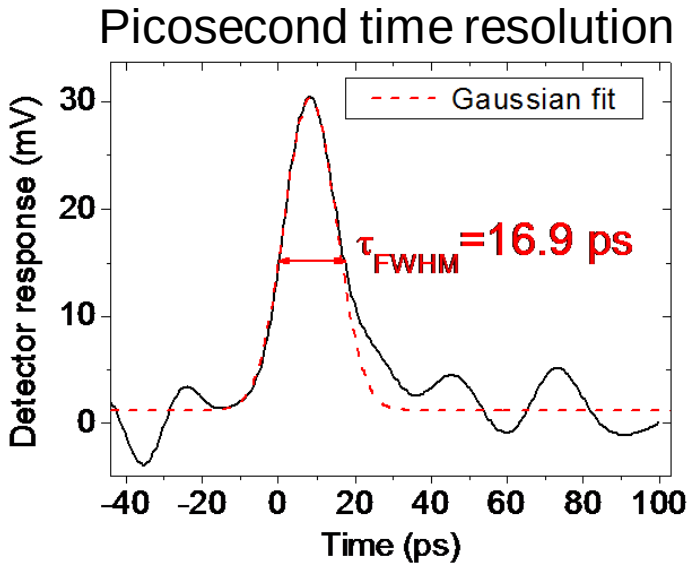
Ultra-fast YBCO THz detectors for picosecond synchrotron pulses



Nanometer-sized YBCO detectors in a high-speed readout system **operated > 77 K**

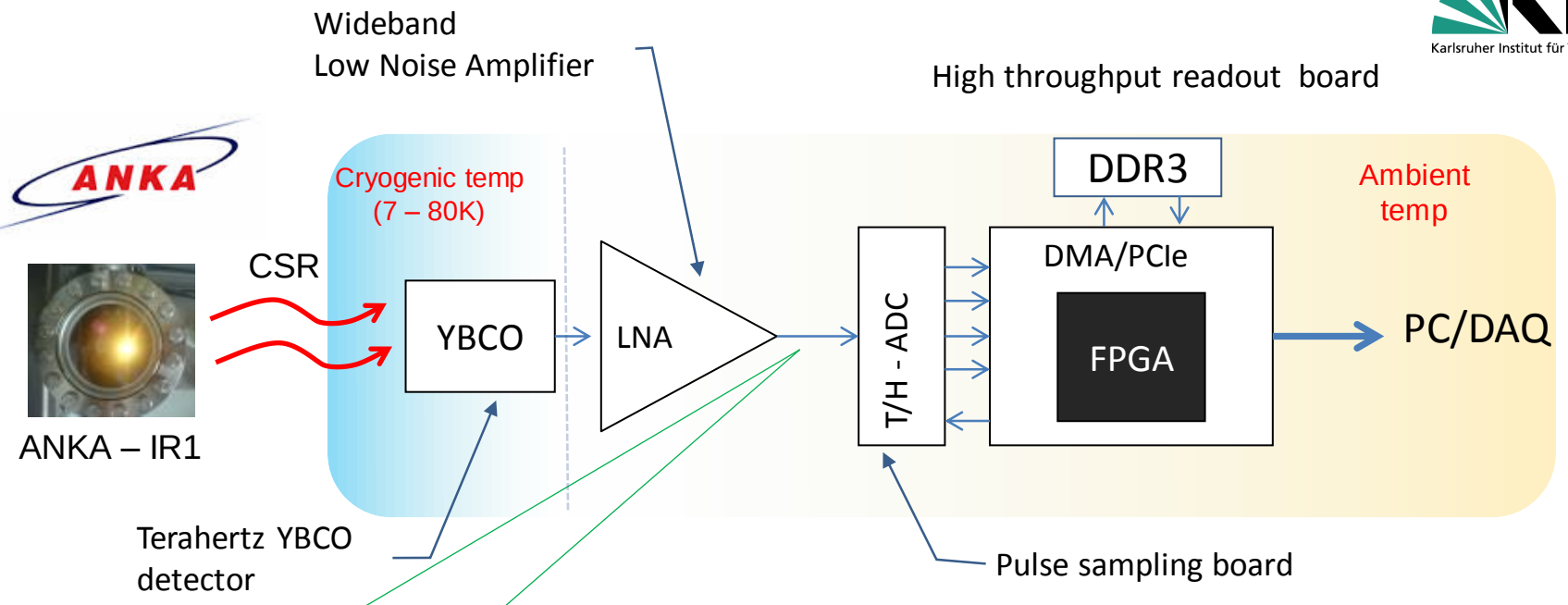


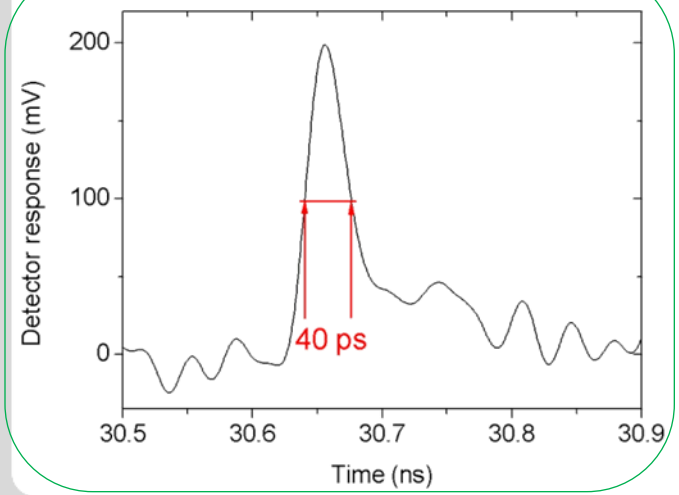




P. Thoma et al., *Applied Physics Letters*, 101, 142601, 2012
P. Probst et al., *Physical Review B*, 85, 174511, 2012

CSR - THz experimental setup





Detector system based on a superconducting NbN/YBCO ultra-fast bolometer with a bandwidth up to 1 THz.

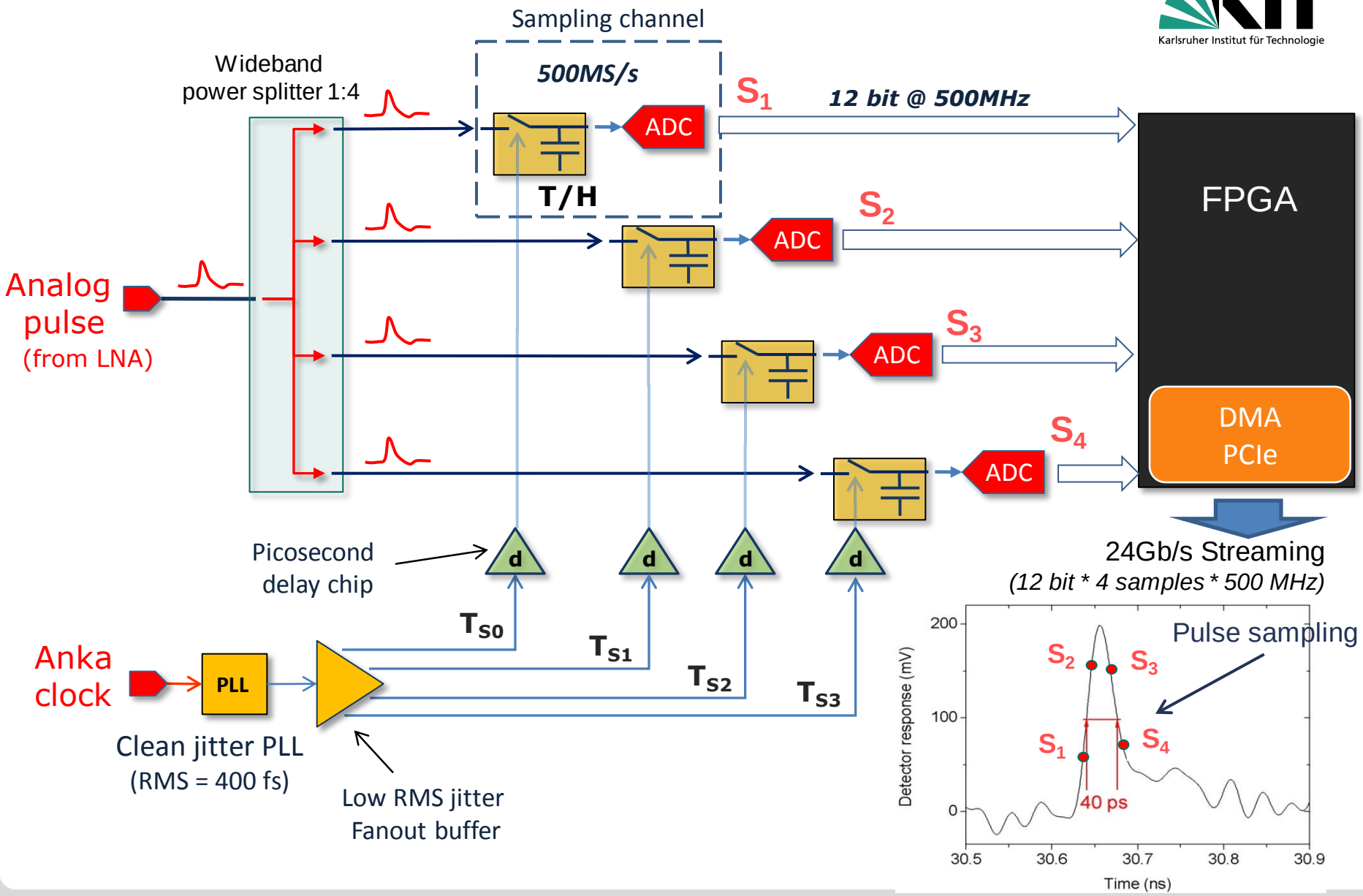
P. Probst. APPLIED PHYSICS LETTERS 98, 043504 (2011)

Pulse width (output of LNA)→ few tens of picoseconds

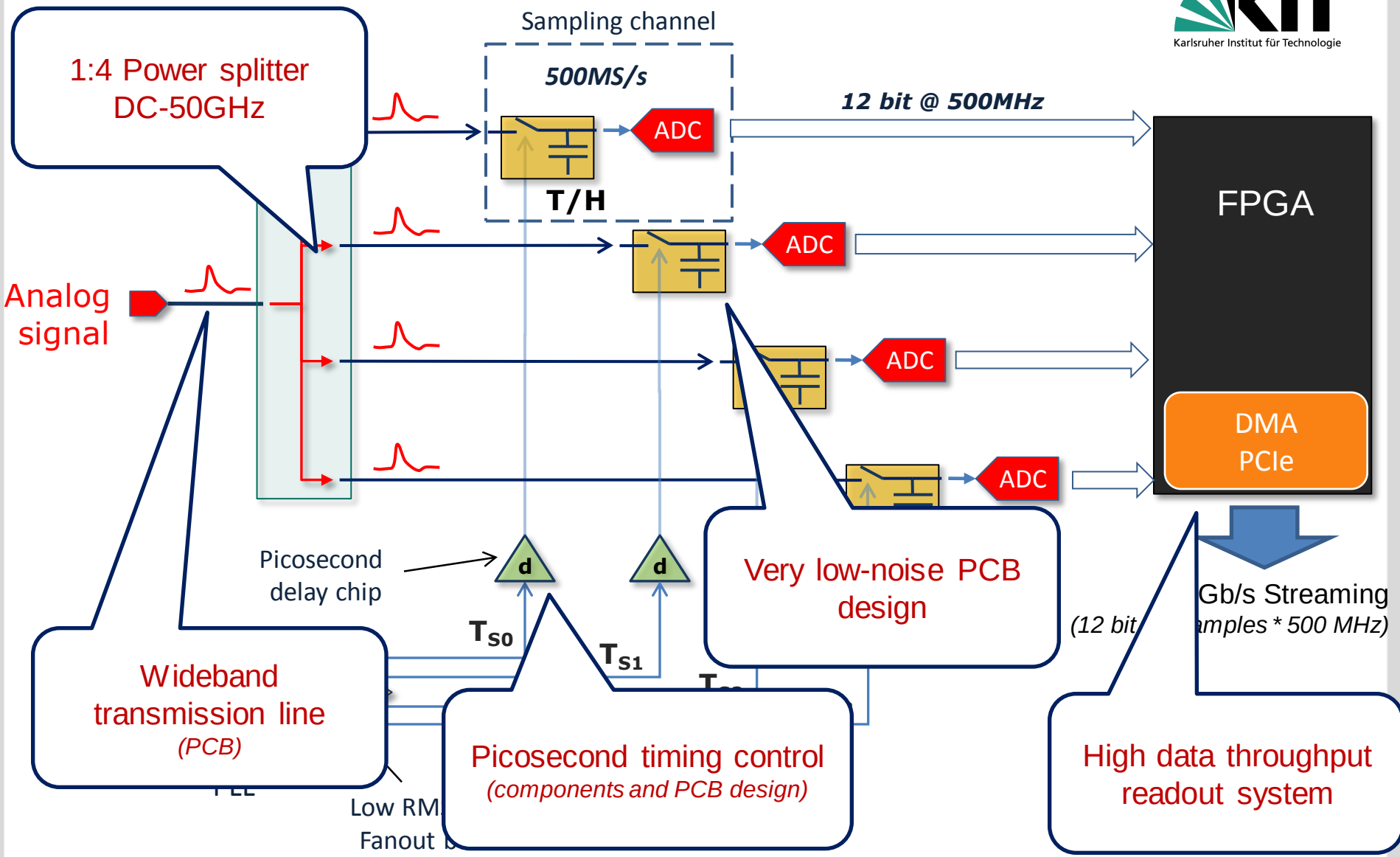
Incoming pulse frequency of 500MHz synchronous with ANKA RF system (resp. CSR bunch emission)

***GOAL:** Turn-by-Turn and Bunch-by-Bunch measurement of CSR intensity.*

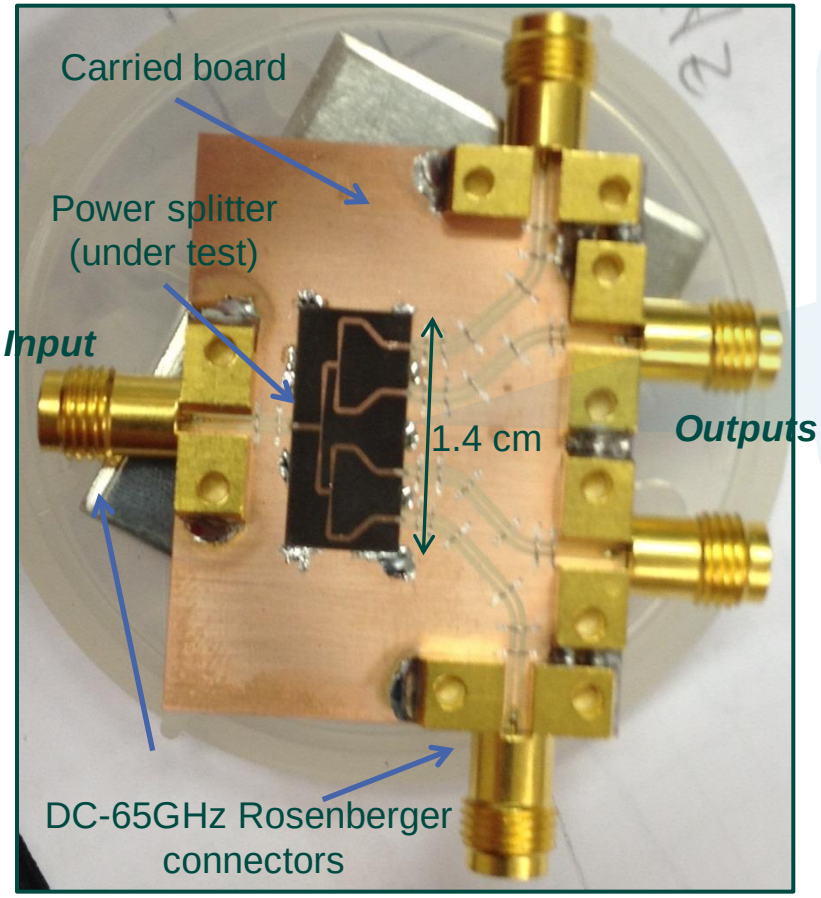
Fast pulse sampling board *(basic concept)*



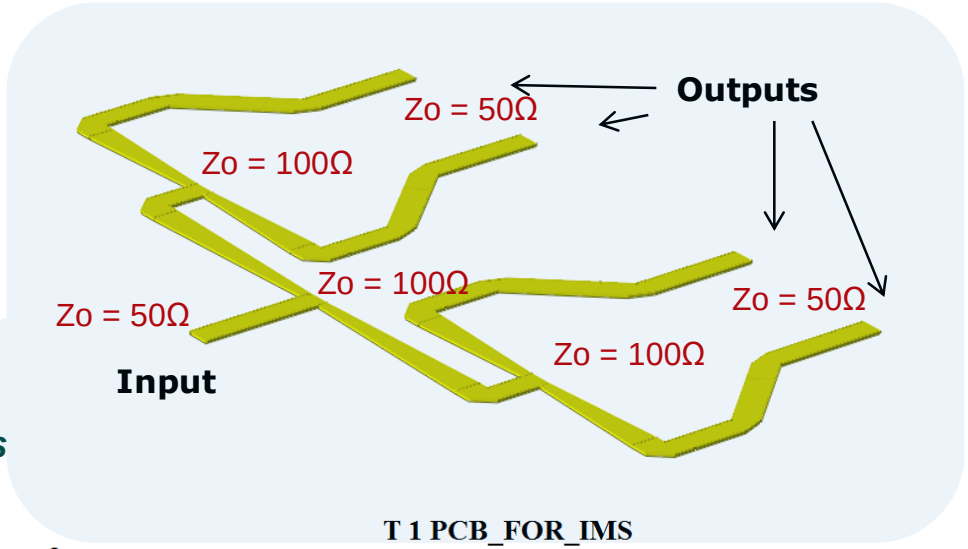
Fast pulse sampling board *(basic concept)*

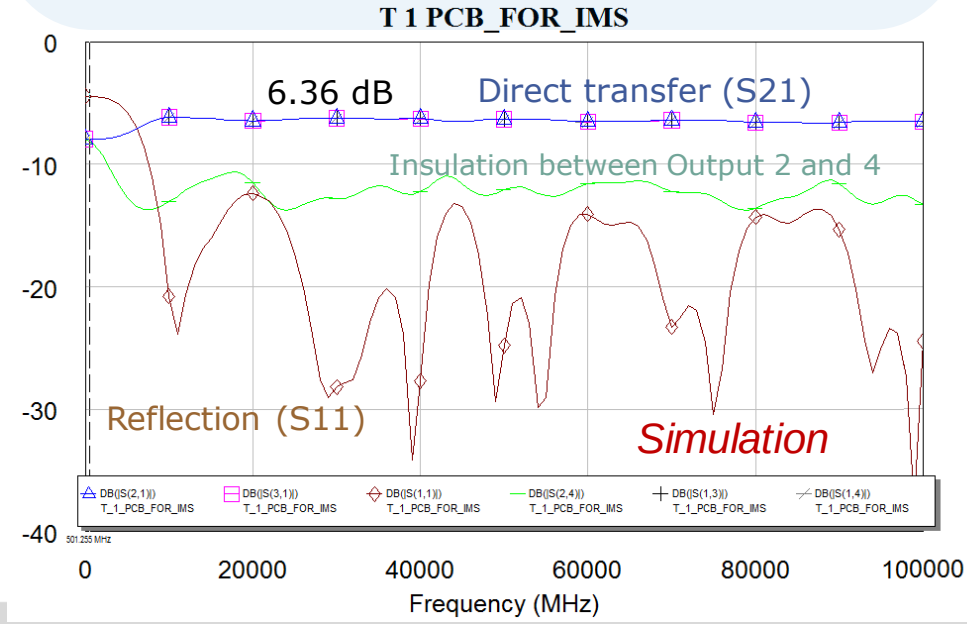


Power splitter DC - 50 GHz, PCB layout



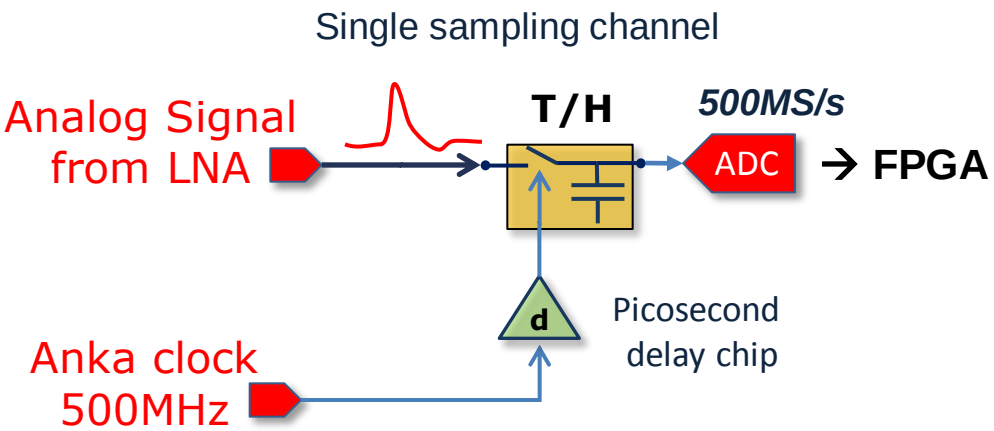
Substrate: Duroid5880

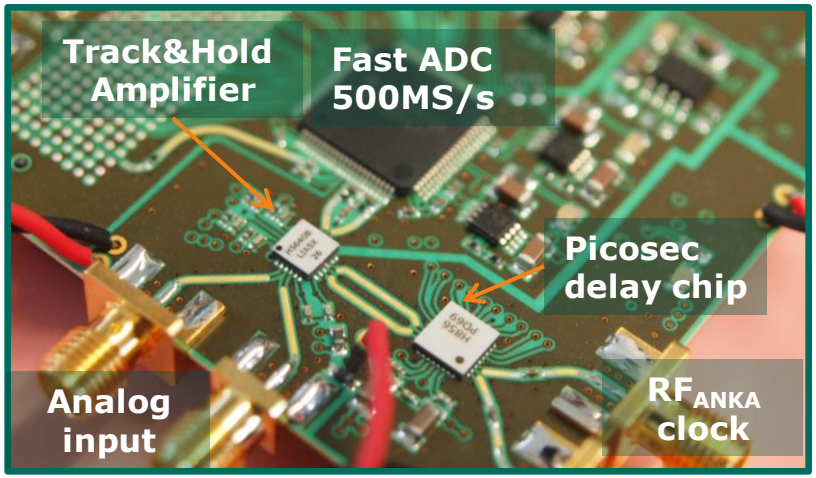




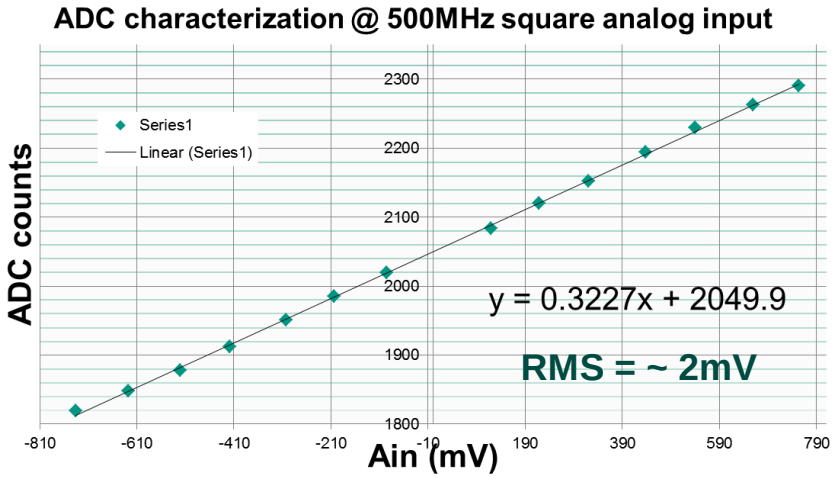
Fast sampling prototype board

Acquires one sample in the peaking time region of each THz pulse (resp. CSR bunch emission).

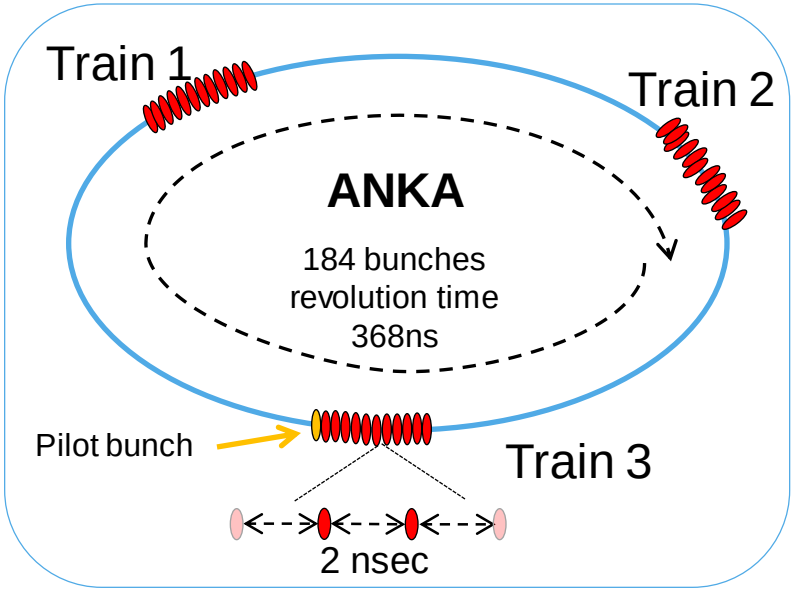




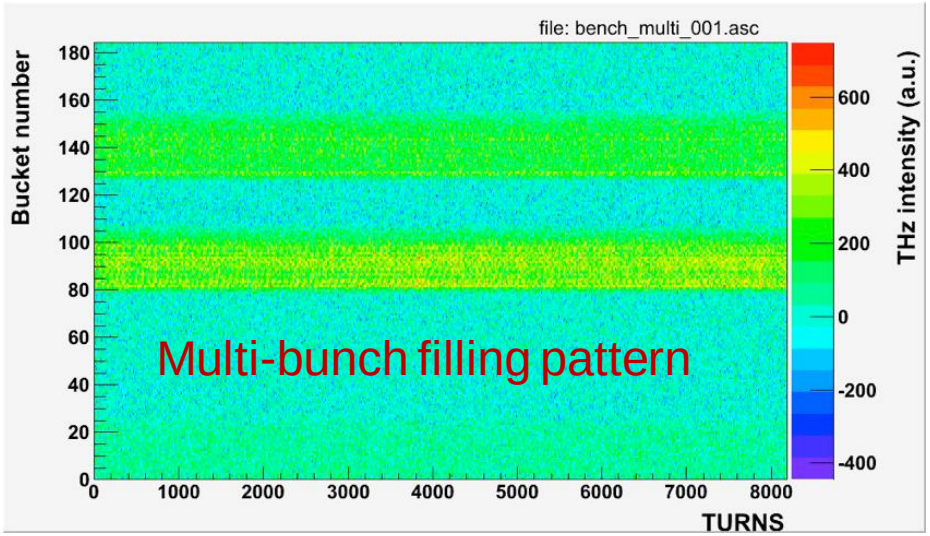
- ✓ *PCB → Roger 4003 substrate and high-speed CPW transmission lines (BW: 50GHz)*
- ✓ *Separation between Analog and digital GNDs*
- ✓ *Ad-hoc RF-filters on critical components*
- ✓ *Vias fences and guard-ring layout techniques*
- ✓ *Low RMS time jitter → components selected*



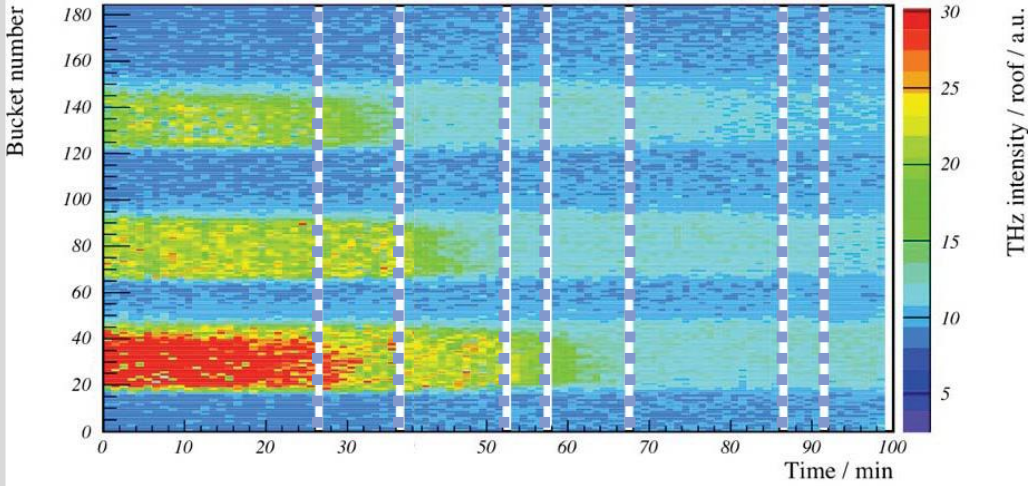
Sampling prototype board ANKA Test Beam



ANKA CSR (with NbN HEB detector)



ANKA CSR (long observation time with YBCO detector)

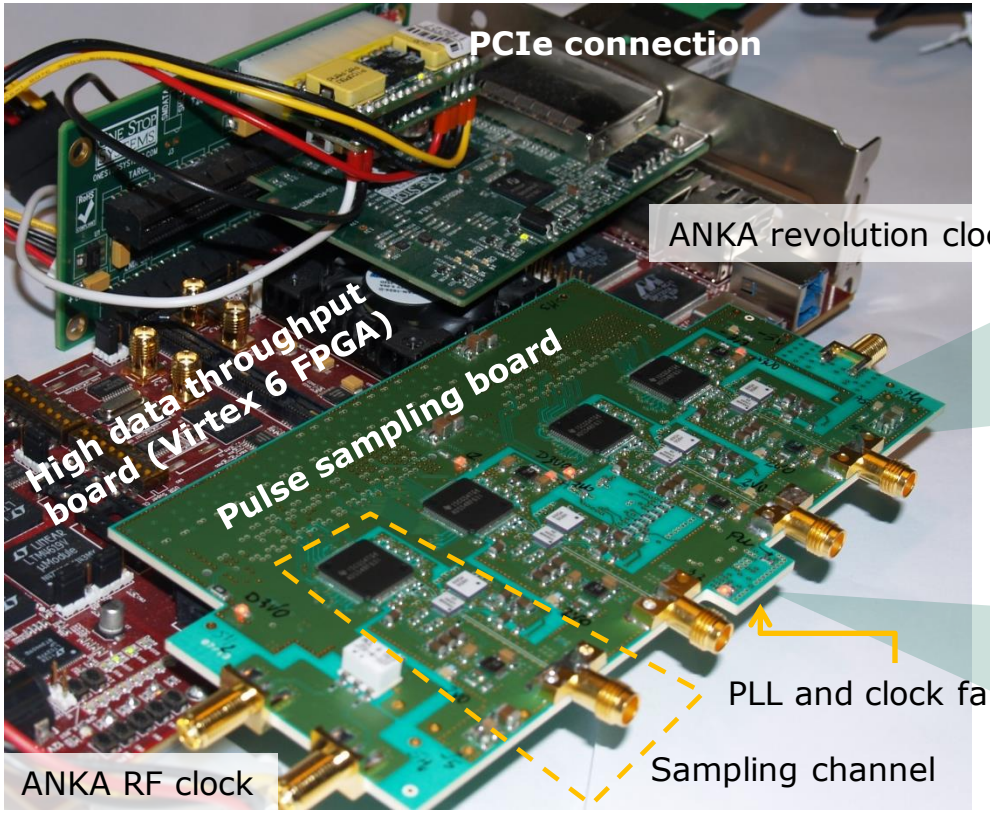


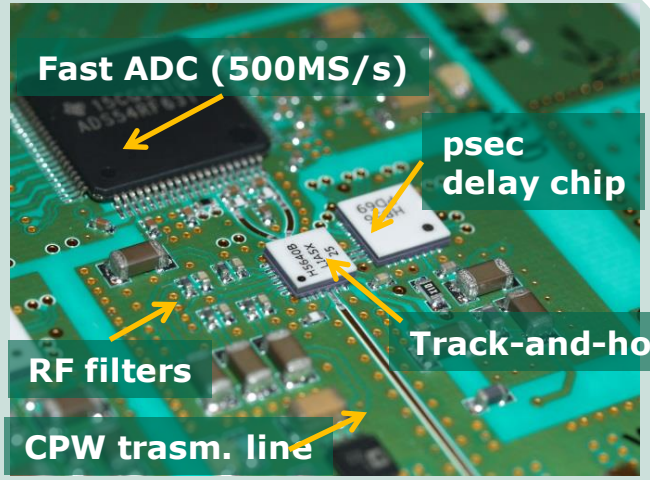
Recording & analysis of time evolution of each bunch

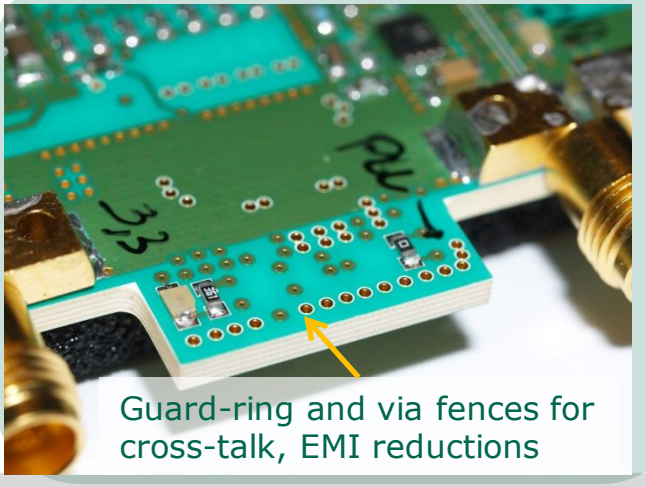
- ✓ Tested with YBCO and NbN THz detectors
- ✓ Simultaneous turn by turn monitoring of all 184 buckets
- ✓ Continuous data stream (all bunches all turns) without dead time
- ✓ Measurements of CSR oscillation amplitude
- ✓ ***A.-S. Müller, et al. MOPEA019, these proceedings***

Four sampling channels board

4 sampling channels board has been produced → recently electrically tested







PCB made by ROGER 4003 consisting in 10 layers metal Stack-up

Conclusion and what's next

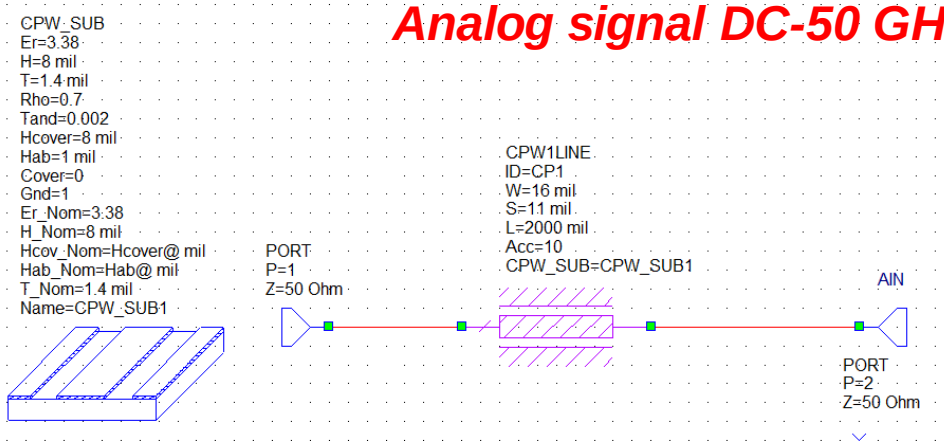
- ✓ Fast sampling prototype board → dynamical range of ± 800mV with RMS = 2 mV
- ✓ Very low Deterministic jitter → sampling time accuracy of 3 ps
- ✓ The Random jitter estimated to be < 500 fs
- ✓ High data throughput readout board based on PCIe-DMA (16Gb/s)→ already available and used for beam studies
- ✓ Four sampling channels board → developed and produced

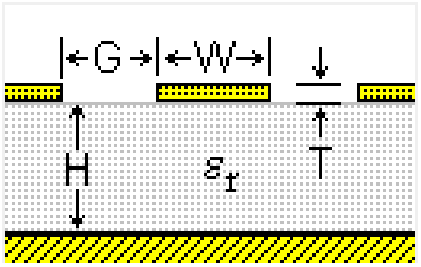
- ➢ First test beam test → foreseen in the summer
- ➢ High data throughput readout board based on PCIe-DMA (32Gb/s)→ under developing

Thank you for your attention ….

High-band CPW transmission line

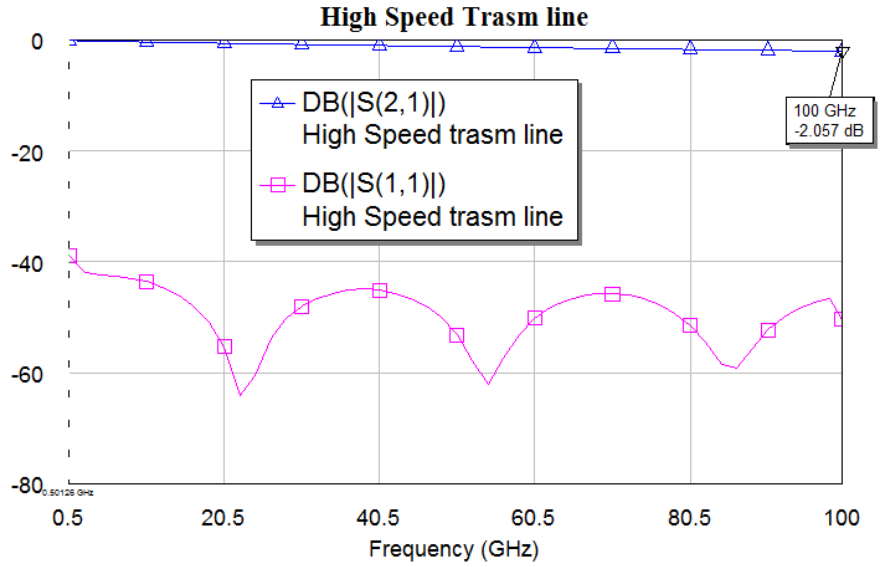
Analog signal DC-50 GHz

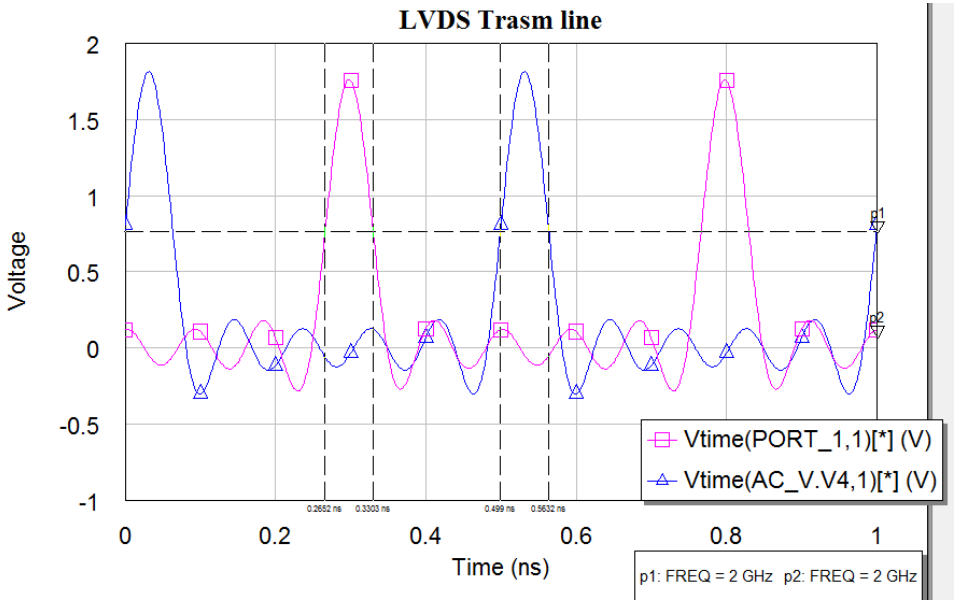




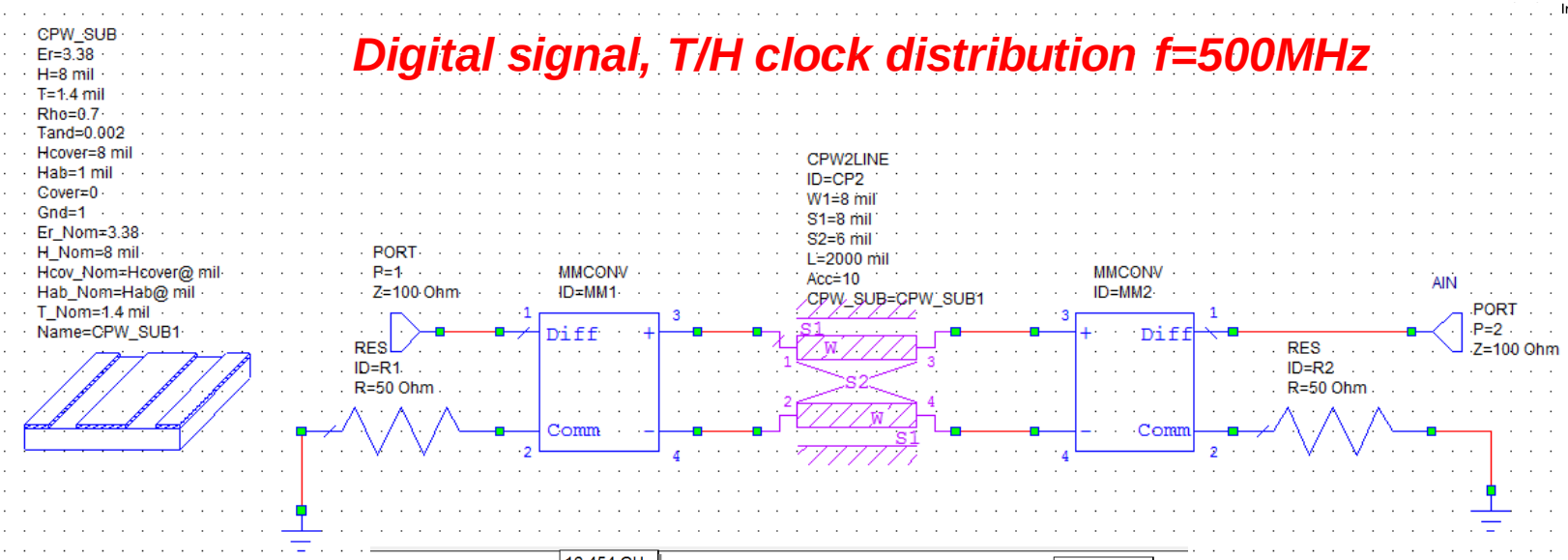
Loss= 38dB/m

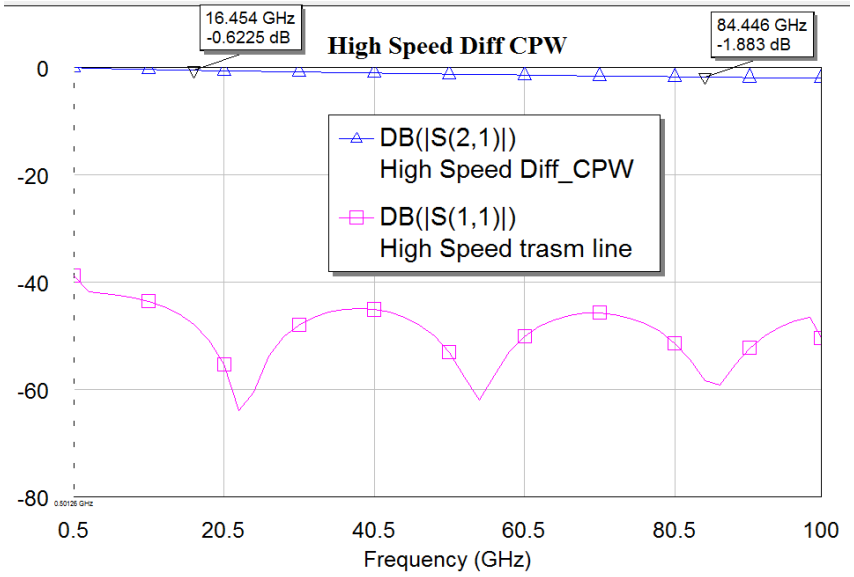
Z0 = 50.7 Ω





Differential CPW transmission line





Differential Stripline (TL)

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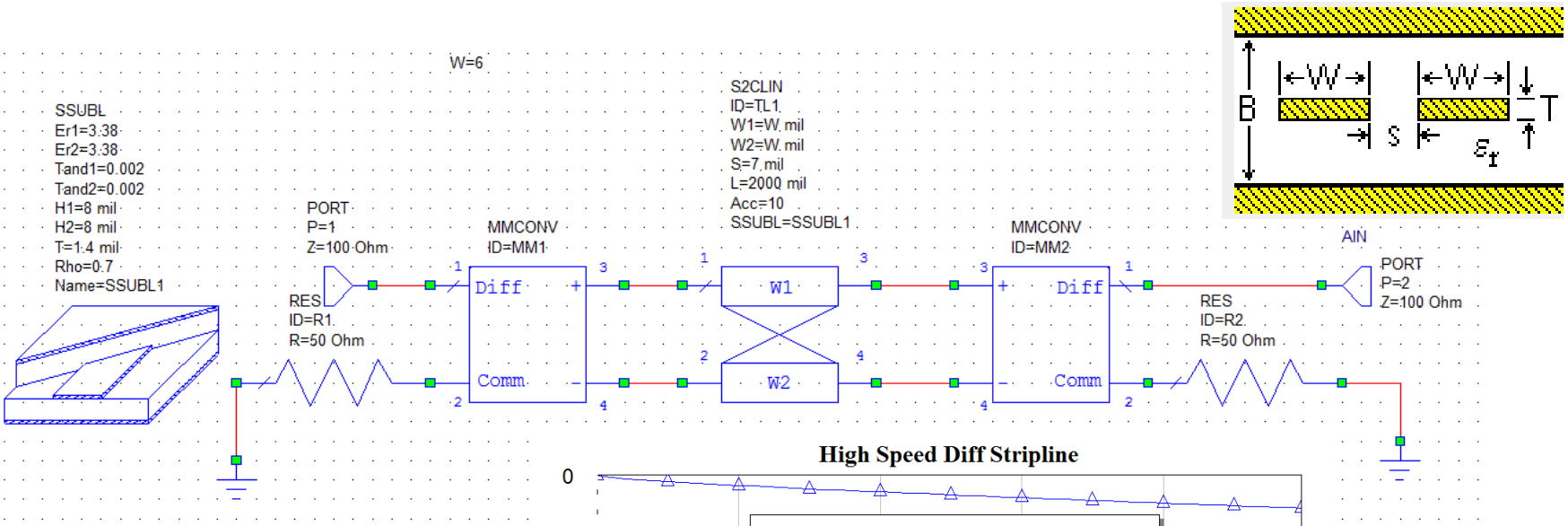
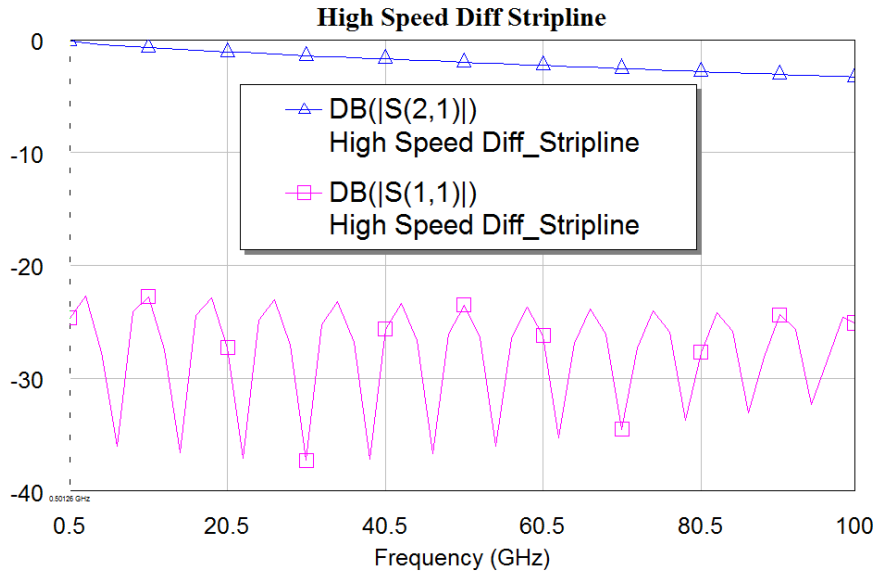
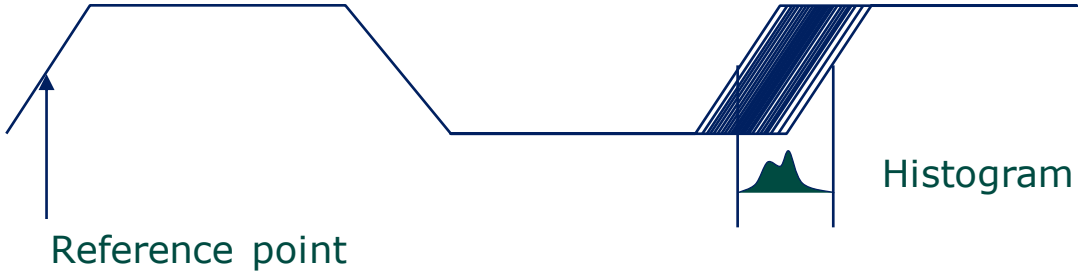
Digital signal, ADC clock distribution f=500MHz





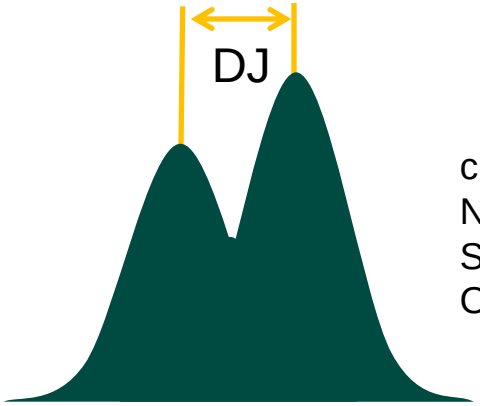
Time and voltage jitters in high speed sampling board

Jitter: *The deviation from the ideal timing of an event.*



Jitter is composed of: both deterministic and Gaussian (random) content.

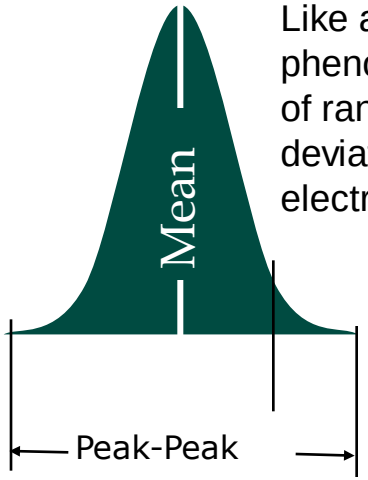
Deterministic jitter (DJ)



cross talk, EMI radiation, Noisy reference plane, Simultaneous Switching Outputs (SSO), etc.

Jitter with non-Gaussian probability density function

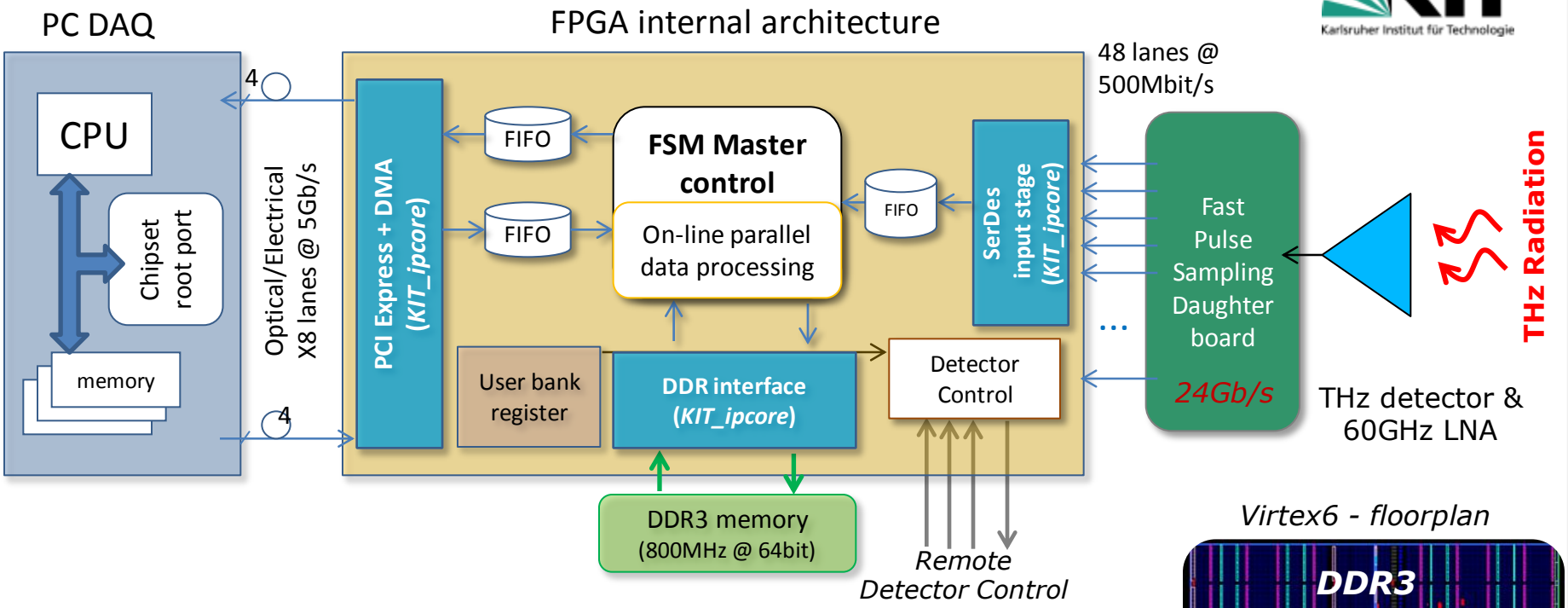
Random (Gaussian) Jitter (RJ)



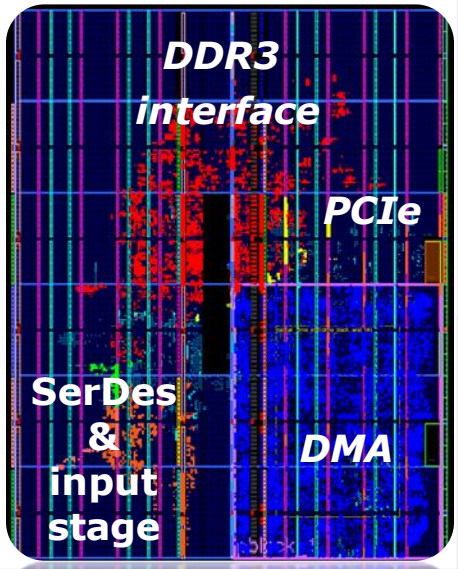
Like all physical phenomena, some level of randomness to edge deviation occurs in all electronic signals.

Standard Deviation (1s)

High-throughput readout system & FPGA architecture

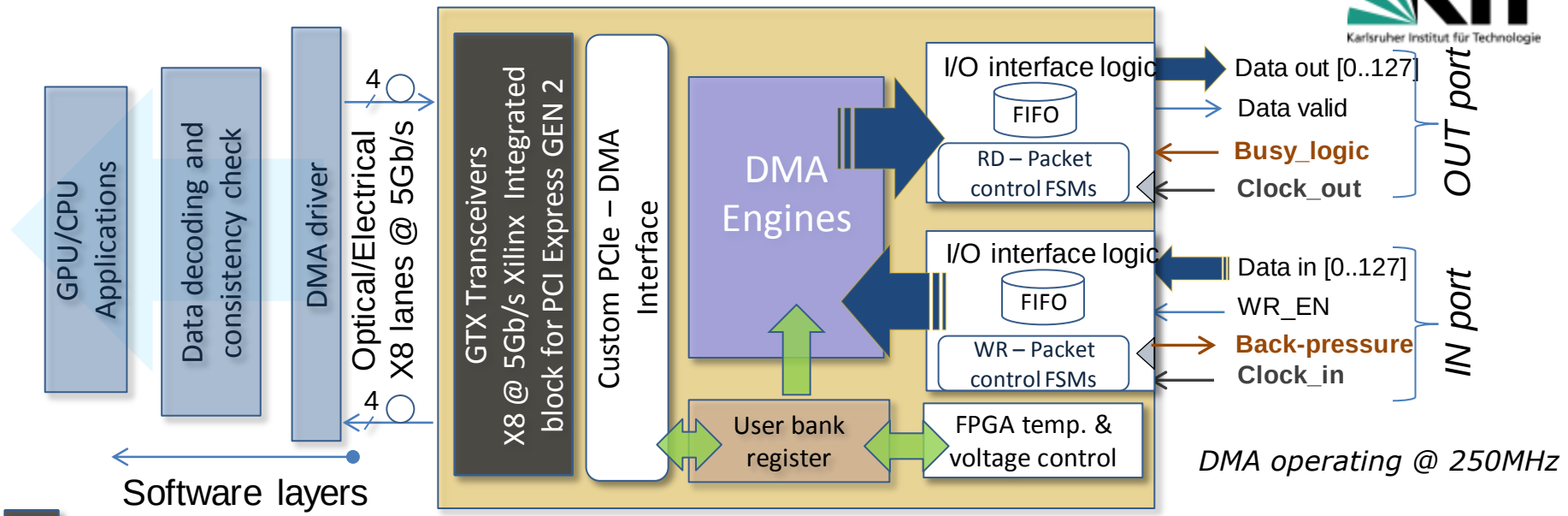


Virtex6 - floorplan



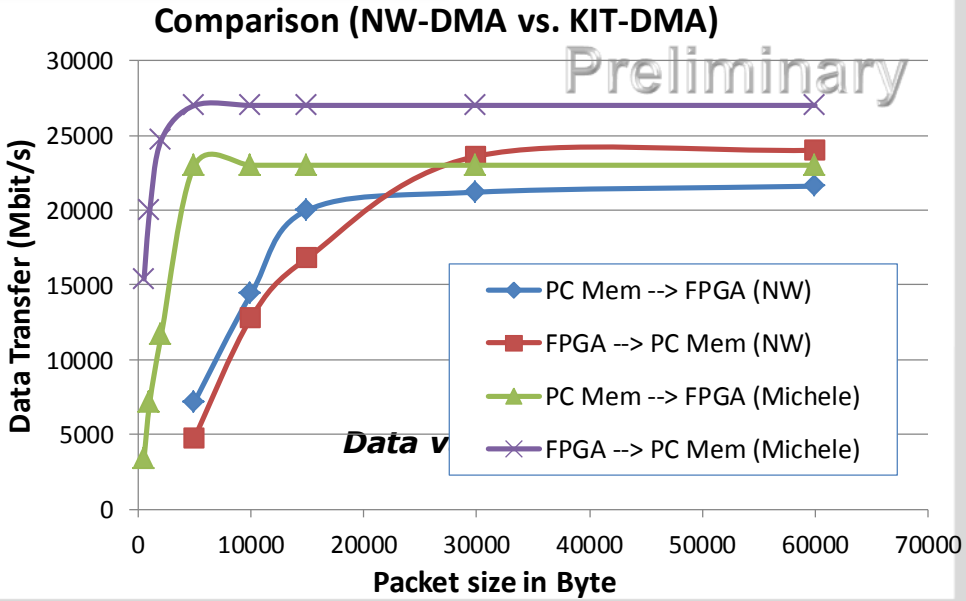
- ✓ PCIe-Bus Master DMA readout architecture operating with 8 lanes PCIe @ Gen2 (250MHz)
- ✓ Multi-port high speed DDR3 interface @ 51Gb/s
- ✓ PCI Express/DMA Linux 32-64 bits driver
- ✓ Integration in the parallel GPU framework

PCIe-Bus Master DMA readout architecture



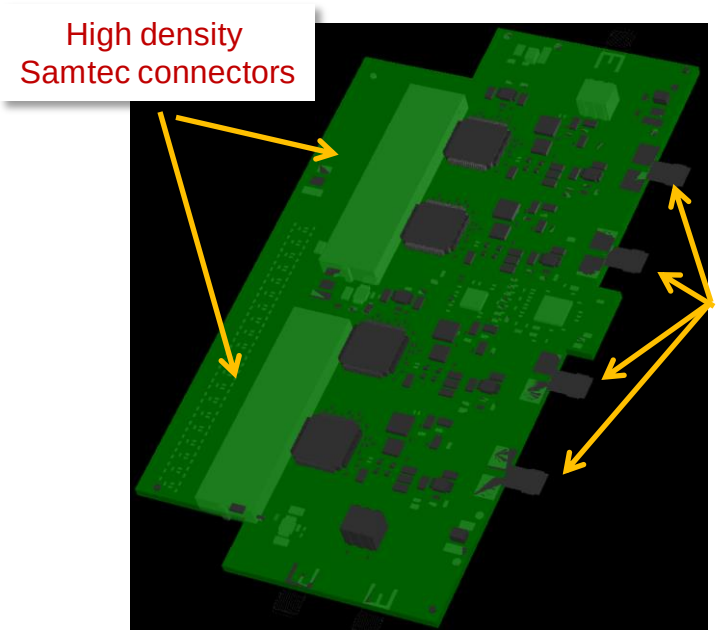
DMA operating @ 250MHz

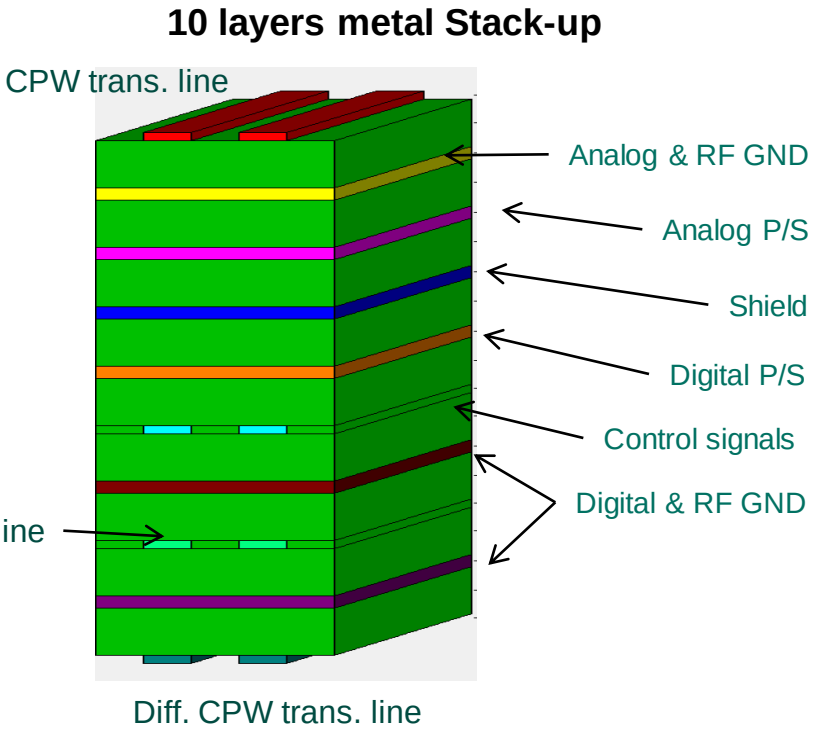
- ✓ Bus Master DMA operating with 8lanes PCIe @ Gen2 (250MHz)
- ✓ Two individual engines for write/read from FPGA (User logic) to PC centre memory
- ✓ IN and OUT FIFO-like interface (for User logic)
- ✓ FIFO used to decouple the time domain between DMA and User custom logic



Conclusion & What's next

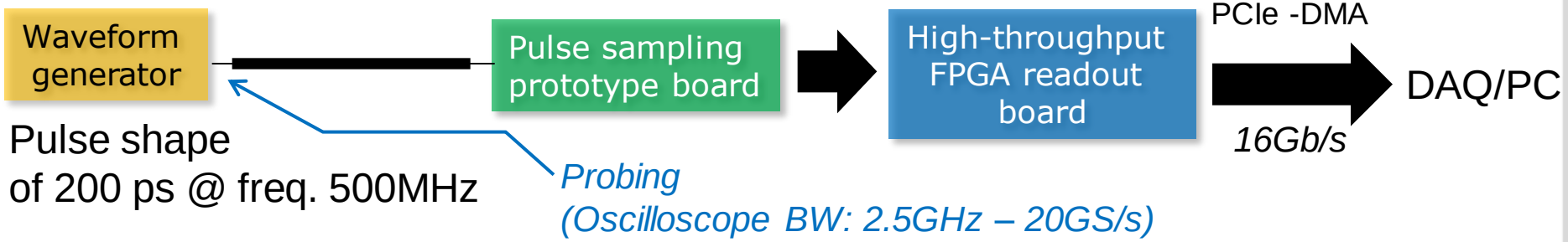
- 4 channels Fast Pulse shape Sampling board → is completed





- First board available → mid of February
- Test beam planned → summer 2013
- The commissioning for the experimental station → 2013.

Fast sampling prototype board – time characterization



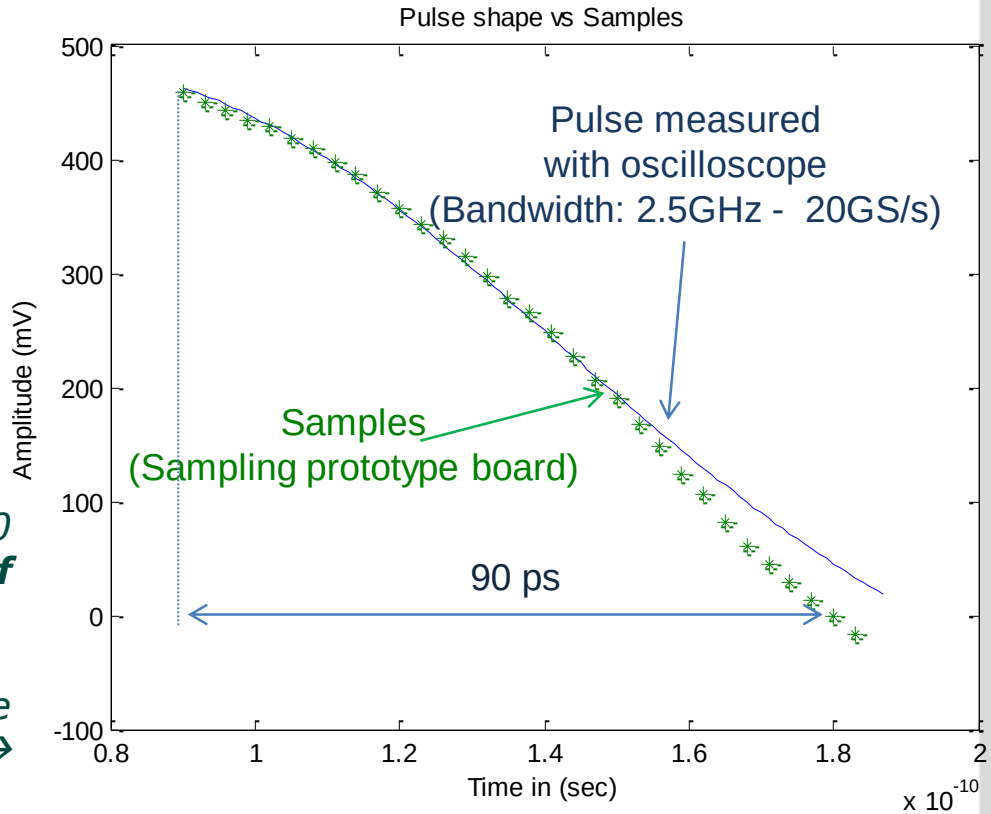
Fall pulse acquired by equivalent time sampling method (both oscilloscope and sampling prototype board)

(When the pulse occurs, a minimum settable sampling time is added by the delay chip in order to move the sampling time with a minimum time step)

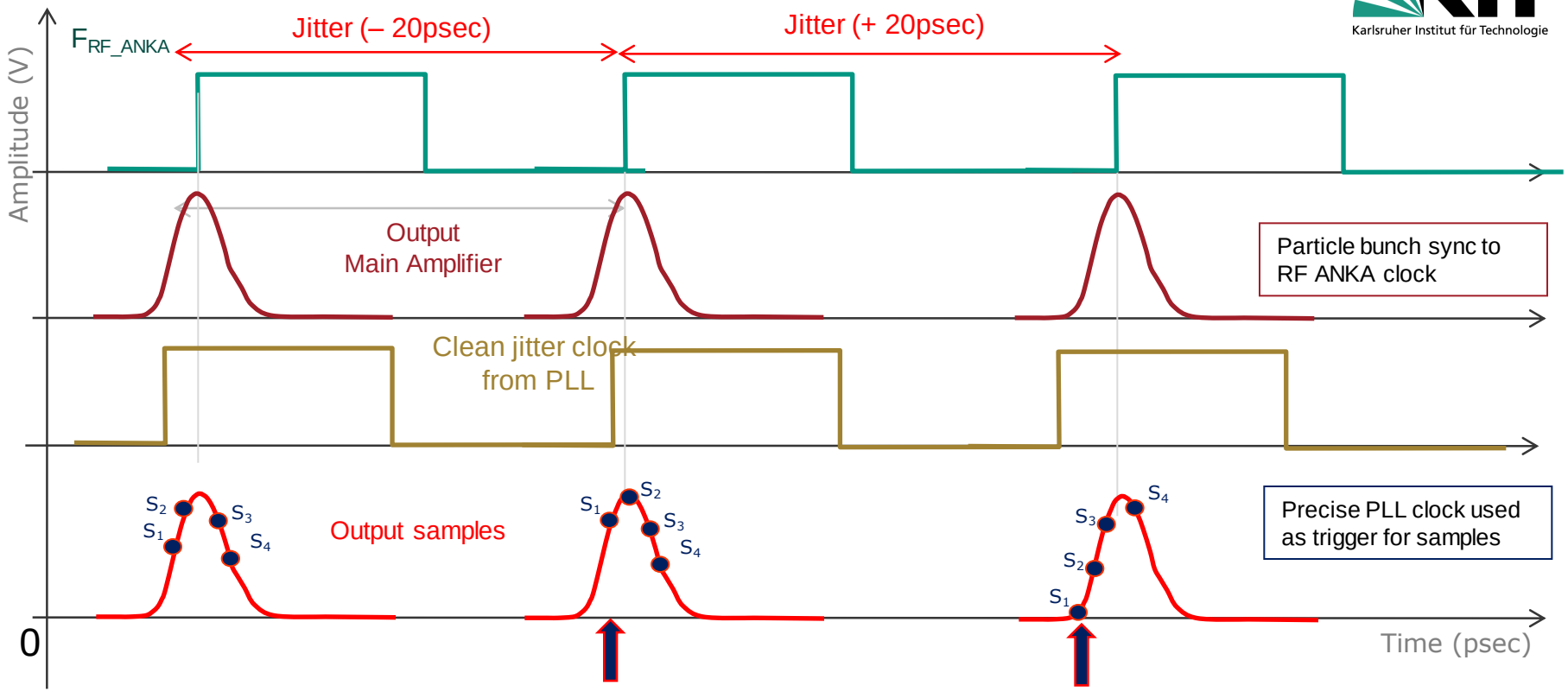
The pulse profile was obtained by 32 samples, one for each delay chip setting.

We recorded the pulse fall time by 30 samples inside 90 ps → a ***time accuracy of ~ 3 ps***

High linearity *between the sampling time (set by FPGA) and the real sampling time → Very low deterministic jitter on the board*



Picosecond time jitter estimation between bunches



Procedure:

Fast reconstruction of the analog pulse by the 4 samples (FPGA or GPU)

→ Measuring of the peak pulse amplitude

→ Measuring of the time jitter between bunches by the position of the samples in the reconstructed pulse