

DEVELOPMENTS AND PERFORMANCE OF THE LLRF SYSTEM OF THE S-BAND FERMI LINAC

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Abstract

The requirements on beam quality of the FERMI Free Electron Laser (FEL) linac impose challenging specifications on the stability of the RF fields that can only be met using reliable and high performance state of the art LLRF systems. The system installed in FERMI has met these requirements and is routinely operational for the machine on a 24/7 basis. The completion of the deployment of the LLRF units in 2015 increases the capabilities of the system, adding further measurements channels and monitoring, and allowing new functionalities. This paper provides an overview of the results achieved with the LLRF system of FERMI and an outlook of the further developments that are being implemented or planned.

INTRODUCTION

FERMI, the Italian seeded FEL located in Trieste, consists of two FEL lines, FEL-1 and FEL-2, covering the wavelength range between 20 and 100 nm and between 4 and 20 nm. Both the two FEL lines are now open to external users [1]. The accelerator is based on a 1.5 GeV S-band linac [2]. FEL generation requires very high beam stability and for the S-band RF system this translates in a specification of a stability in RF phase and amplitude within 0.1° rms and 0.1% rms respectively [3]. In addition to a careful design of all the parts of the system, from modulators supplies to cables and waveguides temperature stabilization, meeting these targets requires a high performing LLRF system. The LLRF system measures the RF signals and, according to the requirements and taking into account the beam feedbacks, controls the RF drive to the klystron. The system implemented in FERMI is an all-digital system specifically designed in collaboration with Lawrence Berkeley National Laboratory [4].

SYSTEM DESCRIPTION

Fourteen 3 GHz 45 MW peak RF plants are installed to power sixteen accelerating sections, the RF gun and the three RF deflectors. Two more accelerating sections will be added at beginning of 2016. An additional power plant is installed to provide a hot-spare backup solution for the first two. The basic hardware unit is the LLRF chassis. The layout foresees one of them for each RF powered component of the machine, whether it is an accelerating section or gun or deflector. In case of plants which power more than one section, one chassis will act as the master, controlling the RF drive to the klystron, besides monitoring the corresponding section parameters, while

the second one will act as a slave chassis primarily providing information to the master, for example the RF measurements of the second section.

Hardware

The LLRF chassis basically includes the RF front end (RFFE), the processing board (AD board), the OCXO and all power supplies (see Fig. 1) [5]. The RFFE performs the conversion between RF (3 GHz) and IF (99 MHz) signals and hosts all the frequency dependent components. The AD board, which implements a Virtex5 FPGA, performs all controls, diagnostics and system communication. The chassis has five RF inputs and two RF outputs. The inputs signals are the reference, the klystron output, the cavity input forward, the cavity input reflected and the cavity load signals. The outputs channels are used for the driving signal to the klystron and to generate a calibration signal. Each LLRF unit is designed to be beam feedback ready.



Figure 1: LLRF chassis.

A block diagram of a complete LLRF for a one klystron/two sections plant is shown in Fig. 2. The scheme shows as well the interconnections of the LLRF units with the other systems of the machine. All the components of the LLRF for each plant are installed in a temperature controlled EMC shielded IP65 rack. The temperature is kept stable better than ± 0.2 °K by means of an air/water heat exchanger. Also all the cables between racks and accelerating structures are installed in an insulated environment.

Firmware

The firmware presently in operation [6] implements all the basic loops needed: amplitude, phase, cable calibration, local oscillator phase drift and phase reference locking loops. All these are feed-forward loops. In addition, the control of the SLED phase reversal and phase modulation is also implemented through the LLRF firmware.

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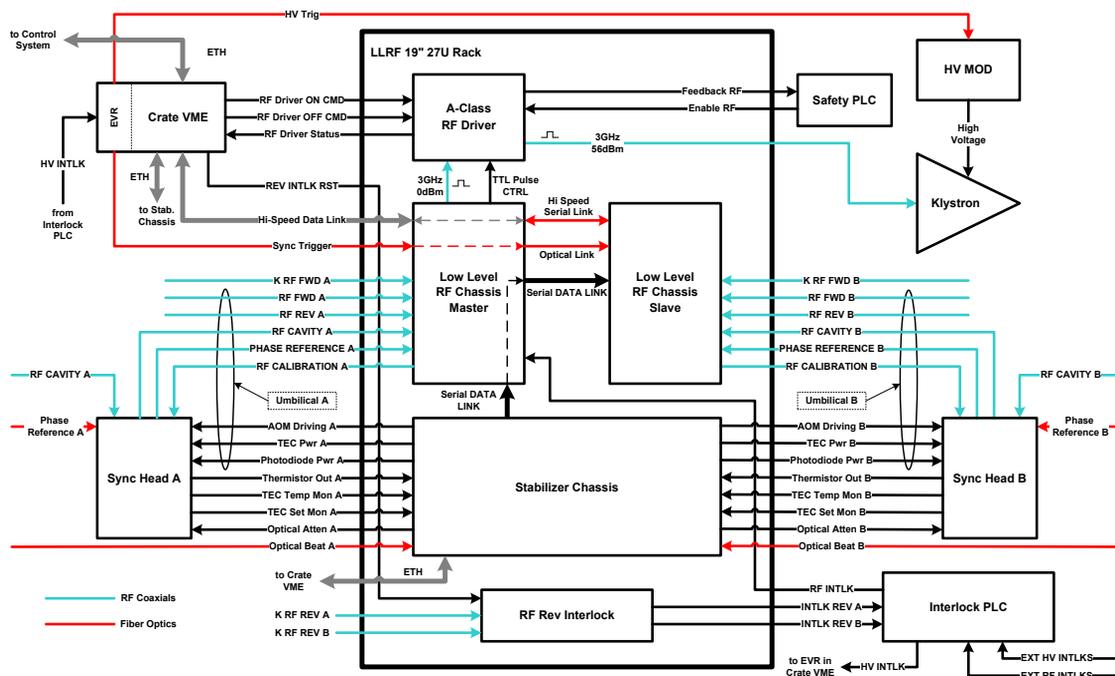


Figure 2: Block diagram of the LLRF for the double section/one plant case.

STATUS AND OPERATION RESULTS

One chassis per plant is installed and operational. After the initial operation with a commercial processing board, all the chassis have been upgraded in 2014 to the final AD board specifically designed for FERMI, which allows higher processing speed and an increased number of measuring channels. With both the boards the specifications (0.1 % amplitude and 0.1 ° phase) are met with a large margin, however, the installation of the AD board has provided an improvement in the performance which has been evaluated in a better stability, both in amplitude and phase, around 20 %. The implementation of the rack temperature control and stabilization has then given an additional improvement that has been estimated around 19 %.

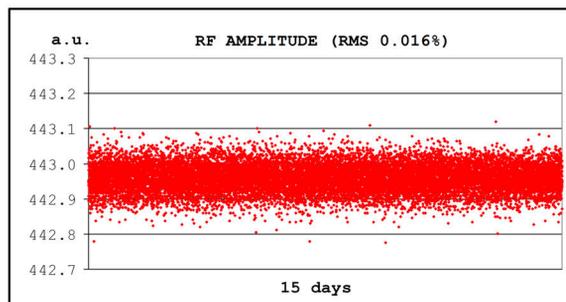


Figure 3: Amplitude stability measurement, long term acquisition on one plant.

The achieved stabilities are in the order of 0.016 % in amplitude and 0.043° in phase. As an example, Fig. 3 and Fig. 4 show a long term acquisition (15 days) of amplitude and phase stability respectively. The LLRF

units operate, as all the machine components, on a 24 hours 7/7 basis for around 6500 hours/year. Reliability of the system is very good with no major faults.

The installation of the second units, the slave chassis, is now in progress and should be concluded by the end of 2015. At this point the layout foreseen in the project will be completed.

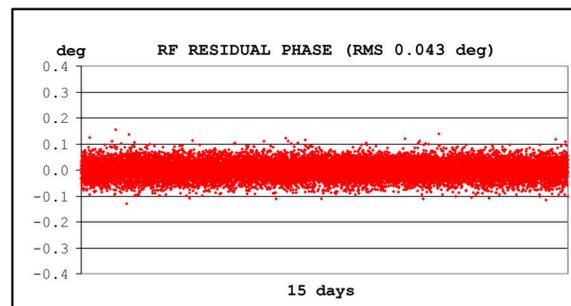


Figure 4: Phase stability measurement, long term acquisition on one plant.

DEVELOPMENTS

Double Chassis Operation

The slave chassis installation will primarily allow to increase the number of measured channels being acquired for the single klystron/two sections plants, since the measurements of the klystron forward power, cavity reflected power, cavity input power and cavity load power will also be available. It must be remembered that the klystron used, TH2132A, has two outputs each one feeding one section. Besides the increased monitoring, the installation completion opens the possibility of new field control regulation strategies, like implementing a vector

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sum of the voltages of the two sections or other algorithms exploiting the information acquired on the second cavity.

Communication between the slave and master chassis will be performed by means of a point-to-point optical link connecting the two units. Moreover the master chassis performs a bridge between the slave chassis and the control system. The firmware for the communication of the chassis has been developed and is now under test.

Intra-pulse Feedback and Clock Doubling

The present feedbacks are inter-pulse feedbacks and correct the RF drive power to the klystron between pulses. This scheme compensates mainly drifts in phase and amplitude, but does not correct random jitter contributions. Shot to shot jitter contributions can be related to different reasons. The most important factor is caused by modulator instabilities, which can be related to the HV power supply or the pfn charging. An intra-pulse feedback should be able to correct these jitter contributions acting inside the single RF pulse which has a maximum duration of 4.5 μsec [7].

The major constraints for an intra-pulse feedback implementation are related to the latency time, which comes mainly from three contributions: the section filling time, the digital acquisition time and the digital processing time.

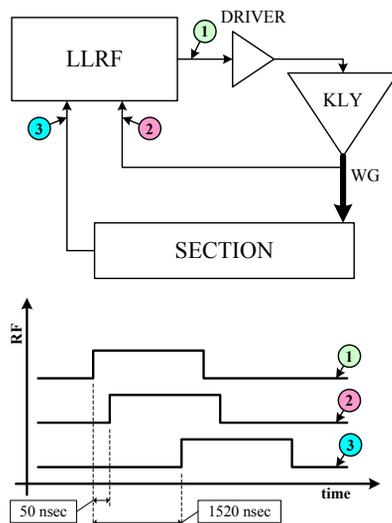


Figure 5: Layout (upper) and signal delays (lower).

The section filling time, for the different types of accelerating structures used in FERMI, ranges between 0.8 and 1.5 μsec and represents the major contribution to the latency time. However, since waveguides and section are passive elements, they introduce drifts and not jitter. Drifts are already corrected with the present inter-pulse feedback. Therefore the sample of the RF field at the output of the klystron will be acquired and used (see Fig. 5). In addition to eliminating the contribution of the section filling time this has also the advantage of having a

minor contribution from the cables, which will be much shorter.

The AD board features low latency ADCs, high FPGA clock frequency and double data rate DACs. The digital acquisition time minimization was already considered in the design of the AD board, using low latency components and optimizing the design to have high acquisition accuracy (0.017°, 0.029 %), avoiding in this way the need to averaging the input signal.

To reduce the digital processing time, firmware developments are on-going for the clock doubling. This means to increase the data elaboration frequency from the present 121 MHz (ADC sampling frequency) to 242 MHz, performing an interpolation of the input data. Introducing an interpolation of the input data means also to add a FIR filter at the input and then to add some clock period in the digital process. However, thanks to the halving of the clock period, it is expected that the total digital processing time should be reduced roughly to 60 % of the original one.

CONCLUSION

The FERMI linac LLRF system is in operation meeting the design specifications on phase and amplitude stability. It is in routine operation with the reliability and operability necessary for a users' facility. The completion of the hardware installation will allow to extend the capability of the LLRF systems with the implementation of further features and developments.

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