

MEASUREMENT OF CLOCK JITTER IN BEAM DIAGNOSTIC SYSTEM*

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Abstract

Low clock jitter can improve the performance of beam diagnostic system. This paper presents a procedure for the direct measurement of low-level clock jitter. High resolution spectrum analyzer or broadband high sampling rate oscilloscope is not demanded by using this method. Simulation will be introduced.

INTRODUCTION

As the demand for high fidelity sampling of clock frequency in excess of 100MHz continues to increase in beam diagnostic system, the aperture uncertainty (jitter) of the system sampling clock itself is becoming the limiting factor of the achievable SNR of the whole signal-conditioning chain [1]. Numerous methodologies have been proposed and discussed, since jitter performance still is one of the most challenging issues in state-of-the-art sampled systems [2].

The most directed method is using broadband high sampling rate oscilloscope. However, to measure clock jitter less than 20ps, the sampling rate of oscillator must be more than 50Gps where the effective number bits of the ADC in oscilloscope is more enough. Integrating the phase noise near the central frequency can also obtain the clock jitter if we have a high resolution spectrum analyzer. To measure low-level clock jitter, the dynamic range of spectrum analyzer will be not enough.

Another strategy to measure the clock jitter is through the SNR of the sampling system itself. The simplest and most widely adopted one infers the jitter value from the SNR measurements at high input frequency, where the random deviation σ_T of the occurrence of the sampling edge translates into a random voltage error $\sigma_{V_{jitter}}$ that dominates the noise deviation σ_V . The retro-fitting is usually accomplished according to the formula:

$$SNR = \frac{P_{in}}{\sigma_V^2} \approx \frac{P_m}{\sigma_{V_{jitter}}^2} = \frac{A_{IN}^2 / 2}{\sigma_T^2 \frac{(A_{IN} \omega_{IN})^2}{2}} \quad (1)$$

as applied to a sinusoidal input of amplitude A_{IN} and angular frequency $\omega_{IN} (= 2\pi f_{IN})$:

$$V_{IN}(t) = A_{IN} \sin(\omega_{IN} t) \quad (2)$$

Previous methods of estimating the jitter from the ADC's SNR were hampered by the imperfect knowledge of the real values of thermal noise, random non-linearity contributions, and any additional noise effects entering Eq. (1). Determining a f_{IN} high enough for the formula to be applied was somewhat of an arbitrary process. At very high input frequencies lots of dynamic effects such as

substrate noise, signal leakage, complex device behavior, and many more, affect the noise term of the equation thus making the jitter estimation harder.

This paper describes a precise yet easy method of measuring the jitter of a clock. The description of an innovative technique for the determination of the jitter in sampled-input systems is provided. The extraction of the period jitter from the SNR data collected on a 14b 105MSps ADC is then simulated.

CALCULATING JITTER THROUGH INPUT COHERENT SAMPLING

Coherent sampling (or locked-histogram) techniques have been successfully employed in the past in order to estimate clock jitter. However, this paper presents a parametric analysis of the correlation between the jitter and the phase of the input at which noise is measured. The main advantage of the proposed technique is that the measurements obtained from the clock under test are parametrically fitted to the true profile of the jitter in such a system, thus providing for a true numerical solution to the problem. In addition, since the results are fitted to the expected shape of the jitter vs. phase theoretical dependence, the clock jitter can be measured down to levels lower than the ones allowed by the noise floor of the converter.

Jitter Formula Derivation

The theoretical RMS voltage error $\sigma_{V_{jitter}}$ induced by the clock cycle jitter (defined as the standard deviation of the Gaussian distribution of the periods, σ_T) is calculated through the input slope via the formula:

$$\begin{aligned} \sigma_{V_{jitter}} &= \sigma_T \cdot \left| \frac{\partial V_{IN}(t)}{\partial t} \right| \\ &= \sigma_T \cdot A_{IN} \omega_{IN} \cdot |\cos(\omega_{IN} t)| \end{aligned} \quad (3)$$

Equation (3) quantifies the well-known concept that when an ADC is sampling a sinusoidal input, the contribution of clock jitter is much more pronounced when the sampling instant coincides with the zero crossing of the input, and has very little impact on the output noise when the sampling instant coincides with the top or bottom of the input sinewave.

Figure.1 illustrates this concept: the Gaussian distributions shown on the right represent the histogram of the captured output samples of the ADC, in the two cases described.

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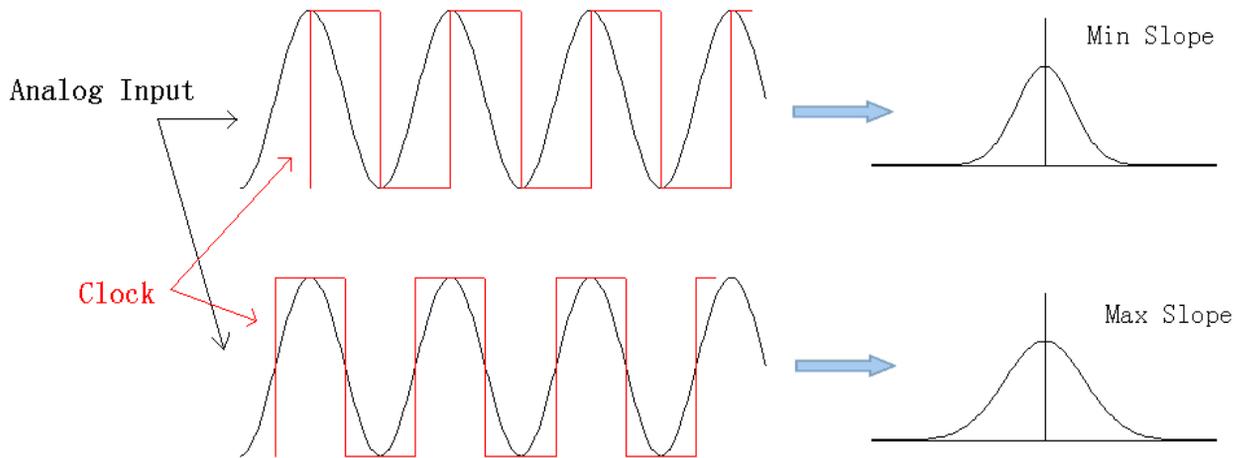


Figure 1: Sinusoid sampling at different phases: sampling at the top of the input sinewave yields a much tighter output code distribution than sampling the input at its maximum slope (zero-crossing).

Locked-histogram Sampling Basics

Ideally, in order to remove any dynamic and non-linear effects and isolate the random contribution of the jitter, the best possible condition is to feed the quantizer of the ADC with dc input. Obviously, no real information could be derived from providing a signal to the input of the ADC at 0Hz, other than the theoretical maximum attainable SNR and the converter's noise floor. However, a careful choice of input and clock frequencies and their relative phase makes the input of the ADC appear as dc.

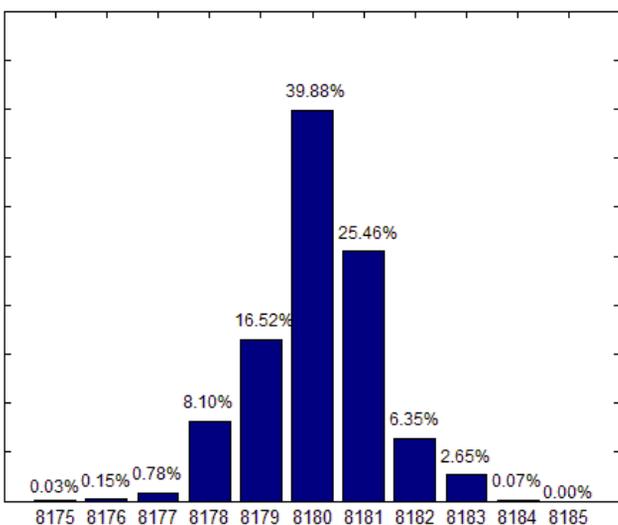


Figure 2: Histogram of sampling system under test with DC input applied. The x-axis represents the ADC output code in LSBs, and the height of the barrels is the percent hit count for each code in a run of 16384 sample points. The mean of the distribution is 8180 LSBs, indicating an offset of approximately 12 LSBs.

This can be accomplished by coherently sampling the input; i.e., adopting a sampling rate $f_s = f_{IN}/N$ (N integer) to sample the same voltage in every period, or every few

periods. For a sinusoidal input, the sampling instant can be set to occur always at the V_{IN} peak (90° phase of the input waveform), always at the zero crossing (0° phase), or so forth at any intermediate point. And the SHA the signal to be quantized is indeed a dc.

We use the matlab module of AD6645 provided by analog device to simulate this sampling process and in this way, it is possible to obtain a distribution of the noise for each ADC code, as shown in Figure 2 where the input to the ADC V_{IN} equals 0V. In this case, the ADC output should be at its midscale value, $2^{13} = 8192$ for the 14-bit ADC under test. Figure.2 exemplifies the simulation outcome of the procedure used to collect the code histograms at dc level. If jitter is present, the Gaussian curve will be wider for samples taken close to the zero-crossings, and narrower when sampling near the peaks. The standard deviation of the noise represents only the thermal noise contribution, plus injections from substrate and any other terms not related to jitter. The adoption of "locked histogram" methods guarantees a distinctive advantage over other techniques where the samples still change with time during the measurement, since dynamic non-idealities in the quantizer (reference bounce, hysteresis effects in the stages, etc.) are completely removed [3].

SIMULATION RESULTS

The matlab module of AD6645 can be used to simulate the real device. AD6645 is a 14bit 105Mps ADC, so we choose sampling rate $f_s = 100$ Mps in the simulation and add 2ps jitter to the sampling clock. The analog input is also chosen to be 100MHz. The sampling clock and the analog input are coherent. We change the relative phases between sampling clock and the analog input, and then calculate the RMS voltage error σ_V through 4096 points.

The data collected at different relative phases $\Delta\phi$ of input vs. clock are represented in Fig.3.

Once collected, the data can be fitted to the theoretical noise vs. phase dependency shown as Eq.(3) through an LMS algorithm. This method enables the extraction of the RMS jitter from the best-fit function found, providing an accurate measurement. In Fig.3, we obtain the RMS voltage error 2.26LSB and calculate the clock jitter value 2.23ps.

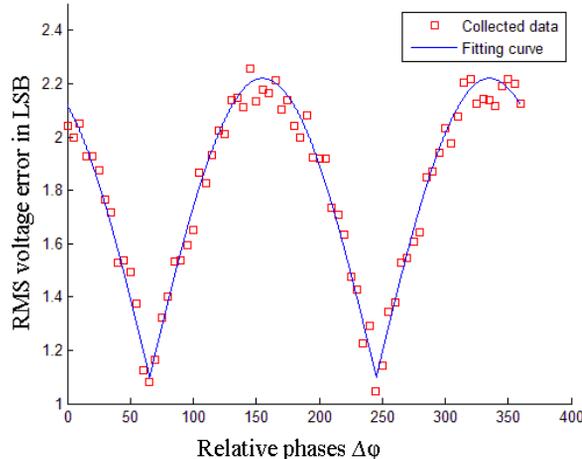


Figure 3: σ_V vs. $\Delta\phi$ at 100MSps clock rate with 2ps jitter, 100MHz coherent input: the σ_V due to jitter amounts to 2.26LSB.

The same principle can be extended to undersampled inputs, yielding the same evidence. Figure 4 shows the simulation results and parametric fit for the case where the analog input f_{IN} is 200MHz, with the ADC still sampling at 100 MSps. The RMS voltage error is 4.61LSB and we calculate the clock jitter value 2.35ps.

Figure 5 is the case where the analog input f_{IN} is 300MHz, with the ADC sampling at 100 MSps. The RMS voltage error is 6.83LSB and we calculate the clock jitter value 2.28ps.

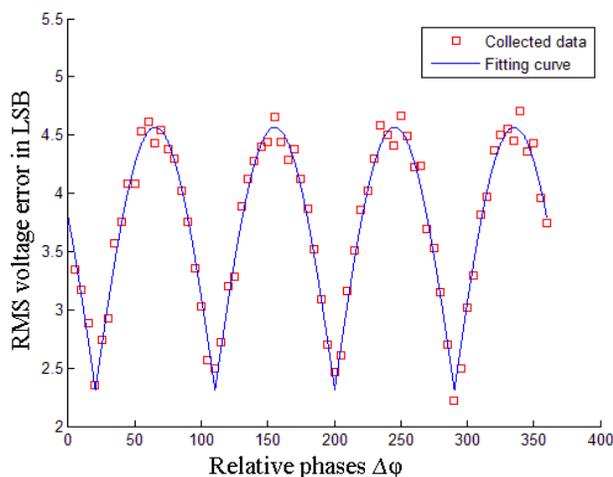


Figure 4: σ_V vs. $\Delta\phi$ at 100MSps clock rate with 2ps jitter, 200MHz coherent input: the σ_V due to jitter amounts to 4.61LSB.

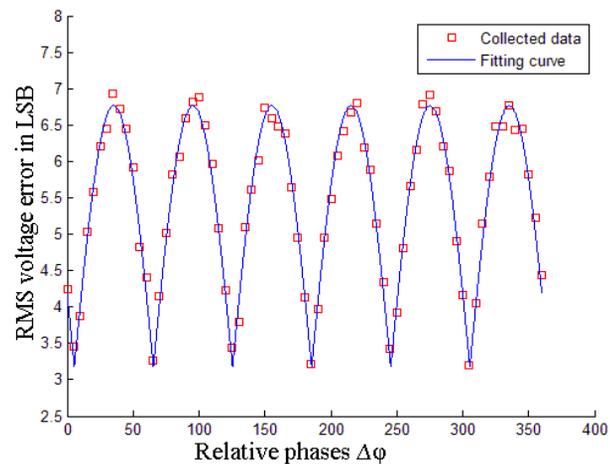


Figure 5: σ_V vs. $\Delta\phi$ at 100MSps clock rate with 2ps jitter, 300MHz coherent input: the σ_V due to jitter amounts to 6.83LSB.

CONCLUSION

In this paper, we present a convenient method for measuring RMS jitter of sampling clock in beam diagnostic system using the locked histogram coherent sampling method. The technique enables a direct and parametric measurement of the sampling instant uncertainty. Simulation result through MATLAB module of AD6645 shows this methodology can easily measuring picosecond RMS jitter without high resolution spectrum analyzer or broadband high sampling rate oscilloscope.

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