

# BUNCH BY BUNCH DBPM PROCESSOR DEVELOPMENT AND PRELIMINARY EXPERIMENT IN SSRF\*

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## Abstract

Digital BPM processor with turn-by-turn capability has been widely used in synchrotron radiation facilities over the world, which is proved to be very useful and powerful for daily operation and linear optics study but not good enough in the case of individual bunch information required. In order to sufficient individual bunch diagnostics requirements a development plan of the next generation DBPM processor with bunch-by-bunch capability has been initiated in SINAP since 2012. The whole development was divided into three steps: a concept processor based on digital oscilloscope IOC, an algorithm prototype processor based on commercial high speed ADC board, and a custom designed dedicated processor. The progress of this work and several preliminary beam experiments will be discussed in this paper.

## INTRODUCTION

In order to improve the efficiency and quality of the light, the top-up mode was adopted at the SSRF since the end of 2012, which results more frequent beam injections (about one injection in ten minutes).[1] Since injection process involves a variety of equipments, parameters of all the equipments can not match perfectly with each other during the transient injection process. Any parameter mismatching will lead to a closed orbit distortion, which will leave a residual betatron oscillation after injection. For light source users, this disturbance must be as little as possible. An appropriate analysis and diagnosis tool is needed to provide basis for optimizing the parameters of related equipments.

The turn by turn position data and slow acquisition data acquired by normal DBPM processor can be used to observe the average effect of bunch train disturbance. The excitation current waveform mismatch between kickers and the alignment error of kickers can be studied by using these data. But the disturbance introduced by refilled bunch is hardly analysed using turn by turn data. In this case a new DBPM processor with bunch by bunch capability is required.

On the other hand realizing the measurements of the bunch by bunch position will also help study the beam impedance, coupling instability and nonlinear dynamics quantitatively, and can provide the accelerator physicists with an incredibly powerful machine study tool.

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## DEVELOPMENT OF BUNCH BY BUNCH DBPM PROCESSOR

The development was divided into three steps: a concept processor based on digital oscilloscope IOC, an algorithm prototype processor based on commercial high speed ADC board, and a custom designed dedicated processor.

### Concept Prototype Based on Oscilloscope

A digital oscilloscope embedded EPICS IOC was developed in SSRF to do transverse position measurement at bunch-by-bunch rate.[2] The hardware setup is shown in Fig. 1. Broad band beam signals coupled from four button electrodes, passing through a BPF (central frequency 500MHz, BW 300MHz), are feed into four channels of scope directly. To satisfy bunch-by-bunch analyse requirement an high performance digital oscilloscope, practically Agilent DSO9064A (analogue BW 600MHz, real-time sampling rate 5GHz for 4 channels, and 100M samples per channel on-board buffer), is adopted. Beam signal will be recorded simultaneous at 5GHz sampling rate.

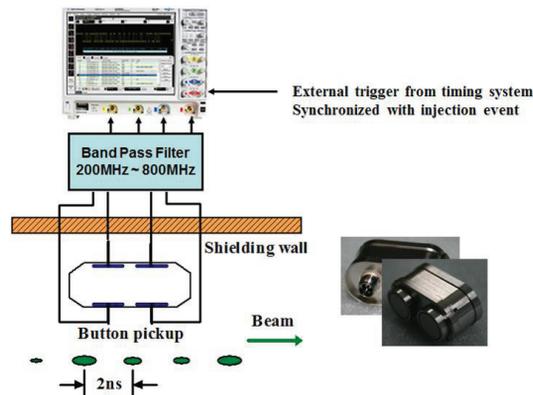


Figure 1: Hardware setup of the concept prototype of bunch-by-bunch processor.

If the sampling rate or its fraction is equal to machine RF frequency (synchronized sampling) the peak value of raw data can be used to calculate bunch charge and bunch position using  $\Delta$  over  $\Sigma$  method directly. But for SSRF, RF frequency is usually varying between 499.654MHz and 499.674MHz depending on ground temperature. In this case using raw data will introduce a large sampling phase noise due to difference of RF and sampling frequency. A specific data processing method we called "virtual re-sampling" technique is employed to solve this problem. With correct sampling frequency and initial

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sampling phase, synchronizing sampled data can be calculated using spline interpolation method. Ideal sampling frequency, which is equal to practical RF frequency, can be determined by using zero-padding FFT method which makes the data length 128 times than the raw data. Meanwhile the initial sampling phase can be defined manually based on raw waveform.

The beam experiment result shows that the position resolution of 50 microns has been achieved with such a concept prototype shown in Fig. 2.

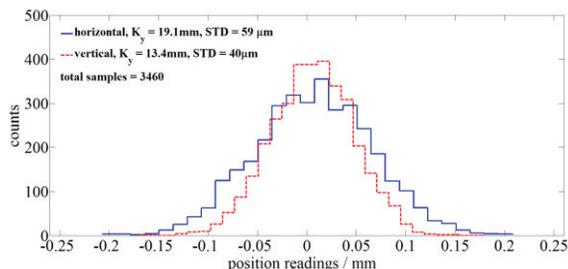


Figure 2: Position resolution of the concept prototype.

### Algorithm Prototype Based on Commercial High Speed ADC Board

The hardware architecture of the algorithm prototype of bunch-by-bunch processor is shown in Fig. 3.

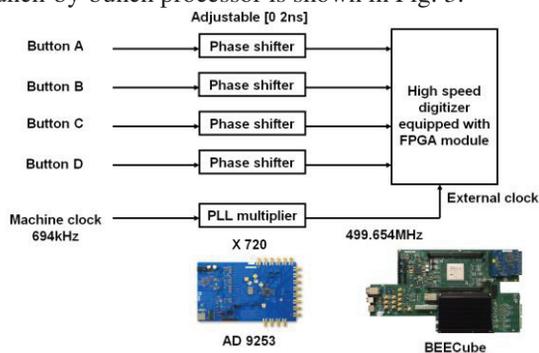


Figure 3: Hardware architecture of the algorithm prototype of bunch-by-bunch processor.

To get the synchronous sampling clock, we use a wideband synthesizer as PLL which multiplies the machine clock (694kHz at SSRF) 720 times and the frequency of sampling clock is strict equal to RF frequency. BEEcube, a high-performance FPGA-based computing, prototyping, and emulation platform featuring the Xilinx Virtex-6 family of FPGAs, is adopted to do data acquisition. 4GB on board DDR3 module is large enough to capture more than 10Mpts of raw data (about 20ms). The ADC on the system is ISLA214P50 which is a 14-bit, 500Mps analog-to-digital converter designed with a standard CMOS process.

Since the length of four cables from BPM to each channel of the data acquisition system could be different and to achieve the sampling point at the peak of the signal waveform, we insert adjustable phase-shifter before the data acquisition system.

Figure 4 shows the system resolution on different bunch charge, and if the intensity of signal is big enough, the position resolution of 10μm can be achieved.

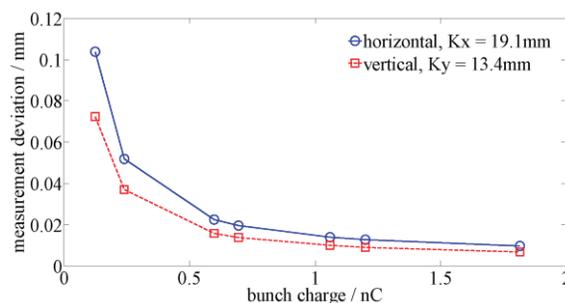


Figure 4: Position resolution of the algorithm prototype.

### Custom Designed Dedicated DBPM Processor

The architecture design and PCB design of the dedicated DBPM processor are completed for now and the first demo unit can be expected to be online at the end of this summer. The function diagram of hardware architecture is shown in Fig. 5.

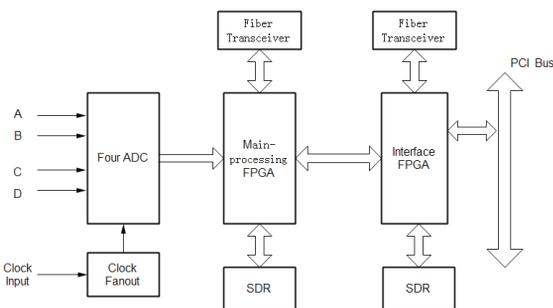


Figure 5: Hardware architecture of the custom designed bunch-by-bunch processor.

Four ADCs digitizes the analog signal from BPM. Compromising the sampling rate, quantization bits and analog bandwidth, we will choose ADS54RF63 produced by TI. The main-processing FPGA receives the data from ADC and calculates the bunch position. The main-processing FPGA must have the ability to receive the data with 500Mbps data rate and have enough processing units like multiplier. EP2C70F896 will be used in our design.

A CPCI crate will be utilized and the crate controller will run Linux operating system and EPICS IOC. The interface FPGA will translate the internal bus signal to PCI bus signal. Fiber transceiver will also be used for remote data transmission in the future.

## BEAM EXPERIMENTS

Both concept prototype and algorithm prototype have been used in normal user operation and machine study.

### Study of Injected Bunch

The bunch by bunch position data collected during injection was used to evaluate the performance of injection system and study the behaviour of injected bunches.

The PCA method was proved to be very useful for bunch by bunch data analyse. Using this tool the refilled bunch index can be easily identified and the transverse motion of injected fresh bunch can be separated from stored bunch. Then the behaviour of fresh bunch during

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injection process can be observed and studied. Fig. 6 shows a typical measurement of such a transient state: (a) transverse oscillation of stored bunch (blue, almost pure betatron oscillation) and fresh injected bunch (red, mixture of betatron and energy oscillation); (b) position spectrum variation of fresh bunch in the first 200 turns after injection; (c) oscillation mode analyse of fresh bunch.

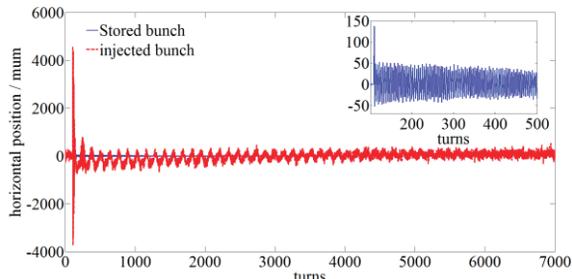


Figure 6 (a): Transverse oscillation of stored bunch (blue) and injected fresh bunch (red).

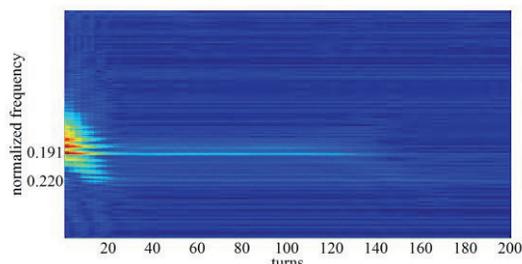


Figure 6 (b): Position spectrum variation during the first 200 turns after injection.

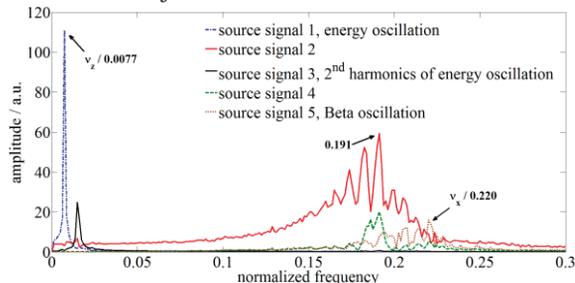


Figure 6 (c): Oscillation modes of fresh bunch.

### Wake Field Measurement During Injection Stage Using Bunch Train as Probe

The bunch by bunch position data collected during injection stage can also be used to study wake field issue. In this case the stored bunch train can be treated as a probe to sample wake field strength.

The more details including model, data analyse method and experiment results can be found in the reference [3].

### Beam Loss Analysis

Unexpected beam loss occurred when average current reached 240 mA with uniform filling of 500 bunches in 2013. To achieve higher current the cause of beam loss need to be identified. The fast ion instability is accepted as a reasonable guess based on the filling pattern after beam loss. To confirm this guess the bunch by bunch data was collected before and after beam loss. Fig. 7 shows a

typical measurement: (a) bunch filling pattern before beam loss; (b) betatron oscillation amplitude distribution before beam loss; (c) bunch filling pattern after beam loss.

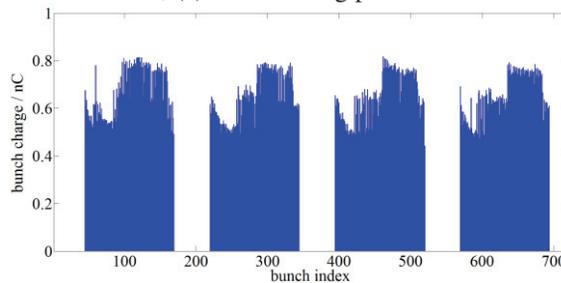


Figure 7 (a): Filling pattern before beam loss.

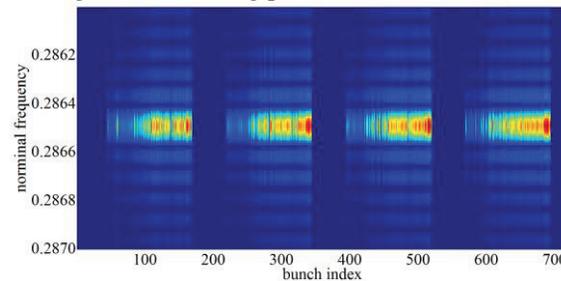


Figure 7 (b): Betatron oscillation amplitude distribution.

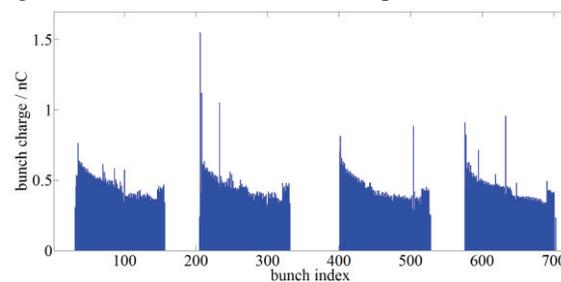


Figure 7 (c): Filling pattern after beam loss.

The result showed that there was a strong correlation between the bunch filling pattern after beam loss and betatron oscillation amplitude distribution.

## CONCLUSION

Several prototypes of bunch-by-bunch beam position acquisition system at SSRF have been developed. Beam position resolution of 10 microns can be achieved with proper signal strength. Bunch by bunch instrument was proved to be a very useful tool in machine study.

## REFERENCES

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