

QUALIFICATION OF THE BYPASS CONTINUITY OF THE MAIN DIPOLE MAGNET CIRCUITS OF THE LHC

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Abstract

The copper-stabilizer continuity measurement (CSCM) was devised in order to attain complete electrical qualification of all busbar joints, lyres, and the magnet bypass connections in the 13 kA circuits of the LHC. A CSCM is carried out at ~ 20 K, i.e., just above the critical temperature, with resistive magnets. The circuit is then subject to an incremental series of controlled powering cycles, ultimately mimicking the decay from nominal current in the event of a magnet quench. A type test to prove the validity of such a procedure was carried out with success in April 2013, leading to the scheduling of a CSCM on all main dipole circuits up to and including 11.1 kA, i.e., the current equivalent of 6.5 TeV operation. This paper details the procedure, with respect to the type test, as well as the results and analyses of the LHC-wide qualification campaign.

INTRODUCTION

Following the 2008 incident [1], thorough investigation found that this was as a result of discontinuities in the superconducting busbar-joints' copper stabilizer - depicted in Fig. 1. To prevent such an event happening again, the LHC was operated at 3.5-4 TeV for the duration of Run 1. To allow for operation of up to nominal energy, it was decided that, during Long Shutdown 1 (LS 1), every interconnect (over 10,000) was to be repaired and consolidated with each splice having an electrical shunt applied, Fig. 2 [2].

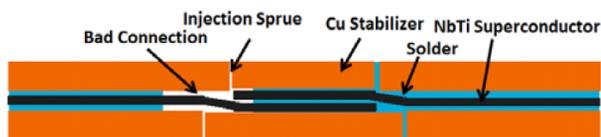


Figure 1: Depiction of a typical main dipole splice showing both good (right side) and bad (left side) continuity.

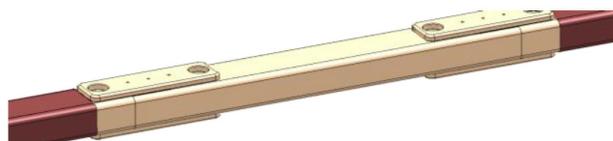


Figure 2: Illustration of the splice consolidation shunts, as applied, to reduce overall connection resistance and prevent adverse consequences from quenches in these locations [2].

LS 1 electrical quality control (ELQC) measurements at warm, ~ 300 K, found that 5.9 % of all splices ex-

ceeded the acceptance criteria [3]. Furthermore, abnormally high resistances were found in the magnet bypasses, $> 200 \mu\Omega$ (accepted maximum being $15.5 \mu\Omega$) [4], as well as other types of soldered/welded connections [5]. Even though all discovered defects were consolidated, due to the foreseen quench training, with over 100 quenches predicted [6], an LHC-wide copper-stabilizer continuity measurement (CSCM) was carried out on all the main dipole circuits to guarantee that no defects were missed during LS 1 ELQC and that all aspects of all circuits are intact, in particular, the lyres, as they contain welded connections, but were not systematically checked during LS 1.

CSCM TEST PROCEDURE

The principle of a CSCM is to have the current bypass the magnets by operating at ~ 20 K - just above the critical temperature, making the magnets resistive. Fig. 3 shows the expected current flowing through the magnet bypass along a main dipole circuit. To provide sufficient voltage to account for this, two 6.5 kA/200 V sub-converters had to be connected in series, normally connecting in parallel. The result, however, is that tests require a short period of over-current. The test also required protection system (PS) board modifications to monitor both the voltage across all busbar segments from the magnet voltage taps, "BS board A", and the voltage across the busbar segments as well as the adjacent diode leads connections, at the diode voltage taps, "BS board B". The difference of the two ($B - A$) gives the voltage across the bypass diode leads, which encompasses six contacts. The BS boards allowed for V, dV/dt and d^2V/dt^2 thresholds to be set, ensuring detection and protection against any thermal runaways, by turning off the power converter (PC) (0.03 s decay constant due to the atypical inductance during a CSCM of only 3 mH, compared to 15.7 H during normal operation). Other, "DS", boards allowed for the monitoring of the voltage directly across the diodes.

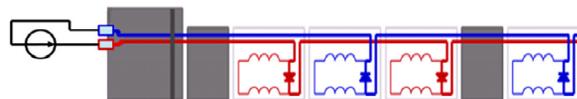


Figure 3: Depiction of the current flow during a typical CSCM test on a main dipole circuit. Note that all current flows through the bypass diodes instead of the magnets.

CSCM TYPE TEST IN LHC SECTOR 23

In April 2013, a CSCM type test was carried out [7]. Being prior to the splice consolidation campaign, thermal run-

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always were almost certainly guaranteed and system protection was paramount. All carried out tests were deemed a success in that all thermal runaways were detected and protected against with no measurable damage, proving CSCM a viable option as a qualification test. Figure 4 shows a thermal runaway in the main dipole circuit being successfully detected, protected against and accurately simulated, using CERN's own QP3 software [8].

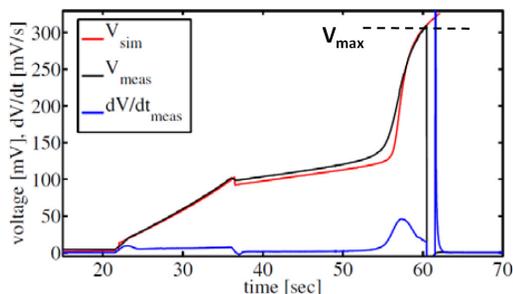


Figure 4: Plot of a measured, and subsequently simulated, thermal runaway occurring in a bad splice, being successfully detected and protected against, during the 2013 S23 CSCM type test [7].

LHC-WIDE CSCM CAMPAIGN 2014

Standardization and Procedure Changes

To standardize the procedure, fixed decay constants as well as ramp-up and plateau phase lengths, 92 s, 8 s and 4 s, respectively, were defined. This was possible due to the circuit's low inductance allowing for ramp-rates in excess of 1000 A/s. Furthermore, the number of overall high current powering cycles was reduced and the PS threshold calculations were simplified. However, as a precautionary measure, due to erratic cold diode behaviours witnessed during quench tests and follow-up experiments at CERN's SM18 test facility [9, 10], a low current, 400 A, resistance measurement was carried out between each powering cycle, to monitor trends and detect possible defects.

To define a circuit as completely qualified via CSCM, all connections of the circuit must withstand the maximum energy deposition, characterized by MIIts (the time integral of the current squared, in units of $10^6 A^2s$), expected to occur during a quench at nominal current levels, ~ 11.1 kA.

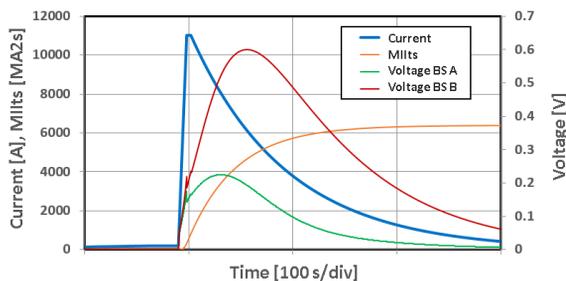


Figure 5: Typical CSCM powering cycle profile to 11.1 kA, as well as the simulated corresponding voltage and MIIts for a single bus segment.

The programmed decay constant was slightly faster than with nominal inductance, normally 104 s, to account for the MIIts accumulated during the ramp-up and plateau phases. The full qualification procedure involves six high current powering cycles, gradually increasing the peak current – 2, 5, 7, 8.6, 10 and 11.1 kA. This allows for detection of any faults at the lowest possible current, whilst having the qualification time remain reasonable. Figure 5 shows a simulated powering cycle of the final qualification cycle.

As the current is gradually increased, protection thresholds have to be set accordingly. For each cycle, the thresholds were re-calculated taking into account variations in current, voltage and temperature. Due to the scale of the scheduled campaign, the process of calculating the protection thresholds was also simplified, with respect to the type test, by using fixed additional margins across all tests, for V and dV/dt thresholds, accounting for calculation error and erratic diode behaviours.

Campaign Results

All splices, bypass connections and lyres of all main dipole circuits were eventually subject to the full programmed current decay from 11.1 kA, without a single thermal runaway being detected throughout the entire campaign of ~ 150 tests. Overall, the BS board A resistance measurements were relatively low and consistent throughout. Due to no thermal runaways occurring, one can conclude that all lyres are intact and survived the thermal cycling of LS 1 as well as that, in stark contrast to before consolidation, all splices of LHC can now withstand nominal current levels.

Regarding the bypass resistances, deduced from the difference in voltages (B – A) divide by the current, measurements were notably less consistent, with powering cycles sometimes increasing and or decreasing the subsequently measured resistance. However, looking at the LHC-wide bypass resistance averages, Fig. 6, one can see a trend of an initial increase, saturating at ~ 8 -10 kA, and then a notable decrease occurring as current levels increase. This trend was also witnessed during the aforementioned cold diode experiments in SM18. However, the underlying physical phenomenon is not fully understood.

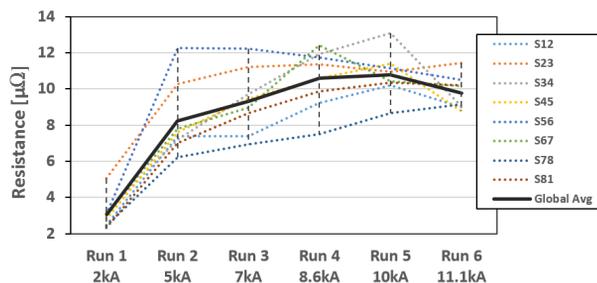


Figure 6: Global average of all bypass resistance measurements, for all sectors of the LHC. Note the initial rise, saturation and healing trend arising as current levels increase.

Investigating the worst cases, Fig. 7 show two examples of largest resistance increases, $>100 \mu\Omega$, during otherwise successful powering cycles. The non-linearities are typical erratic cold diodes behaviours, however, the notably linear global trend does show a steady increase in resistance in at least one of the encompassed bypass contacts.

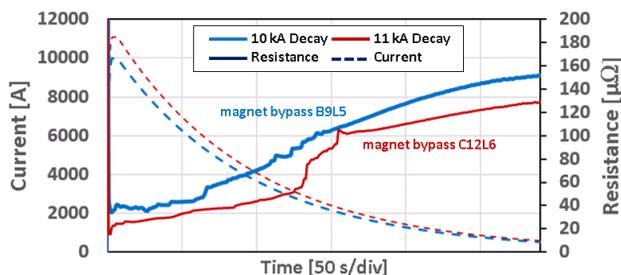


Figure 7: Two examples of the resistance increase of a magnet bypass, during a single event, exceeding $100 \mu\Omega$. Linear trend suggests steady increase in contact resistances.

Figure 8 shows the highest resistances, across all “successful” tests, measured during subsequent 400 A runs, for a given peak current. Also shown is the corresponding calculated temperature in the diode wafer, derived from the DS boards forward voltage, in correspondence with [11], and in the diode’s heat sink. The design maximum temperature for both is 300 K and 240 K, respectively. It is assumed that all excess resistance lies within only one of the six encompassed contacts and that there was a linear increase in resistance from previous measured values, mimicking the witnessed phenomenon. Furthermore, if the excess resistance were to be within the “half-moon” contact, which has no adjacent heat sink, the temperature would have been at least an order of magnitude higher and very fast thermal runaways would have occurred resulting in a trip and or structural damage. Therefore, one can conclude that most, if not all, abnormally high excess resistances were present in the diode-to-heat sink contacts. Nonetheless, resistance increases $>100 \mu\Omega$ come close to the rated maximum temperatures and deliberately inducing the witnessed resistance decrease was becoming a necessity for qualification.

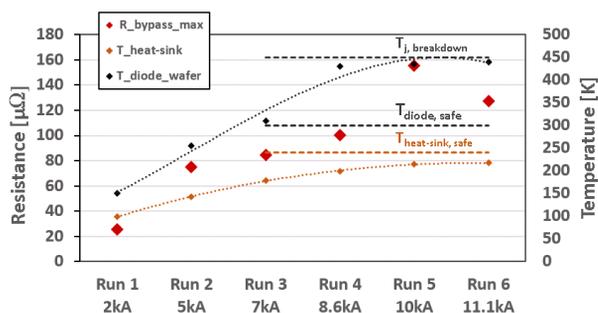


Figure 8: Maximum bypass resistance after each current level and the corresponding calculated temperature in the diodes and diodes’ heat sink. Resistances $>100 \mu\Omega$ result in temperatures above the design limits and close to the rated maximum values.

Inducing Diode-to-Heat Sink Contact Healing

The highest witness increase in resistance, from one cycle to next, was measured at a worryingly high $355 \mu\Omega$ – PS triggered a power abort ~ 10 s into the decay of a 10 kA cycle. At this point, it was decided not to proceed with the CSCM as normal and attempt to deliberately induce the healing effect in a controlled manner. The devised solution was to perform a stepped powering cycle with 1 kA increments and ~ 20 s plateaus, to deliberately heat up the particular contact in attempt to induce the witnessed healing phenomenon via Joule heating. The results were successful, reducing the same bypass resistance to below $55 \mu\Omega$. Furthermore, the stepped cycle was used twice more during the campaign to heal contacts that exceeded $100 \mu\Omega$, example shown in Fig. 9. It also follows that for any quench during training, normal operation, and or otherwise, all bypass resistances of the relevant magnet(s) are now to be systematically calculated and, if found to be high, one could induce healing in a similar manner, by provoking a quench. A follow-up study to understand the underlying sources of the physical phenomenon is under way [12].

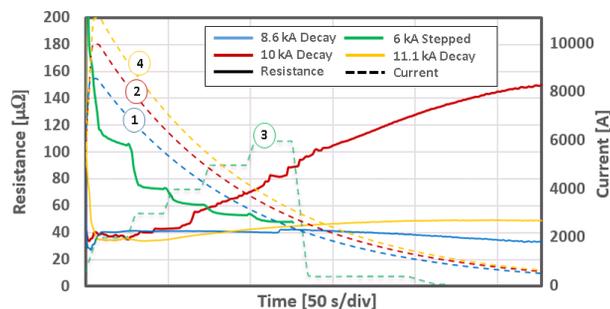


Figure 9: Stepped powering cycle being used to induce the healing phenomenon on a diode-to-heat sink contact following a previous 10 kA cycle greatly increasing its resistance.

SUMMARY

A CSCM campaign was carried out to completely qualify all of the LHC’s main dipole circuits’ magnet bypass continuity as well as all soldered/welded connections. A total of approximately 150 tests were carried out during the 2014 CSCM RB qualification campaign. In summary, the campaign went relatively smoothly, with the exception of erratic cold diode behaviours. Results gave further justification to systematically calculate the bypass resistances after every quench, during quench training, normal operation or otherwise. To conclude, all tested circuits were eventually subject to the full decay from 11.1 kA, without measurable damage, and the green light was given for quench training to begin.

REFERENCES

- [1] M. Bajko, *et. al.* “Report of the Task Force on the Incident of 19th September 2008 at the LHC”, *LHC-PROJECT-Report-1168*, CERN, 2009
- [2] F.F. Bertinelli, J.Ph. Tock, *et. al.* “Consolidation of the LHC Superconducting Circuits: A Major Step towards 14 TeV

Collisions”, *Proceedings of the IPAC’12 (THPPD032, pg. 3575-3577), New Orleans, Louisiana, USA, 2012*

- [3] S. Heck, J.-Ph. Tock, *et. al.* “Nondestructive Testing and Quality Control of the LHC Main Interconnection Splices”, *IEEE Trans. Appl. Supercond.*, vol. 25, no. 2, Oct. 2014, Art. ID. 4000108.
- [4] M. Bednarek. “Dipole diode lead resistance measurements”, *Presented to the MP3 Working Group, CERN, Jan. 2014.*
- [5] A. Perin. “Status of DFBA Splices Consolidations”, *Presented to the LS1 committee, Indico No. 257354, CERN, Jun. 2013.*
- [6] A. Verweij. “Training the Dipoles”, *Proceedings of Chamonix Workshop 2009, Indico No. 45433, Chamonix France, 2009.*
- [7] S. Rowan, H. Thiesen, A. Verweij, *et. al.* “CSCM: Experimental and Simulation Results”, *Proceedings of the IPAC’14 (THPRI093, pg. 3988-3990), Dresden, Germany, 2014*
- [8] A. Verweij. “QP3 Users Manual”, *CERN Document Server, EDMS No. 1150045, 2011.*
- [9] M. Koratzinos. “A proposal for a fourth series of Quench propagation tests”, *Presented at the TE-MPE-TM, Indico No. 159542, Oct. 2011.*
- [10] V. Roger, *et. al.* “Contact Resistances in the Cold Bypass Diode Leads of the Main LHC Magnets”, *IEEE Trans. Appl. Supercond.*, vol. 24, no. 3, Jun. 2014, Art. ID. 4802504.
- [11] R. Denz, D. Hagedorn. “Experimental Analysis and Modeling of the Electrical and Thermal Transients of the Diode-By-pass for the LHC- Magnet Protection at Cryogenic Temperatures” *LHC Project Report 268, Presented at ICEC98, Bournemouth, UK, 2009.*
- [12] G. Willering. “Private communications” *CERN.*