DESIGN, DEVELOPMENT AND INITIAL RESULTS OF SOLID STATE MAGNETRON MODULATOR

Abhijit R. Tillu#, Shiv Chandan, Kavita Pramod Dixit, Kailash Chander Mittal, Hemant Sarukte
Accelerator & Pulse Power Division, Bhabha Atomic Research Centre,
Mumbai - 400085, INDIA

Abstract

A prototype solid state pulse modulator based on Induction Adder Topology has been designed and is currently being tested on an S Band Pulsed magnetron rated for 3.2MW Peak RF Power. After successful lab tests the modulator is intended for use in cargo scanning and radiography applications. Currently the topology consists of 4 nos. of single turn primaries driven independently at voltages not more than 1000V. The secondary encircles all the four primaries to generate the desired pulsed voltage across the magnetron. The designed output pulse parameters are 50kV, 120A, 4 micro s, at a pulse repetition rate of 250 pps. The paper describes the design and development of the Epoxy Cast Pulse transformer and the Low Inductance Primary Circuit. The rise time measured was < 400ns, and the reverse voltage at the end of the pulse was less than 12kV (at 43k V pulse). The testing was done at low PRF, on two different magnetrons having different operating points to demonstrate fairly good impedance independent operating characteristic of the magnetron modulator. Initial test results on the Resistive load and Magnetron load will also be discussed.

INTRODUCTION

Various low power linear electron accelerators designed for cancer treatment, radiography, cargo scanning and related applications use pulsed magnetrons as RF Source. The magnetrons are typically rated for 3.2MW peak RF Power and 3kW average RF Power. 1000's of such machines are available worldwide. The pulse modulators required to power these magnetrons are traditionally Line type-modulators. Though these modulators are very rugged, they are being replaced by Solid state modulators due to various reasons which are elaborated in various references [1, 4, 5, 6]. The paper describes a solid state magnetron modulator being developed in our lab. The output specifications towards with the modulator is designed are listed in Table 1.

The design of the modulator is based on Induction Adder Topology, also referred to as Split Core topology or Matrix Adder Topology [1, 3, 4]. The topology has been chosen over other solid state topologies mainly because it is much compact as compared to other competing topologies, and the gate drives and control logic need not be floating at HV.

tillu@barc.gov.in

Table 1: Output Pulse Specifications

Output Pulse Voltage	-52kV
Peak Current	120A
Pulse width	4µs (flat top)
Rise time	<400ns
Backswing	< 5kV
Pulse Droop	< 1%
Pulse to Pulse Stability	<1%
Max Pulse Repetition Rate	250 pps

DESIGN

The peak electrical power delivered to the magnetron per pulse is ~6MW. The modulator is designed for at-least 8MW of pulse power. There Split core pulse transformer has four primaries independently driven by their respective power modules. Each module is a 1kV pulse source implemented as shown in fig 1. The IGBT used is a 1700V, 2400A IGBT (ABB make 5SNA 2400E170100). The 200µF/1100V energy storage capacitor is implemented by two Vishay make Axial type Metalized polypropylene Capacitors GLI 1100-100A. The electrical connections between the IGBT, Capacitors and diode are implemented by low Inductance strip line geometry.

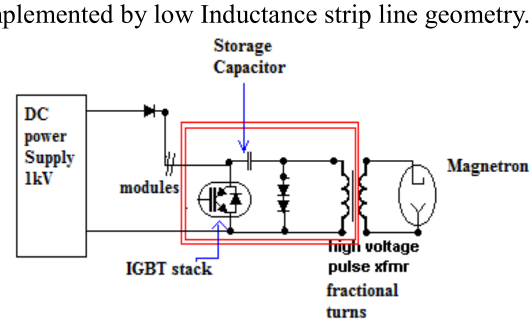

Figure 1: Conceptual schematic of the Pulse Modulator.

The split core pulse transformer also referred as fractional turns transformer has four primaries, each implemented by using a single turn foil winding of 0.3mm thick Copper. The secondary consists of 14 turns of SWG16. The secondary is in bifilar type, so as to allow filament heating power to the magnetron. There are 8 turns of Reset winding on the secondary, implemented by using SWG14 enamelled copper wire. The entire secondary is adequately screened and epoxy potted, so as to allow Oil Free construction of the pulse transformer. The pulse transformer core uses 4 pairs of Amorphous Cut C cores (2605SA1). Each core is excited by its own primary. The cores are arranged such the transformer is in E type configuration. The modelling in CST EM Studio is shown in Fig 2. The estimated flux swing is ~ 1,5T. Hence the cores are biased at ~ 0.75T, so as to get the best

ISBN 978-3-95450-142-7

pulse permeability. The pulse permeability of the core was evaluated separately and was confirmed to be ~ 3500 for the required flux swing, if the core is biased at ~ -0.75T.

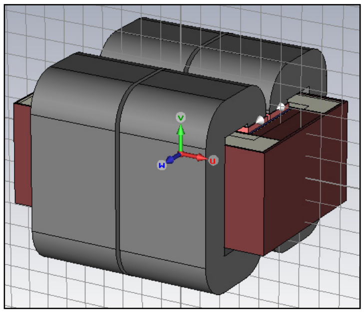

Figure 2: CST EM Studio model of Pulse Transformer.

The Capacitor charging power supply charges the storage capacitors to the set voltage (1KV max). The freewheeling diode has been implemented by using a series combination of diodes such that the volt-second instability doesn't saturate the core. The gate drive circuit for improved short circuit protection is in advanced stage of implementation. The results generated using commercially available Gate Drives.

Estimation and Measurement of Circuit Parameters

The main challenge of this modulator topology is implementation of primary circuit with extremely low stray series inductance, and low leakage inductance of the pulse transformer. This is many times at the cost of increased distributed capacitance, and shunt circuit capacitance. The Pulse transformer leakage Inductance, and the Distributed Capacitance were estimated using Analytical formulas [2, 3, 6], and CST EM Studio. They were verified with Low Voltage Measurements. Primary Circuit stray Inductance was also measured. The results are listed in Table 2. The equivalent circuit of the modulator as seen by one of the modules is as shown in fig 3.

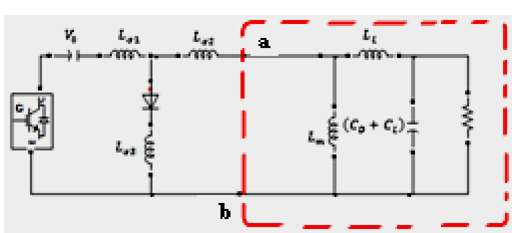

Figure 3: Equivalent circuit of split core pulse modulator.

When the modulator is not loaded (secondary Open Circuited), the pulse transformer is highly under-damped and hence, the output has significant ringing. The period of which is determined by the Series Inductance and the Shunt Capacitance. The Series Inductance is the combination of pulse transformer leakage inductance and stray primary Inductance. The Capacitor is the Distributed capacitance as seen by one fraction ($4n^2 C_{D\ sec}$). The Pulse Transformer is loaded by a known capacitance in the secondary (50pF and 100pF in this case), and the shift in resonance frequency is noted. Hence the estimations are experimentally verified. Fig 4 shows the pulse transformer output without any capacitive loading and with 50 pF loading. As seen the damped oscillation period without ant loading is 500ns, and with 50pF loading is 592ns. The damped oscillation frequency is approximated as fundamental oscillation frequency for all practical considerations. The probe capacitance (~3pF) need not be considered, as the capacitance being measured is at-least two orders of magnitude higher and the error introduced is negligible.

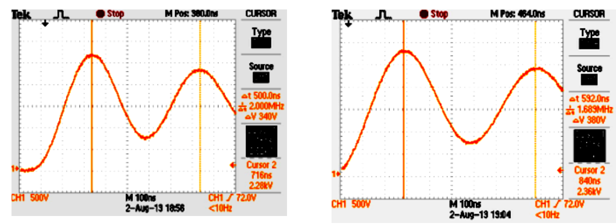

Figure 4: Voltage waveform of pulse transformer at no load and 50pF Loading respectively.

The Region encircle in red in Fig 3 is the equivalent circuit representation of the pulse transformer. A voltage probe connected across node a and b, gives a signature of voltage division between the stray primary circuit Inductance, and the pulse transformer leakage inductance. Hence the stray primary inductance is also estimated.

Table 2: Measurement of Pulse Transformer Parameters

Transformer parameters	Theoretical Estimation	CST EM Results	Measured values
Leakage inductance (L_l)pri	29.21nH	25.36nH	26.9nH
Distributed capacitance(C_D)sec	118.59 pF	123.08 pF	127.3 pF

The waveforms shown in Fig 4 suggested a series inductance of ~ 63.5nH. From the voltage waveform across Node a-b, the primary circuit stray Inductance is estimated to be 36.5nH. The distributed capacitance tabulated in Table 2 is as seen from the secondary, and the leakage Inductance is as seen by each primary. There is a scope of error of ~ 20% but it is not affecting the design, as the interest is to ensure that the series inductance is lesser than certain value, and accurate knowledge of stray inductance is not necessary.

Testing

The Prototype pulse modulator was assembled and tested on a resistive load of 400Ω. It was ensured that the ESL of the load is very low (<1µH). The Fig 5 shows the view of the test setup. The DC voltage was increased upto ~ 550V. The maximum Pulse Voltage was measured to be 30kV, at 545V. The Rise times measured was < 300ns and the backswing is negligible. When the Pulsed voltage was increased from 10kV to 30kV the rise time did not change

ISBN 978-3-95450-142-7

significantly. It was tested at higher voltages also but the probe was removed as the limitation of the probe is 40kV. Fig 6 shows the waveform on the resistive load at 15kV and 30kV.

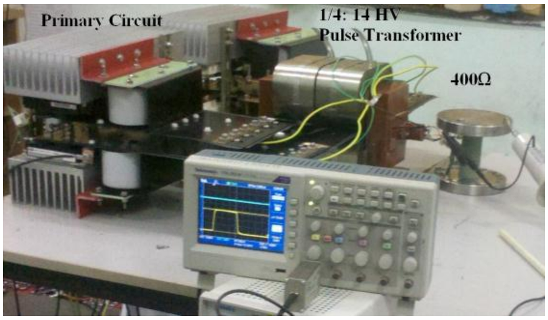

Figure 5: Testing on Resistive Load.

After this testing the modulator was subjected to ARC Testing and it was confirmed that the maximum voltage across the switch is within 1.3kV during IGBT Turn OFF in ARC Condition.

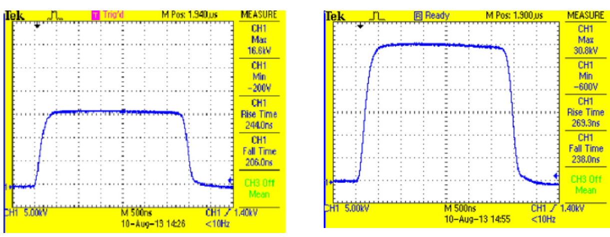

Figure 6: Modulator output across resistive load at 15kV and 30kV pulse Voltage.

With this testing concluded the modulator was connected to the e2v make magnetron MG5028. The electromagnet current of the magnetron was set for 130mT Field in the magnetron, This corresponds to the operating point of 38kV/ 168A. The magnetron output was terminated on a waterload, and the waveguide line consisting of one directional coupler was pressurised with ~ 20 psi of SF6. The filament was heated at the rated parameters and the pulse voltage was slowly increased.

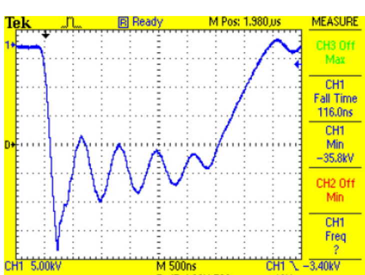

Figure 7: Modulator output at voltage much lower than Hulls Cutoff

At Voltages much below the Hulls Cutoff, the magnetron offered very high impedance, and hence the output showed significant ringing, as shown in Fig 7. As the magnetron pulse voltage was increased further the magnetron current increased and the pulse shape improved significantly, as indicated in Fig 8. The magnetron was tested upto ~34kV, 100 A and the peak RF Power was measured to be ~ 1.6MW maximum using Diode Detectors

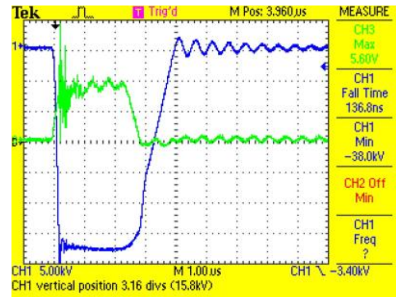

Figure 8: Modulator Output on e2v magnetron MG5028.

Fig 8 indicates a rise time < 350ns and backswing of ~3kV. The e2v make magnetron was in regular use and hence well conditioned, hence there were no ARC events. The testing was done upto 30pps for around 15 min and the pulse shape was stable. The blue waveform (Ch 1) in Figure 8 is the magnetron voltage and green waveform is the magnetron current. The setup was used for conditioning of buncher linac. The e2v make magnetron was disconnected and the FAZA make 2.7MW magnetron MI456A was connected to the modulator. It has an operating point of 55kV/100A. With this magnetron testing was done up-to 43kV, 70A pulse. The magnetron required some conditioning and there were ~ 8 ARC events, but the modulator did-not indicate any damage.

FUTURE SCOPE

Commercially available gate drives were used for this testing. These commercially available Gate drives were slightly modified to restrict the ARC current, however they are not suitable. An improved Gate Drive has been designed, fabricated and is being tested. The CCPS for the modulator has been designed and is under fabrication, Water cooled heat sinks will be used for more compactness, and based on the results, we may finally freeze the design to 2 IGBTS only.

CONCLUSION

Indigenous design and development of a Proof of Principle Solid State Modulator has been successful. It has been tested on actual magnetron Load and the required rise time has been achieved. It is also concluded that the modulator performance is largely load independent, as the modulator was successful tested on two different magnetrons. The experience gained is very useful for the development of similar modulators for higher power klystrons.

ISBN 978-3-95450-142-7

REFERENCES

[1] S. Roche, "Solid State Pulsed Power Systems", Physique and industries.
[2] "Design Procedure for Compact Pulse Transformers with Rectangular Pulse Shape and Fast Rise Times" D. Bortis, J. Biela, G. Ortiz and J.W. Kolar Power Electronic Systems Laboratory, ETH Zurich
[3] "Transient Behaviour of Solid State Modulators with Matrix Transformers", D. Bortis, J. Biela, and J. W. Kolar Power Electronic Systems Laboratory, ETH Zurich
[4] "A new Solid State High Power Pulsed Modulator", Walter Crewson et. al.
[5] "Klystron Power Supplies, Modulators and Testing" Saul Gold, SLAC klystron Lectures
[6] "Pulse Generators", G.N. Glasoe, J.V. Lebacqz, McGraw-Hill

ISBN 978-3-95450-142-7