Development of FPGA-based Predistortion-type Linearization Algorithms for Klystrons within Digital LLRF Control Systems for ILC-like Electron Accelerators

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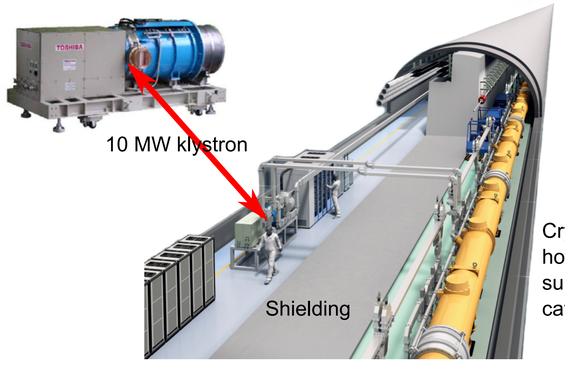
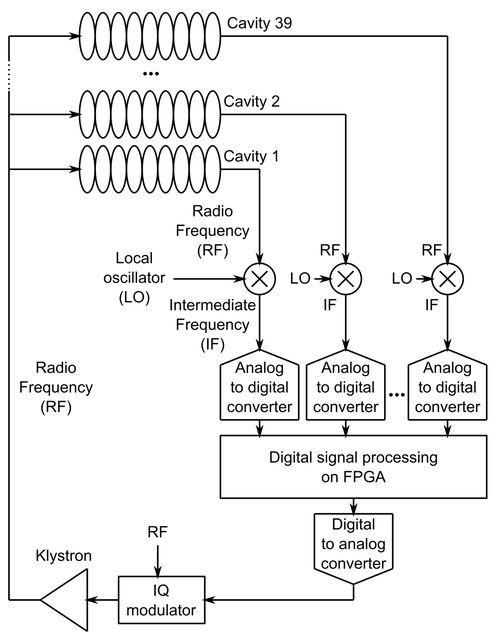
Introduction

At the International Linear Collider (ILC) [1] the superconducting 9-cell TESLA type L band cavities will be driven in a configuration of 39 cavities per 10 MW klystron [2].

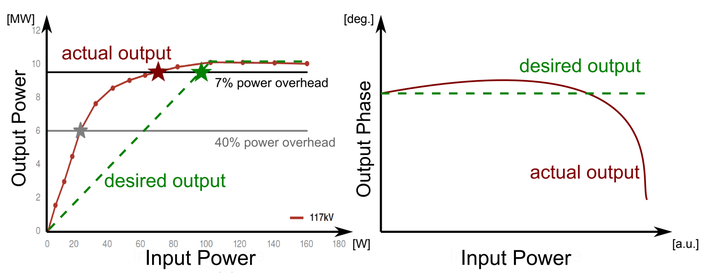


Schematic of possible ILC tunnel layout [2].



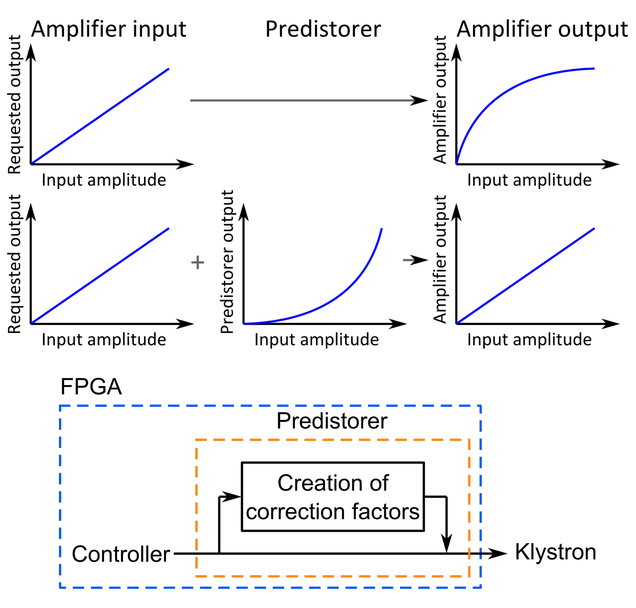
Simplified schematic of the digital LLRF control loop for ILC.

For cost optimization reasons it is intended to operate the klystrons 7% in power below their quench limits [2]. Klystrons are non-linear devices.



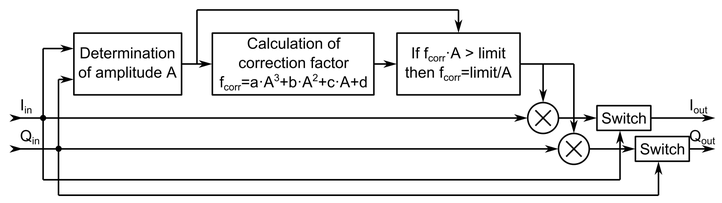
Schematic of the klystron output characteristics.

The feedback gain is proportional to the klystron output amplitude characteristic. Close to operation the gain decreases and makes control difficult or even impossible. This situation can be overcome by the implementation of a klystron linearization, which linearizes the klystron output and keeps the control gain constant up to the point of saturation. In the following the development of predistortion-type FPGA-based linearization algorithms is described [3].

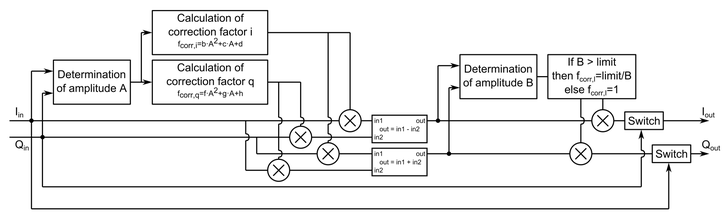


General principle of a predistortion-type FPGA-based klystron linearization algorithm.

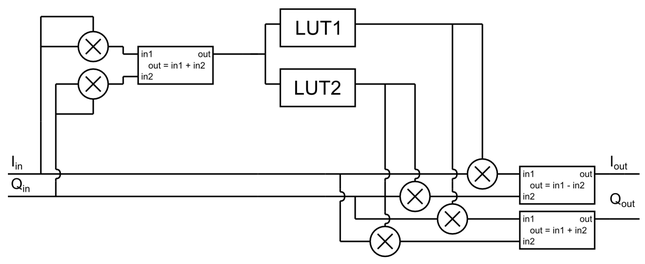
Linearization Algorithms



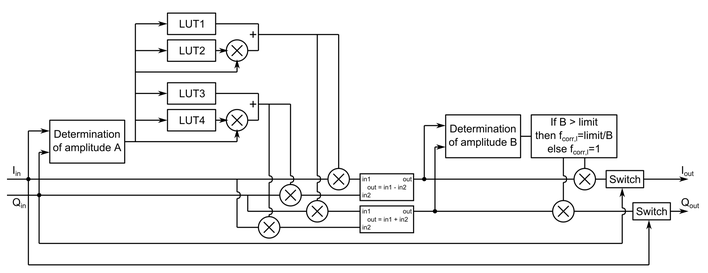
3rd order polynomial function based algorithm [4].



2rd order polynomial function based algorithm.



Direct lookup table based algorithm [3,4]*.



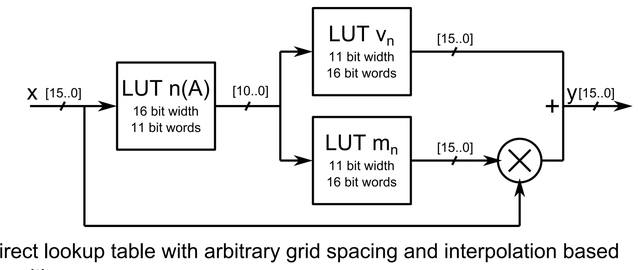
Direct lookup table with interpolation based algorithm.

Test of Algorithms

	3nd order	2rd order	Direct LUT	LUT w/interp.
Target FPGA	Altera Cyclone II	Altera Cyclone II	Xilinx Kintex 7	Altera Cyclone II
Test method	Klystron	Klystron	Simulation	Klystron
Test result	Successful	Proof of concept	Successful	Proof of concept
Amp. and pha. linearization	Amplitude only	✓	✓	✓
Quantization	✗	✗	✓	✗
Precision	Good	Good	Very good	Best
Memory usage	Low	Low	High	High
Multiplier usage	High	High	Low	Low
Total loop delay added	1 clk	3 clks	3 clks	3 clks

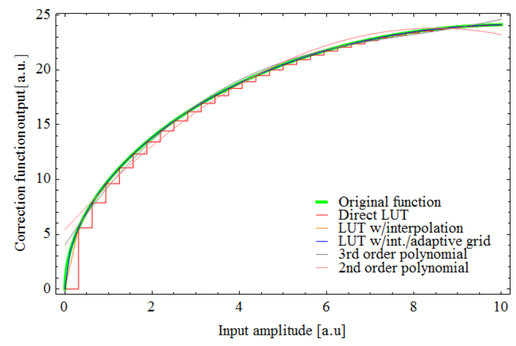
Algorithm of choice: Two lookup tables with linear interpolation:
- Linearization in amplitude and phase
- No quantization
- Best precision

Improvements possible? Yes!

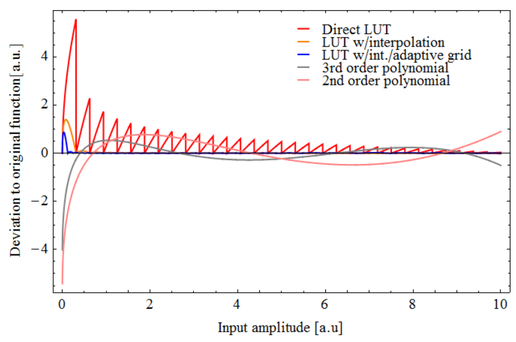


Direct lookup table with arbitrary grid spacing and interpolation based algorithm.

Performace Comparison



Modeling simulation of an arbitrary function (green) for all introduced linearization algorithms.



Error functions in modeling an arbitrary function for all introduced linearization algorithms.

Algorithm of choice: Lookup tables with arbitrary grid spacing and interpolation:
- Best modeling performance (lowest total error)
- Requires only 1 clk more than the LUT w/int.

Conclusion

Five different algorithms for klystron linearization have been developed. Three of those were successfully tested using an actual 5 MW klystron. In a modeling performance simulation of all algorithms it was shown that the algorithm based on lookup tables with arbitrary grid spacing and interpolation yielded the best result. By the implementation of such a linearization algorithm the ILC requirement of klystron operation 7% in power below the point of saturation will be satisfied. Furthermore this kind of klystron linearization can be applied to any other accelerator or application at which high efficiency RF usage is required.

References

[1] http://www.linearcollider.org
[2] "The International Linear Collider - Technical Design Report - Volume 3.II: Accelerator Baseline Design", CERN, FNAL, KEK (2013).
[3] W. Cichalewski, "Linearization of Microwave High Power Amplifiers in the RF Systems of Linear Accelerators for FLASH and X-FEL", (PhD Thesis), Technical University of Lodz, Lodz (2008).
[4] M. Omet, "Development and Test of Klystron Linearization Packages for FPGA-based Low Level RF Control Systems of ILC-like Electron Accelerators", Proc. RT2014, Nara (2014).

Acknowledgements

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