SYNCHRONOUS DEVICE INTERFACE AND POWER SUPPLY CONTROL SYSTEM AT NSLS-II *

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Abstract

A new approach to embedded device control is being developed by Lawrence Berkeley Laboratory (LBNL) and Brookhaven National Laboratory (BNL). Synchronous device interface (SDI) will be implemented in NSLS-II project as a key communication protocol. This paper describes the design motivation and principles of SDI. It also discusses SDI in fast orbit feedback system and its extension in power supply control system.

INTRODUCTION

An accelerator consists of many distributed subsystems and lots of physics variables need to be transmitted. Some variables are required to be distributed by deterministic and fault tolerant protocol with low latency. A typical example is fast orbit feedback (FOFB) system. In a FOPB system, beam position monitor (BPM) data at various locations are required to be distributed so that beam transverse coordinates along the ring can be used to calculate optimal corrector magnet settings to correct the beam deviation. Typically a fast orbit feedback system is required to work in KHz range. Various fast communication protocols were developed to meet the FOFB requirements [1].

We are designing a new fast communication protocol called synchronous device interface (SDI). The main motivation of SDI is to distribute data around NSLS-II storage ring with minimal distribution latency and with fault tolerance. SDI will be the fast communication protocol for BPM data in the FOFB system. SDI will also be extended to the power supply control system, where power supply controllers (PSC) and cell controller form a ring network for power supply data distribution.

SDI is designed with configurable machine parameters and it can be easily adapted to other accelerators. Moreover, SDI will be an open-source design so that other accelerators can benefit from SDI design of NSLS-II.

SYNCHRONOUS DEVICE INTERFACE

Design Motivation

At NSLS-II, an exceedingly stable photon beam is essential for the high brightness and small beam size requirements. In the common case of 1:1 focusing optics, photon beam position stability is directly related to electron beam position stability. At NSLS-II, the requirement for electron beam motion is less than 10% of beam size. This is a common tolerance used by many synchrotron radiation laboratories. This requirement translates to 0.3µm electron beam position stability in the short straight section. To achieve such a stringent requirement, a fast orbit feedback system is necessary.

Figure 1 shows the NSLS-II fast orbit feedback system. It consists of BPMs, cell controller and corrector power supply controllers. As the central part of the FOFB system, a cell controller performs the following major functions:

1) Collects BPM data in the cell (up to 8 RF BPM and 4 XBPM for NSLS-II).
2) Distributes the local BPM data to other cells and retrieves other cells' BPM data.
3) Calculates the optimal corrector settings in the cell based on all BPM readings.
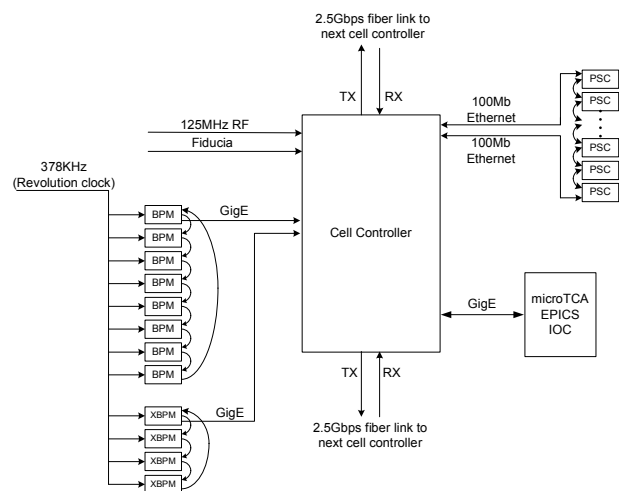4) Sets corrector power supplies with new setpoints.

Figure 1: NSLS-II fast orbit feedback system in on cell.

These are common tasks for a typical orbit feedback system. Among them, 1), 2) and 4) are communication related and ideally they can all use SDI as a reliable and low latency protocol. At NSLS-II, SDI will be used for data distribution between cells (function 2) and power supply controllers (function 4).A BPM vendor provides a proprietary protocol to group local BPMs together and to send the data to cell controller through Gigabit Ethernet. We are working with the BPM vendor to implement SDI as the communication protocol between BPM and cell controller (function 1). In the following paragraphs we use cell-to-cell data distribution (function 2) to demonstrate some of the advanced features of SDI protocol [2].
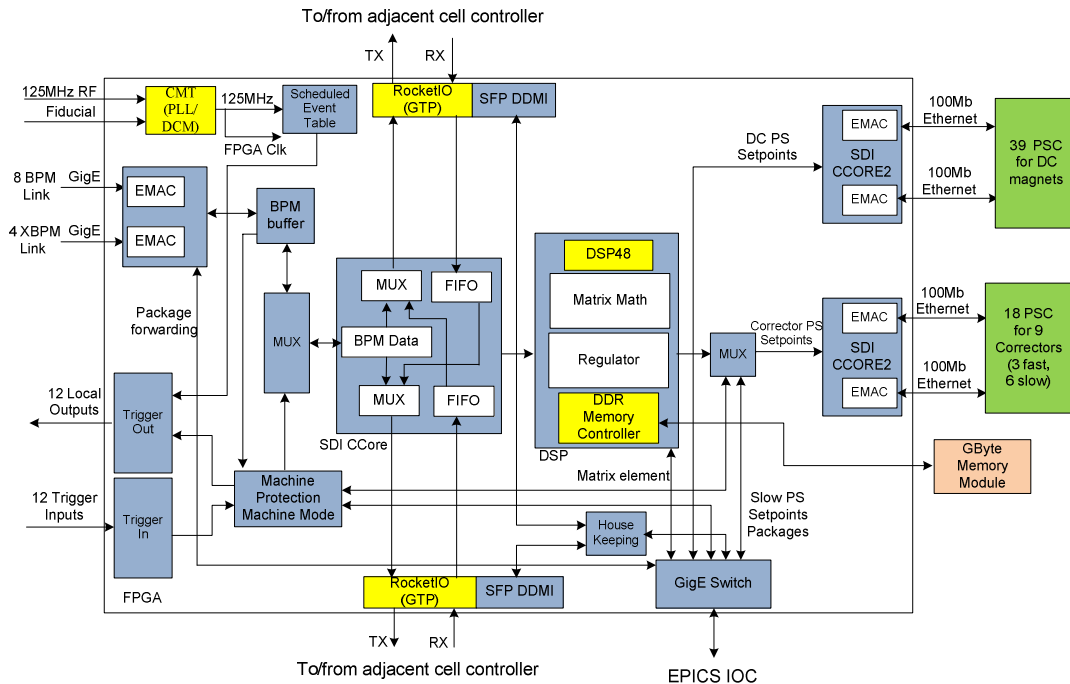
Figure 2: Cell controller structure.

SDI Protocol

The 30 cells in NSLS-II storage ring are connected by fiber links to form a ring network (versus a centralized approach in a star topology). One cell controller is designated master, the rest being slaves. All cell controllers have instinct capacity of becoming master or slave, and the protocol contains mechanism for both time synchronization and auto configuration. Data transmission is through time-division multiplex mechanism: each cell controller put its own data into the links in its time slot and passes through the data in other time slots. There are two links carrying the data in opposite directions to ensure fault tolerance.

Figure 2 shows the detailed structure of a cell controller. The left side of the figure shows the local BPM datapath. The middle of the structure is the SDI communication core (ccore), which manages the distribution of BPM data through the 30 cells. A DSP block is shown as the calculation engine for the new corrector power supply setpoints. The right side of the figure shows that the new corrector power supply setpoints are delivered to each power supply controller through SDI links using 100Mbit/s Ethernet link.

SDI communication core (ccore) has the control logic of cell-to-cell SDI link. It manages the RocketIO GTP transceivers, the time-division multiplex scheme for transmitting/passing through BPM data into the ring, and the switch to fault recovery operation mode. Ccore uses a elastic FIFO to save the received data and to transmit the data out in the corresponding time slots. The FIFO length is auto configured, depending on the cell controller ID assignment.

Latency

SDI latency depends on the data size in each cell, total cell counts and system bandwidth. For NSLS-II, the first two parameters have fixed values. SDI uses the latest low cost RocketIO transceiver to increase the system bandwidth and therefore reduce the latency.

As shown in Figure 2, each cell controller has two Xilinx RocketIO GTP transceivers, which are highly configurable and provide minimized, deterministic datapath latency. At NSLS-II, they are configured to transmit and receive data at 2.5Gbit/s (effective rate of 2Gbps with 8b/10b encoder) rate. SFP connectors and multimode fiber are used to connect adjunct cells.

Table 1: SDI link data size and latency

Data Per BPM (byte)	Data Per Cell (byte)	Total Data (byte)	Latency
10 (X:4; Y:4; Status:2)	120 (10B/BPM *12BPMs/cell)	3.6K (120B/Cell *30 Cells)	14.4us (3.6KB/2Gbps)

Table 1 gives the data size and the data distribution latency for NSLS-II FOFB system. It takes 14.4us to distribute all the BPM data to each cell controller. For a 10KHz FOFB system, it leaves more than 85% of bandwidth for other data distribution. Since SDI provides a redundant and deterministic data distribution with low latency, it is desirable to use the remaining bandwidth to distribute other important data around the storage ring. Figure 2 shows that machine protection data, machine

state data, or local triggers can be put on the SDI link. As NSLS-II control system develops, other data type support might be required for the SDI link. The current SDI and cell controller architecture has enough flexibility and capacity for future expansions.

Synchronism

Since there are 30 cells around the 780 circumference ring, it is desirable to synchronize SDI protocol with the same clock. For many acceleration applications, a synchronized design brings a lot of benefits [3]. For synchronous light source, the natural choice for the common clock is the RF frequency, which directly provides RF bucket information.

The master RF oscillator at NSLS-II has a frequency of 499.98MHz. A 125MHz clock (in sync with RF master clock) will be distributed through NSLS-II accelerator complex. Such distribution paves the way to design a totally synchronous subsystem. SDI protocol is one example. As shown in Figure 2, all the 30 cell controllers use the same 125MHz clock to drive the communication port and the FPGA logic. Therefore, SDI protocol is both synchronous and deterministic.

Fault-Tolerant

During SDI ring network initialization, each cell controller is assigned an ID number according to its relative location to the master. In normal operation mode, data circulates in one direction and data is introduced into the link according to the ID assignment. When a link (or a pair of links) between two cell controllers is broken, the backup link is used to keep connectivity between any pair of cell controllers in the ring. If this event arises, the system falls into the fault recovery operation mode. In the fault recovery operation mode, the system has localized the broken link and re-configured automatically to maintain connectivity using backup link.

The communication system maintains synchronism and connectivity through both the main and the backup links in normal operation mode. When a failure is detected, the system re-configures automatically and each cell controller determines which link needs to be used to retrieve BPM data from the ring. The BPM data distribution is abstracted from upper application levels, and therefore corrector setting calculations are not altered when the system falls into the fault recovery operation mode. The fault is identified by the system, and error flags are delivered to the operator level.

SDI IN POWER SUPPLY CONTROL

NSLS-II Power Supply Control

There are 10 quadrupole magnets, 10 sextupole magnets, 6 slow correctors and 3 fast correctors in one cell at NSLS-II. There are 57 power supplies for these magnets. Since cell controller is the key control module of the FOFB system and it has high bandwidth connection to control IOC, it has advantages to also use cell controller as the control unit for power supply control system.

Various communication approaches (such as VME, RS485) have been used in power supply control system in other facilities. As discussed above, SDI provides many advanced features for data distribution, naturally we are extending the concept of SDI to power supply control system.

The power supply SDI ring network consists of power supply controllers, cell controller and the 100Mbit/s Ethernet links between them. It is a pure cost reason to choose 100Mbit Ethernet link instead of fiber links to run SDI protocol. Compared with other serial link technologies, Ethernet is a low cost, well developed and hopefully long lasting technology.

Since corrector power supplies update rate is different from that of DC power supplies, there should be two power supply SDI links. We decided to connect all corrector power supply controllers in one SDI link, and to connect all multipole magnet power supply controllers in another SDI link. The configuration is shown on the right side of Figure 2.

Power Supply SDI Link

Power supply SDI link has a bandwidth of 100Mbit/s. The cell controller put setpoint data onto the link and power supply put its readback data onto the link. The link will also be synchronized with RF frequency. Therefore, we are pushing the synchronism down to power supply system. High level physics applications will benefit from a fully synchronized system which includes BPM, cell controller and power supplies.

Power supply SDI link provide redundant and fault-tolerant communication for power supply control system. Implementing SDI protocol into power supply control system will help to improve accelerator system reliability.

CONCLUSIONS

SDI protocol is being developed as a generic synchronous, deterministic and fault-tolerant data distribution solution. It will be used in NSLS-II fast orbit feedback system and power supply control system. As an open source design, it can be easily adapted to other facility as a low cost, high speed communication protocol.

REFERENCES

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