TUNE MEASUREMENT SYSTEM UPGRADE WITH FPGA-BASED TECHNOLOGY AT THE APS*

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Abstract

The Advanced Photon Source (APS) has three circular machines: a 7-GeV electron storage ring (SR), a booster synchrotron (booster) that ramps the beam energy from 325 MeV to 7 GeV, and a particle accumulator ring (PAR). Their tune measurement systems are based on HP 4396 network and spectrum analyzers (NASA) and HP 89400 vector spectrum analyzers (VSA). The instruments are no longer supported by the vendor and need replacement in the future.

An upgrade of these systems with FPGA-based processors has been implemented. The new systems provided faster tune history and bunch-by-bunch tune reading in addition to the functionality of the original systems. We present a brief description of the implementation and performance of the new systems.

INTRODUCTION

FPGA-based tune measurement systems have been implemented in the APS storage ring (SR), booster, and the particle accumulator ring (PAR) [1]. The relevant parameters for each of the rings are listed in Table 1.

Table 1: Machine Parameters Relevant to Tune Measurement

	SR	Booster	PAR
Cycle time T (ms)	cw	226	500
Damping time τ_x,τ_y (ms)	9.6, 9.6	2.69, 2.69 (7 GeV)	20, 25
Nominal tunes υ_x,υ_y	36.2, 19.3	0.35, 0.2	2.17, 1.27
Rev. freq (MHz)	0.271	0.813	9.773
Beam charge (nC)	3.68 to 60	0.5 to 6	0.5 to 6
Required tune RBW	0.0001	0.005	0.005
Chromaticity ξ_x, ξ_y	6, 7	0 to 2.0	0 to 1.0
Short-term tune shift	0.0005	0.02	0.02

Tune measurement can be done in many different ways, but typically involves an analyzer and a chirper. The chirper excites beam oscillations, and the analyzer acquires and processes data. Beam signal can be time-captured and processed by FFT analysis or digital demodulation. The chirper can be a single-frequency sweeping source, a pinging source, or a source with mixed frequency and timing characters. The operation of the chirper and the analyzer must be synchronized with each other in order to maximize tune detection. We wanted to design a system that was flexible and configurable to fit the different characters of each of the three APS rings. On the chirper side the system incorporated three different types of sources: a trigger output for the external drive, an internal chirper that can generate periodic frequency ramping or FM modulation, and a slow-sweeping frequency source. On the data acquisition and processing side we used both the FFT time capture method and digital demodulation method analysis with a predetermined frequency.

FPGA MODULE

Figure 1 shows a block diagram of the FPGA unit [2] that consists of a StratixII DSP processor board [3] and a timing-Coldfire daughter board. The timing-Coldfire board provides system clock and synchronization trigger input. A Coldfire processor board provides network connection and EPICS [4] interface to the APS controls network.

The DSP processor has two 12-bit A/D converters, two 14-bit DAC converters, and as many as 41 logic I/O bits. We use the two A/D channels for x and y tune signals, the DACs for internal chirping, and two of the I/O bits for ping output to external devices.

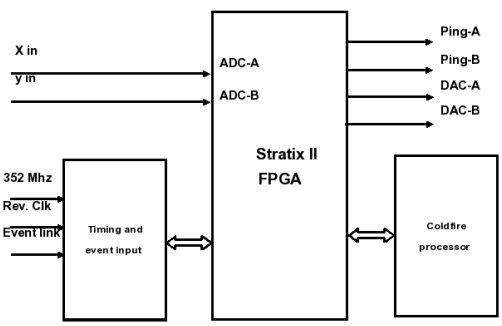

Figure 1: Block diagram of the tune measurement FPGA module.

TUNE MEASUREMENT FIRMWARE

Figure 2 shows a block diagram of the tune measurement firmware. The ADC block acquires input values from the 12-bit A/D coverters at 117.33 MHz, or

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one third of the storage ring rf frequency. The DC part is removed and a Hanning window is applied to the data before FFT processing. FFT is performed with a record length of 2048. Finally, peak detection is performed to extract tune peaks from each FFT record. Several waveform process variables [4] are produced for each input channel: an ADC waveform that contains 1024 continuous samples, turns waveform that contains 262144 turn-by-turn raw samples, and an FFT waveform that contains up to 128 FFT traces.

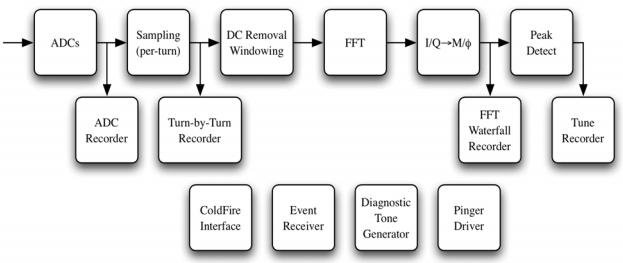

Figure 2: Block diagram of the tune measurement firmware.

SR TUNE SYSTEM

The APS SR has strong chromaticity in both the horizontal and vertical planes, and the beam has a large tune spread. The signal of transverse centroid motion damps within ~150 turns, which is much shorter than the transverse damping time of the ring. This is mainly due to the decoherence of the large tune spread. In order to achieve good tune measurement, a continuous chirping is applied.

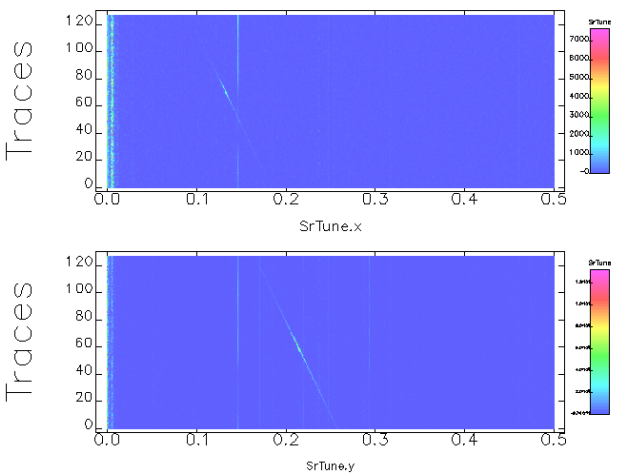

Figure 3: Contour plot of tune measurement result of APS storage ring. Total time is about 1 second.

Beam is excited by either an external source -- in this case a HP6396A network analyzer -- or internal chirping sources of the DAC output. The beam response is down-converted with a mixer circuit to baseband for sampling. Sampled data is either processed by FFT or digital demodulation. In the FFT mode the FFT record length is 2048 turns with a resolution bandwidth of 0.001. In the demodulation mode the resolution bandwidth is 1/1000 of the span or 0.0005, whichever is larger. Figures 3 and 4 show some of the measurement results.

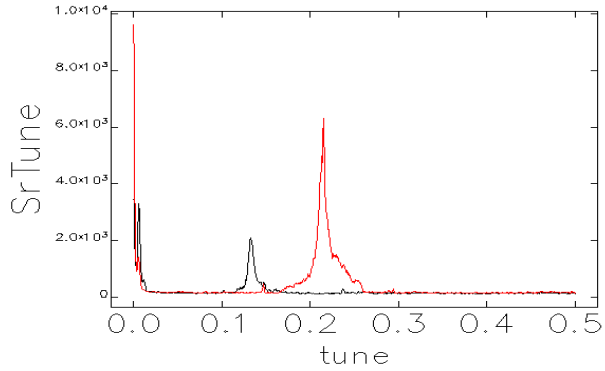

Figure 4: Storage ring tune plot (black trace: x tune, red trace: y tune).

BOOSTER TUNE SYSTEM

The booster synchrotron has a totally different character compared with the SR. The goal of the tune measurement system is to achieve a time resolution of a few ms with a tune resolution of 0.01. Because of the energy ramping, the tunes shift due to imperfect current ramping of the magnets. Damping time changes from a few seconds to a few ms during the full ramping cycle. This makes a frequency sweeping source impractical. Pinging with a pulsed supply is more appropriate in this case. Two pulsed supplies are used to ping the beam with two striplines, one for the vertical plane and one for the horizontal plane. Figure 5 shows a diagram of the booster tune measurement system.

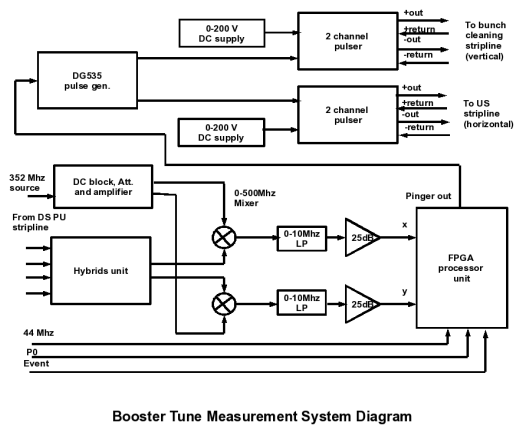

Figure 5: Block diagram of booster tune system.

The pinger is designed in-house and has a maximum output voltage of 2700 V and a maximum repetition rate of 600 Hz. Each pinging produces one FFT record. A maximum of 128 records can be acquired during one booster synchrotron cycle. The tune peaks detected from each FFT record are also available as waveform process variables. Figure 6 shows tune plots of both horizontal and vertical planes and figure 7 shows a plot of tune peaks waveform.

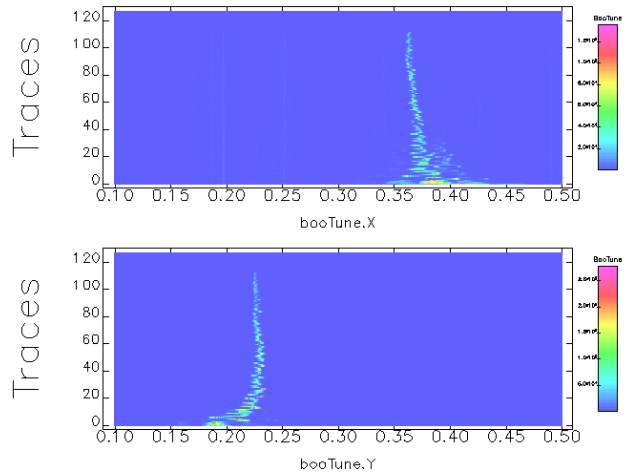

Figure 6: Contour plots of booster tunes (top: x tune, bottom: y tune).

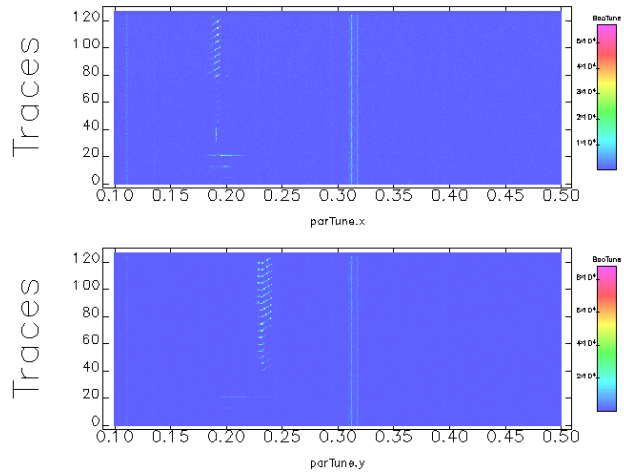

Figure 8: Contour plot of PAR tune history during a cycle (top: x tune, bottom: y tune).

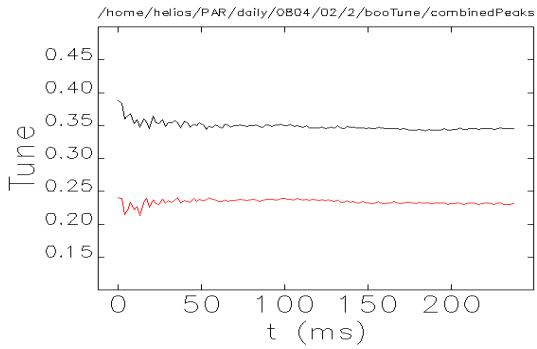

Figure 7: Peaks waveform of booster tunes (black trace: x tune, red trace: y tune).

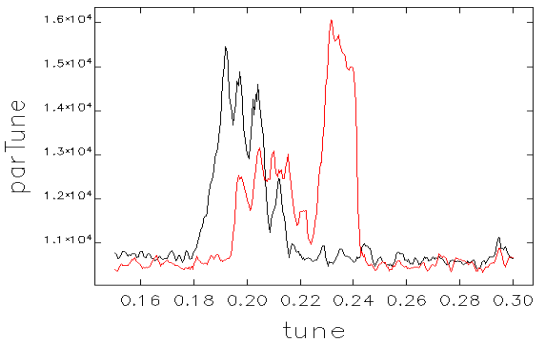

Figure 9: Plot of measured PAR tunes (black: x tune, red: y tune). The lower peaks are from injection perturbation.

PAR TUNE SYSTEM

The PAR system is very similar to the booster tune measurement system. The system shares a driver stripline with the PAR bunch cleaning system. A Stanford Research DS345 arbitrary waveform generator is used to excite beam externally. The generator is triggered by a pinging output of the FPGA unit. We tested various waveforms, including FM, frequency ramping, random noise, and pinging. They all work when proper repetition frequency and strength are applied. Before the harmonic capture the signal is relatively weak due to the long bunch length. Figures 8 and 9 shows some measurement results.

CONCLUSIONS

We developed a general FPGA-based tune measurement system that works well for the APS storage ring, the booster synchrotron, and the PAR. The system can be further expanded to including multibunch capabilities.

ACKNOWLEDGMENTS

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