DESIGN AND ANALYSIS OF A MIXED-SIGNAL FEEDBACK DAMPER SYSTEM FOR CONTROLLING ELECTRON-PROTON INSTABILITIES*

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Abstract

An electron-proton (e-p) instability is observed with increased beam intensity at the Spallation Neutron Source (SNS) in Oak Ridge National Laboratory (ORNL). This paper presents a wide-band, mixed-signal system for active damping of the e-p instability. It describes techniques used for feedback damping, data acquisition, and analysis. The paper also describes analysis strategies to monitor system performance. The mixed-signal feedback damper system includes anti-aliasing low-pass filters, power amplifiers (PAs), analog-to-digital converters (ADCs), reconfigurable field programmable gate array (FPGA) hardware and digital-to-analog converters (DACs). The system will provide feedback damping, system monitoring, and offline analysis capabilities. The digital portion of the system features programmable gains and delays, and equalizers that are implemented using parallel comb filters and finite impulse response (FIR) filters. These components perform timing adjustments, compensate for gain mismatches, correct for ring harmonics, and equalize magnitude and phase dispersions from cables and amplifiers.

INTRODUCTION

An electron-proton instability is observed with increased beam intensity in SNS at ORNL. In this instability, the low-energy electron cloud is confined within the space-charge potential of the proton beam. Coupled transverse oscillations of the beam and the trapped electrons can lead to instable, coherent motion of the beam and possible beam loss [1]. Figure 1 demonstrates that an e-p instability occurs in the SNS accumulator ring.

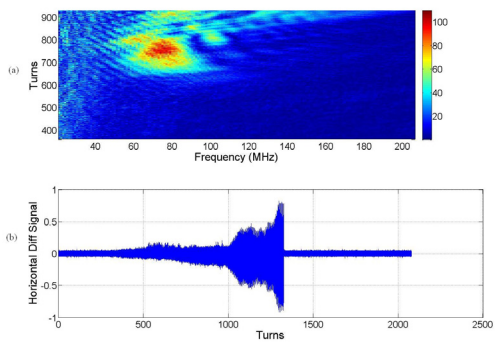

Figure 1: (a) Turns vs. Frequency (MHz) with intensity depicted as a color; (b) Instability evolution over time, Data courtesy of Z. Liu.

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To ramp up the power and compensate for the instability in the SNS ring, we implement a wide-band, mixed-signal system for active damping of the e-p instability. The design is based on previous work on feedback damping instabilities in the PSR (Proton Storage ring). This analoge system[2], working at up to 300 MHz, has limitations such as less flexibility and lack of programmability, which can be overcome by a mixed-signal solution. The mixed signal system is more flexible, and can be used to monitor and control the proton beam in a storage ring or a synchrotron accelerating ring.

MIXED-SIGNAL SYSTEM DESCRIPTION

The feedback damper system, shown in Fig. 2 consists of a Triton FPGA card designed by TEK Microsystems [3] and a LabVIEW [4] workstation. Two operating modes are supported by the system: operational mode and research mode.

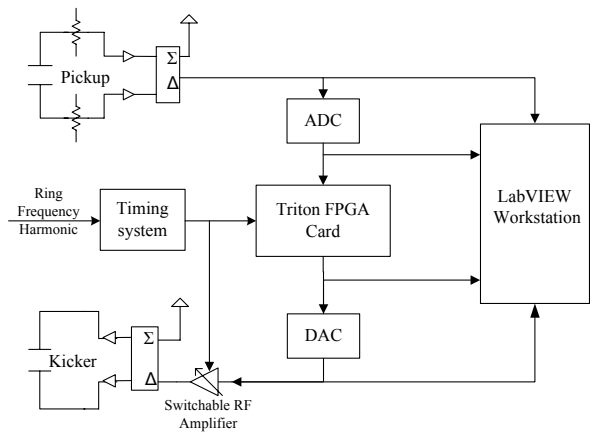

Figure 2: Schematic of the overall system.

In operational mode, the FPGA board captures data from the pickup, processes the data and feeds data back to the kicker. Simultaneously, the workstation monitors the data from four sources: (1) Signal from the pickup, (2) Signal before the FPGA, (3) Signals after the FPGA, and (4) Signal passed to the kicker. A LabVIEW program on the workstation monitors the signals from these data sources and checks the consistency between each pair of signals. If there is any data inconsistency, an alarm is raised and the Triton FPGA stops sending data to the DAC. The program also monitors the digital clock manager on the FPGA to maintain a stable clock, which is essential in the system.

The Triton FPGA card lies between the ADC and the DAC. It implements a programmable digital gain, a programmable delay (FIFO) up to five microseconds, two comb filters capable of zeroing out the entire ring

harmonic spectra, and an equalizer in the form of a Finite Impulse Response (FIR) filter. A schematic of the system on the FPGA with its peripheral components is shown in Fig. 3.

In research mode, the workstation runs a LabVIEW program that facilitates interaction between the user and the FPGA card. All reconfigurable parameters on the FPGA board, such as the gain multiplier and the filter coefficients can be reconfigured in real-time in this mode. The user can opt to store and analyze both the original data from the pickup and kicker and the processed data from the FPGA. A flexible neuro-fuzzy controller is being developing that can intelligently adjust the FPGA parameters and reduce the need for human intervention.

Programmable Delay

The feedback system guarantees the signals that get to the kicker are timed correctly. This requires that the delay maintains a phase difference of -90 to 90 degrees between the pickup and the kicker. The digital delay is designed as a programmable FIFO and it can be updated anytime in either operating modes.

Comb Filters

The beam position monitor (BPM), working as a pickup, inherently obtains the instability signal and the beam revolution frequency with its harmonics. These spectral powers dominate the majority of the total power input to the system.

To reduce the power that the system handles and to improve the resolution of instabilities, it is desired that the feedback damper system not act upon the beam revolution frequency and its harmonics. Therefore, the technical requirement for this system is to place poles at the beam revolution frequency and its harmonics. Comb filters, whose frequency response consists of a series of regularly-spaced spikes, suffice for this task. The comb filter is designed in a feed-forward form in Fig. 4.

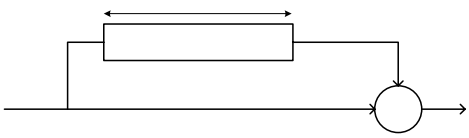

Figure 4: Schematic of a Comb filter.

The frequency response of the comb filter is depicted in Fig. 5. This comb filter is capable of cancelling those frequency components at an integer multiple of the ring revolution frequency, which is 1 MHz in this measurement.

Equalizer

The equalizer is important because the electrodes have non-uniform gain versus frequency, the cables have magnitude and phase dispersion, and the amplifiers have phase dispersion. Designing an equalizer to cancel the phase dispersion improves the system performance by decreasing a power loss by about 10%. In our system measurement, the overall phase dispersion of the cables and electronics is about 22 degrees across the band.

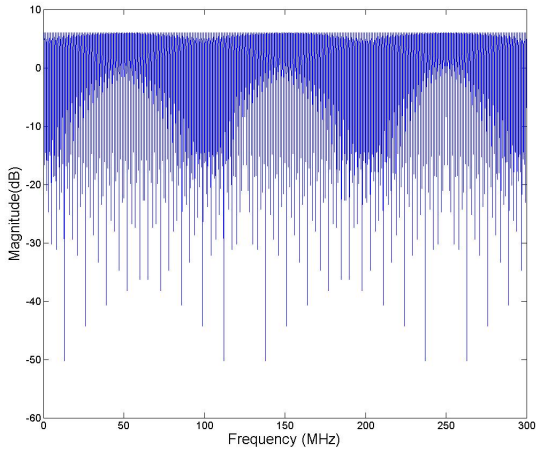

Figure 5: Transfer function of the comb filter.

The FIR equalizer coefficients are calculated based on measurements from a vector network analyzer. A program has been developed for calculating the coefficients, which are based on the transfer function of the system. The impulse response of a typical equalizer in our system is shown in Fig. 6.

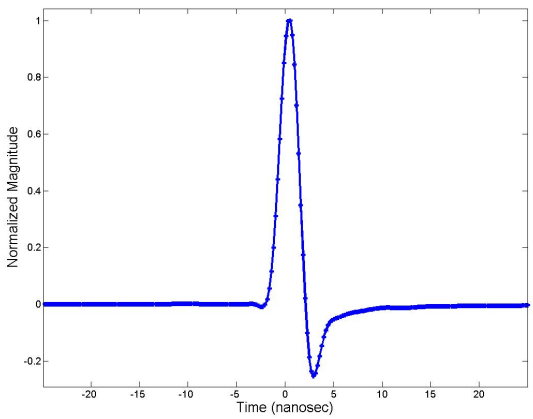

Figure 6: The impulse response of a typical equalizer.

Since the damper system is broadband, it is the most computationally intensive module in the overall design. A schematic of a conventional FIR filter is depicted in Fig. 7. To implement the FIR filter with 256 taps, a 16-channel parallel FIR filter requires a total of 1296 taps. The FPGA card (model XC2VP70 [5]) has 328 multipliers and it is far less than the multiplier requirement for the 16-channel parallel equalizer. To reduce the computational complexity, the multipliers are replaced by lookups into pre-computed tables. Because the inputs to a multiplier are normally two 8-bit fix-point numbers and one of them is constant, a 256-entry by 16-bit table is used to replace each multiplier and the variable input is used to address the table. This technique greatly reduces the number of multipliers needed by utilizing the block random access memory (RAM) in the FPGA.

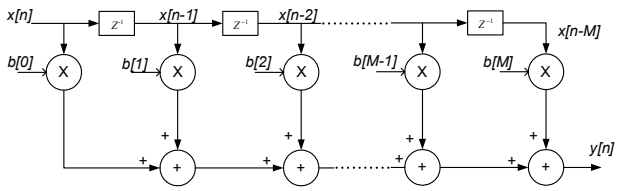

Figure 7: The conventional FIR filter schematic.

Digital Clock Manager

The digital clock source, controlled by a Digital Clock Manager (DCM), must be perfectly synchronized to the ring frequency for the mixed-signal damper system to function. For the SNS system, the frequency of the digital clock for both the ADC and DAC is envisioned to be a factor of 1600 higher than the ring frequency. The clock jitter, skew and any other problems related to clock synchronization is minimized via the clock manager.

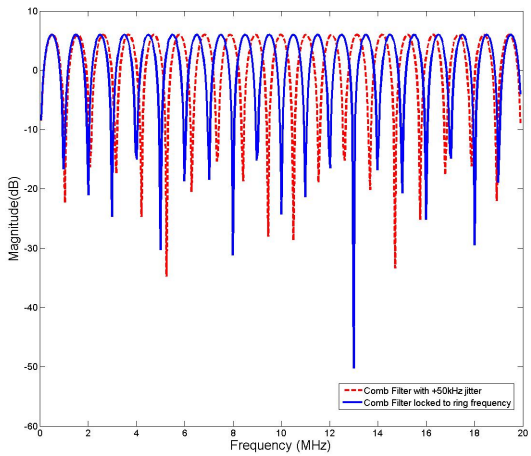

Figure 8: Comparison of the frequency response of a comb filter locked to 1 MHz versus a comb filter with 50 kHz of clock jitter.

If the clock is not locked and there is clock jitter, the comb filters will not function properly. Consider an example where the ring frequency is 1 MHz and the DCM provides a clock at 125 times the ring frequency to the FPGA. If there is a ring frequency jitter of 50 KHz, the clock input to the FPGA is 131.25 MHz instead of 125 MHz. Figure 8 compares the frequency response of the same comb filter with a locked clock and a clock with a jitter of 50 KHz. As can be observed from the figure, without accurate locking of the clock, the comb filters will not function properly.

CONCLUSION

An electron-proton instability is observed with increased beam intensity at SNS. To ramp up the power and compensate for the instability in the SNS accelerator, we are implementing a wide-band, mixed-signal system for active damping of the e-p instability. The system consists of one FPGA card and a LabVIEW workstation. Two operating modes are supported: operational mode and research mode. The digital portion of the mixed-signal feedback damper system and its components has been designed with Verilog HDL and simulation tests have been run. To achieve a high performance, a 16-channel parallel implementation has been developed. The individual components and the system have been tested using Verilog HDL and MATLAB Smodels. The next step is to develop the control program and fine-tune the system for timing accuracy.

REFERENCES

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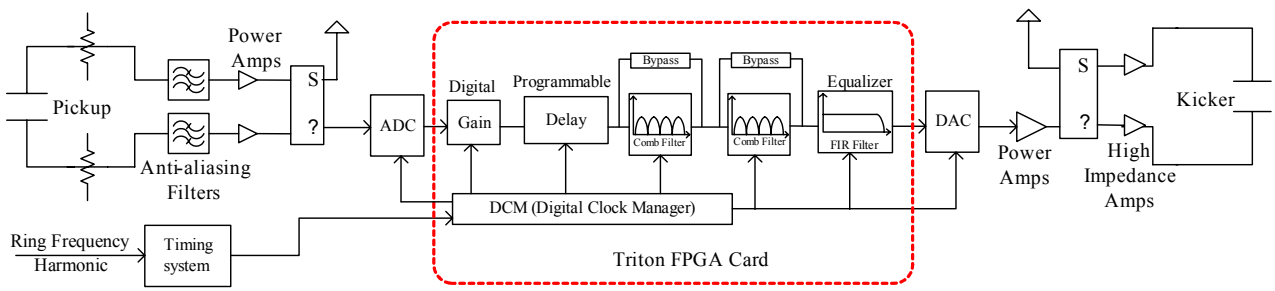

Figure 3: Schematic of the FPGA based system. Digital gain, delay, comb filters can be bypassed individually.