

DESIGN AND TEST OF 10 KW RF AMPLIFIER BASED ON DIRECT DIGITAL SYNTHESIZER*

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Abstract

A 10 MeV cyclotron (CYCHU-10) has been developing in Huazhong University of Science and Technology (HUST). As a RF power amplifier is needed to provide 10 kW continuous-wave (CW) to the resonance cavity in CYCHU-10, some designs and experiments about the RF amplifier have been accomplished. A method of picking up a special aliased signal of DDS output as the target RF signal is adopted in our study. The chip AD9850 is used to synthesize RF signal in the system, and the amplitude modulation of the system is achieved by adjusting the external connection resistor's value of the chip. The output frequency is tuneable from 98.5 to 99.5 MHz. The principles and experimental results of the signal synthesizer will be presented. The driver amplifier consists of two solid-state modules, which can provide the final stage amplifier with up to 300 W of input power. The final stage amplifier based on a tetrode operates in the grounded cathode configuration, and short-circuited coaxial transmission lines are introduced in the resonant circuits. The preliminary design of the tetrode circuit will also be detailed in this paper.

INTRODUCTION

A compact cyclotron CYCHU-10 has been developing in HUST. Due to the space limit within magnetic poles, there is not an automatic frequency tuning equipment in the resonance cavity, so the magnetic field will alter synchronously according to the resonant frequency of cavity. The designed average magnetic field is 1.63 T, the H⁻ revolution frequency is 24.8 MHz, and the cyclotron adopts 4th harmonic acceleration, so the resonant frequency of cavity is 99.2 MHz at this time [1]. The thermal analysis of the cavity shows the resonant frequency drift is lower than 1MHz, so a RF amplifier is required to deliver 10 kW power to the resonance cavities at 99 MHz with 1 MHz bandwidth. Main specifications of RF power amplifier are listed in Table 1.

Table 1: Main Specifications of RF Power Amplifier.

Parameter	Value
Rated Power Output	10 kW
Frequency Range	98.5~99.5 MHz
Frequency Stability	10 ppm
Output Impedance	50 ohms

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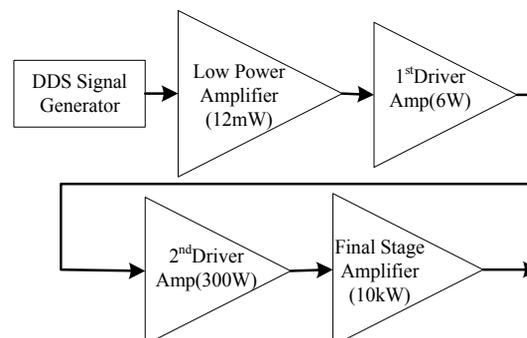


Figure 1: Scheme of RF power amplifier system.

The prototypes of the signal generator and driver amplifiers have been developed. The scheme of RF amplifier system is shown in Figure 1. The signal generation board integrates the DDS circuit and low-power amplifier. The DDS circuit can achieve the flexible output frequency tuning, and trace the resonance frequency rapidly. The driver amplifiers adopt two solid-state modules, providing the final power amplifier with up to 300 W of input power. In addition, the final stage amplifier based on tetrode technology takes the grid drive. The screen grid maintained at RF ground prevents capacitive feedback from anode to the grid. Thus it minimizes the chance of self-oscillation of the tetrode amplifier [2].

SIGNAL GENERATOR

Phase-Locked Loop (PLL) and DDS devices are popular in signal generator along with wide application of digital technology. Account for the long tuning time and low frequency resolution relative to the DDS technology [3], the PLL doesn't meet the requirement of a flexible frequency tuning system, so the DDS is the best choice to fulfil the flexible output frequency tuning.

Synthesis Principle

The reference clock frequency of DDS will be higher than 200 MHz in order to synthesize a RF signal at 100 MHz directly in theory. Therefore, a high performance DDS chip must be utilized in the signal generator which chooses the fundamental signal of the DDS output as the target signal. Whereas, the method of picking up a special aliased signal of DDS output can also achieve the aim of generating a fine RF signal at low expenses. In our signal generator prototype, a chip AD9850 is used to synthesize

RF signal introducing the method mentioned above.

The AD9850's innovative high speed DDS core provides a 32-bit frequency tuning word, which achieves an output tuning resolution of 0.0291 Hz under a 125 MHz reference clock input. The chip allows the output frequency up to one-half of the reference clock frequency, so the output frequency can reach up to 62.5 MHz that is lower than our expected frequency around 99 MHz. Nevertheless, the output sine wave of the DDS device is reconstructed by the internal high speed D/A converter, so the output of the AD9850 is a sampled signal, and its output spectrum follows the Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental and aliased images that occur at multiples of the reference clock frequency plus/minus the selected output frequency [4]. Figure 2 shows a graphical representation of the sampled spectrum.

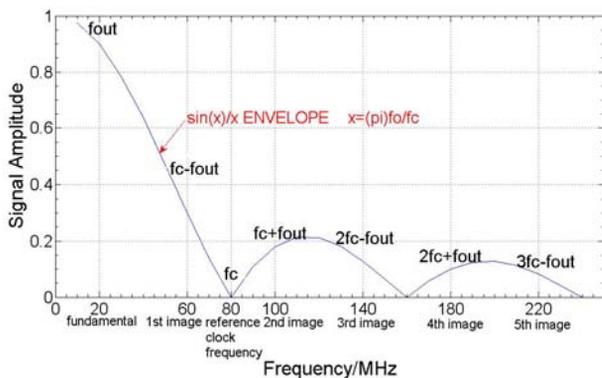


Figure 2: Output spectrum of a sampled signal.

In this sampled spectrum, the reference clock is 80 MHz and the output frequency is set to 20 MHz. As can be seen, the aliased images are very prominent and of a relatively high energy level as determined by the $\sin(x)/x$ roll-off of the quantized D/A converter output [4]. Consequently, we can pick up a specific aliased signal of its output as our desired signal by several band-pass filters and amplifiers.

Signal Generator Desktop Experiment

In our prototype, the reference 80 MHz clock is generated from a precision high stable ± 0.5 ppm quartz oscillator. The output frequency of AD9850 is set to 19 MHz, so the second image of output is 99 MHz which meets our expected signal frequency. Three band-pass filters and low power amplifiers are placed alternately behind the DDS output to suppress the fundamental and other aliased signals sufficiently.

Figure 3 shows the output of DDS chip and three band-pass filters from top to bottom. As far as we can see, the No.1 waveform is the fundamental signal of 19 MHz with notable aliased signals. The band-pass filters inhibit the fundamental and other aliased signals gradually as shown in the figure. Finally, the signal is delivered to the driver amplifier via a low-pass filter. The final output waveform

is presented in Figure 4. The stability of output frequency can reach up to 10 ppm.

In addition, the amplitude modulation of the RF system can be achieved by adjusting the external connection resistor's value on the pin 12 of AD9850. This resistor value (R_{set}) sets the internal DAC full-scale output current (I_{out}) [4]. The relationship is presented in equation (1).

$$I_{out} = 39.936 / R_{set} \quad (1)$$

In the above expression the current is in A, and the resistor is in Ω .

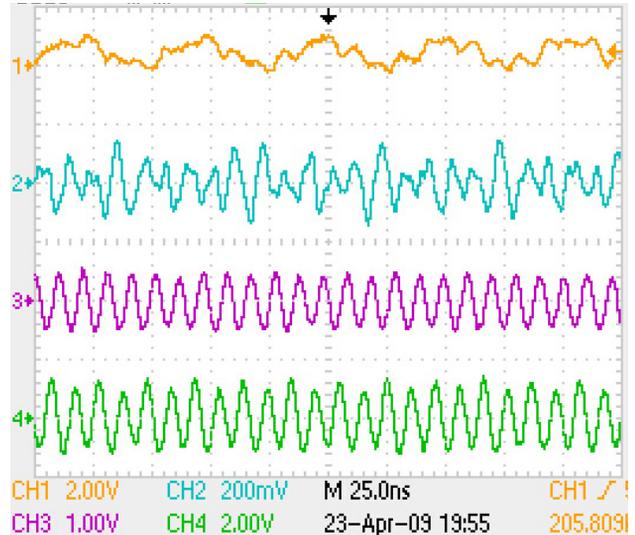


Figure 3: Waveforms in the signal generator.

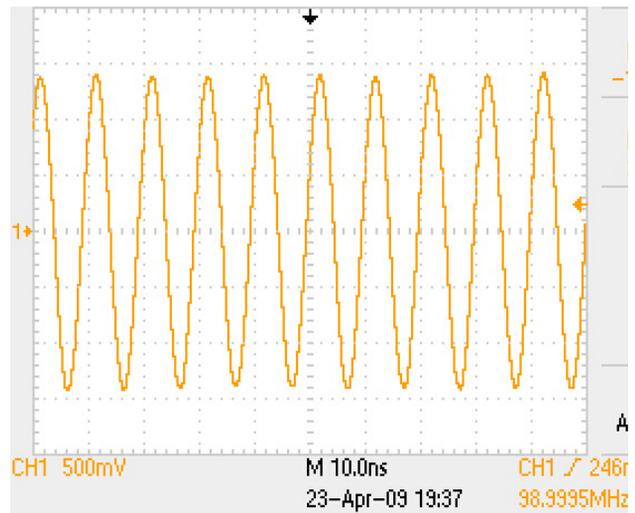


Figure 4: Final output waveform of the signal generator.

DRIVER AMPLIFIER

The output power of signal generator can reach up to 12 mW, so we choose the available modules MDF30-R and FM310-108 to provide up to 6 and 300 W of power, respectively. A 7 dB attenuator is inserted between the signal generator and the module MDF30-R to realize power match, because the power gain of MDF30-R is 34 dB generally. For the same reason, the other attenuator is

placed between two modules. Figure 5 shows the general view of driver amplifier modules.



Figure 5: General view of driver amplifier modules.

TETRODE CIRCUIT DESIGN

A tetrode 4CW10000B is selected to operate in the grounded cathode configuration in the final stage amplifier. It's capable of delivering up to 10 kW CW power to the resonance cavity at around 99 MHz. The screen grid bypass circuit includes eight 1000 pF copper-clad kapton capacitors [5]. Figure 6 shows the schematic of the tetrode circuit.

Considering the low impedance and high current density requirement, both the input and output resonator adopt short-circuited $\lambda/4$ coaxial transmission structure. The length of short-circuited transmission line ' ℓ ' is estimated by $\ell = \lambda/2\pi \tan^{-1} X_C/Z_0$, X_C is the impedance value of short-circuited transmission line at resonance [2].

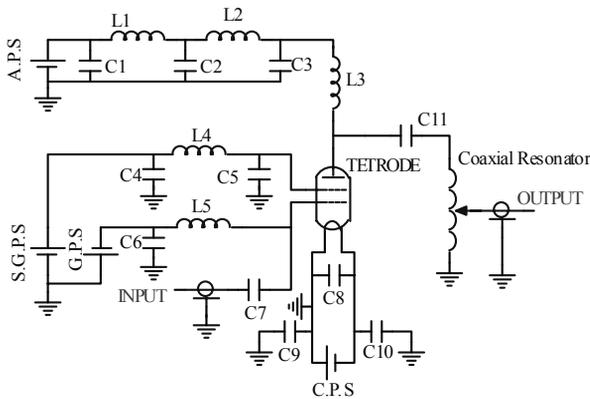


Figure 6: Schematic of the tetrode circuit.

The coupling loops are connected to the short-circuited transmission line directly, like an autotransformer (see Figure 7). This structure can achieve impedance transformation by itself, so the input and output impedance can be matched by regulating the rate of coupling part correctly. Therefore, it's a very simple coupling structure for tetrode circuit in practice.

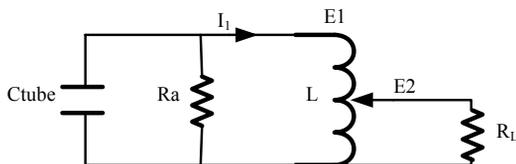


Figure 7: Equivalent circuit of anode resonator.

The Q values of resonance circuits must be considered carefully in the design. A low Q value brings a wide bandwidth, and results in the increase of the power consumption at the same time. Due to the finite plate dissipation, the Q value of anode resonator can't be high generally, and it must be lower than that of the grid resonator in design.

CONCLUSIONS

With the method of picking up a special aliased signal of DDS output, a kind of general performance but widely used DDS microchip can be utilized to generate the desired RF signal. A chip AD9850 is used in our signal generator to realize the frequency tuning and amplitude modulation, and the experimental results demonstrate that the method is feasible.

Two available solid-state modules are chosen in the driver amplifier to provide the tetrode with up to 300W input power. The preliminary design of the tetrode circuit is illustrated. The tetrode amplifier operates in the grounded cathode configuration, and short-circuited coaxial transmission lines are adopted in both the input and output resonator. The further simulation and experiment will be carried out.

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