352-MHZ SOLID-STATE RF POWER SYSTEM DEVELOPMENT AT THE ADVANCED PHOTON SOURCE*

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Abstract

An investigation into development of a 200-kW cw solid-state rf power system design to replace the existing klystron-based 352-MHz rf systems at the Advanced Photon Source has been started. The baseline 352-MHz solid-state system design will consist of multiple 1-kW cw modules combined to produce a total output capability of 200-kW cw, sufficient to drive one single-cell storage ring cavity. A description of the 1-kW cw module building block of the solid state power system will be presented, along with results from hardware evaluation tests at the 1-kW cw level.

INTRODUCTION

The Advanced Photon Source (APS) presently uses five 352-MHz, 1-MW cw klystrons as rf power sources, one for the booster and four for the storage ring. Cost, lifetime, and long-term availability issues with these klystrons have motivated investigation into the possibility of replacing the present klystron-based rf systems with a solid-state equivalent. In addition, it is expected that a solid-state rf system design would provide cleaner rf power with less phase and amplitude distortion, which will improve accelerator beam stability and require less maintenance over time than the existing klystron-based systems.

It was decided that a novel approach to solid-state power implementation would be to develop a 1-kW amplifier module using one solid-state output device, thereby reducing combining losses in a larger system composed of multiple 1-kW amplifier modules. A commercial solid-state device was selected for testing and evaluation at the 1-kW cw output level.

PROPOSED APS SOLID-STATE RF SYSTEM

The APS storage ring presently utilizes sixteen single-cell rf cavities, driven in two groups of eight cavities by four separate 1-MW cw klystrons. Preliminary design options for a solid-state rf power conversion involve possibly operating the storage ring with fewer rf cavities, opening the opportunity to drive each rf cavity with a stand alone 200-kW cw rf system rather than distributing the divided output of a single klystron over eight cavities, as is presently done. Using the storage ring beam as the final power combiner would further reduce combining losses. The conceptual 200-kW rf system would consist of 200 1-kW linear amplifier modules, with the modules grouped in 20-kW combiner stacks, 10 of which are combined to produce the 200-kW total output power applied to each rf cavity. The solid-state system would utilize the existing APS 32.2ºC deionized water system for cooling, and occupy approximately 1,200 watts per square foot of floor space. The 1-kW modules would include an on board circulator and termination, a 300-volt to 50-volt DC-DC converter for input power, on board diagnostics, and occupy no more than 1,600 cubic inches.

352-MHZ/1-KW CW TEST AMPLIFIER CONSTRUCTION AND TEST SETUP

Two 352-MHz/1-kW cw test amplifiers were constructed for the purpose of understanding the thermal issues involved with producing 1-kW cw output from a single solid-state device package, and to determine if a safe output device temperature could be maintained with a cooling water supply at 32.2ºC. The Freescale™ MRF6VP41KH LDMOS rf power transistor and 352-MHz evaluation circuit were chosen as the test platform, and two copper cold plates were fabricated to provide enhanced water cooling for the transistor package and the amplifier circuit board and passive components. Two MRF6VP41KH devices were “de-lidded” by Freescale™ and provided for these tests so that the actual transistor die temperature could be measured during operation using an infrared camera to determine the cooling efficiency of the cold plate. One amplifier was constructed with the output transistor package “clamped” to the cold plate using screws and a thermal grease junction between the transistor flange and the cold plate. The second amplifier was constructed with the transistor package soldered directly to the copper cold plate for maximum heat transfer and electrical contact. Figure 1 shows the assembled test amplifiers.

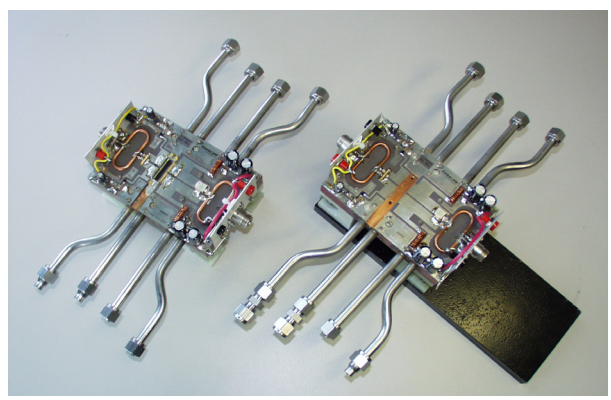

Figure 1: Assembled 352-MHz test amplifiers.

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The cold plate design was optimized to minimize the peak die temperature of the output device using a cooling water supply equal to or greater than room temperature in order to prevent condensation on the coldest parts of the amplifier assembly. Thermal finite element analysis (FEA) performed on the cold plate design (see Figure 2) indicates that dual water channels containing wire-coil insert heat transfer enhancers [1] positioned directly under the output device will meet the design requirements, allowing the transistor package to be maintained at acceptable temperature levels while utilizing room-temperature cooling water with a flow rate at or below 1 gpm per channel.

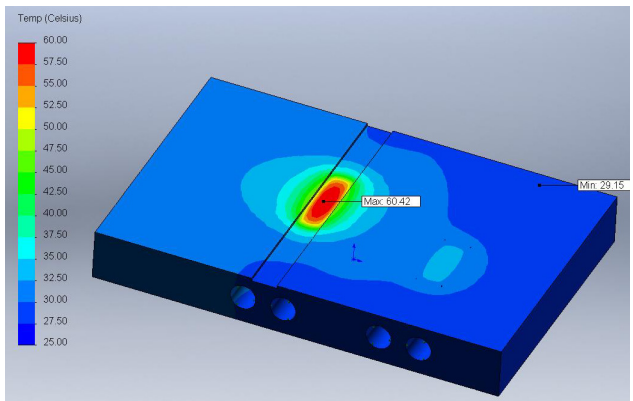

Figure 2. The results of FEA.

The prototype cold plates were machined with dual cooling channels directly under the transistor mounting position and through the center area occupied by the output matching network, with heat-transfer-enhancing coils inserted in each channel for maximum thermal efficiency. Flow and temperature of the cooling water was measured on all water circuits to provide accurate calculation of calorimetric power coupled to the cold plate. A photo of the amplifier test setup is shown in Figure 3.

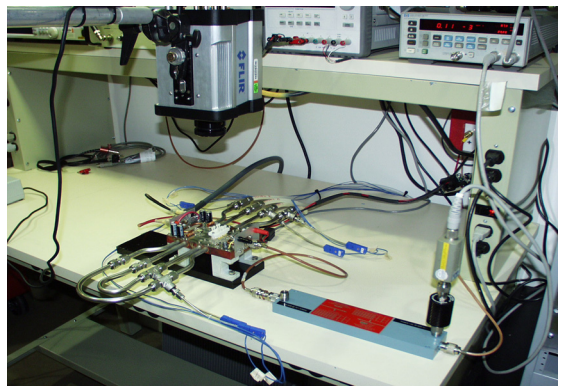

Figure 3: Amplifier test setup with IR camera viewing transistor die.

AMPLIFIER PERFORMANCE

Both test amplifiers produced approximately 1-kW cw output power at 351.93 MHz and demonstrated efficiency and rf gain consistent with published MRF6VP41KH performance data. Supply water temperature was approximately 25.8ºC for the first round of tests. As expected, the thermal performance of the "clamped-transistor" assembly was significantly less than the "soldered-transistor" assembly, with the clamped transistor die temperature reaching a peak of 210.7ºC after five minutes of operation at approximately 909 watts cw output power. However, the soldered-transistor amplifier die temperature ran much cooler, peaking at 136ºC after sustained operation at 1-kW output power. This die temperature translates to an estimated transistor mean-time-to-failure (MTTF) of 9 million hours. Performance data from the soldered-transistor amplifier is shown in Table 1.

Thermal performance of the soldered-transistor amplifier is detailed in the IR camera image shown in Figure 4. The data clearly show that the transistor is

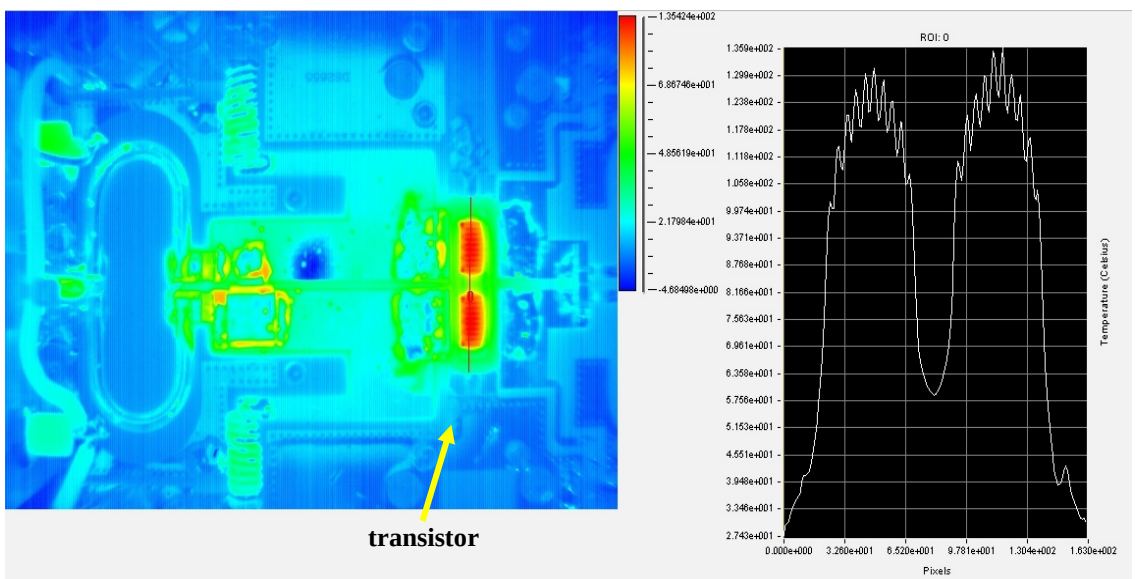

Figure 4: IR camera thermal image of soldered-transistor amplifier operating at 1-kW cw output power.

Table 1: Soldered Transistor Amplifier Data

Test frequency	351.93 MHz
Pout rf	1,000 watts cw
Pin rf	8.32 watts
RF gain	20.7 dB
Input return loss	10.07 dB
Pin DC	1,509.82 watts
Efficiency	66.2%

operating well within thermal limits and can be expected to operate at the 1-kW cw output level continuously without problems. Peak operating temperature data from the IR camera versus output power for the soldered-transistor amplifier are provided in Figure 5.

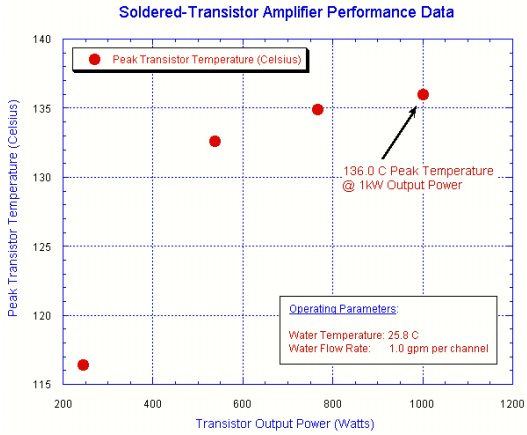

Figure 5: Peak operating temperature vs output power for the soldered-transistor amplifier.

FUTURE PLANS

Further testing of the existing clamped and soldered-part amplifiers will be conducted to determine the minimum amount of water flow required to maintain tolerable transistor die temperatures, and to test a 1-kW cw design. Additionally, the construction of prototype 352-MHz pre-driver, driver, and 1-kW amplifier boards specifically designed for the APS application will be completed utilizing the Freescale™ MMG3015NT1, MRF6V2010NR1, and MRF6VP41KH rf devices, respectively. A four-to-one radial combiner also will be designed, constructed and tested using four 1-kW amplifiers to demonstrate a 4-kW 352-MHz combined amplifier system in order to estimate the efficiency of the proposed 200-kW system. A simplified model of a combiner is shown in Fig. 6 where a shunt capacitive and series inductive distributed matching network is used. With four 1-kW input modules, the total dissipated power in the combining network is approximately 5 W. In addition to rf tuning, the reactive stub is also beneficial as a heat sink for the inner conductor of the combiner, which is difficult to access for cooling. The isolation of the combiner between ports is poor in the event of a module failure. As a result, a circulator will be installed with each of the 1-kW modules in addition to a high-power circulator at the final output to account for beam loading mismatches.

The conceptual design of combiners at the 20-kW and 200-kW levels will be initiated in order to assess the overall shape and footprint of the proposed 200-kW system. Combiner cooling requirements and mechanical layout will be determined.

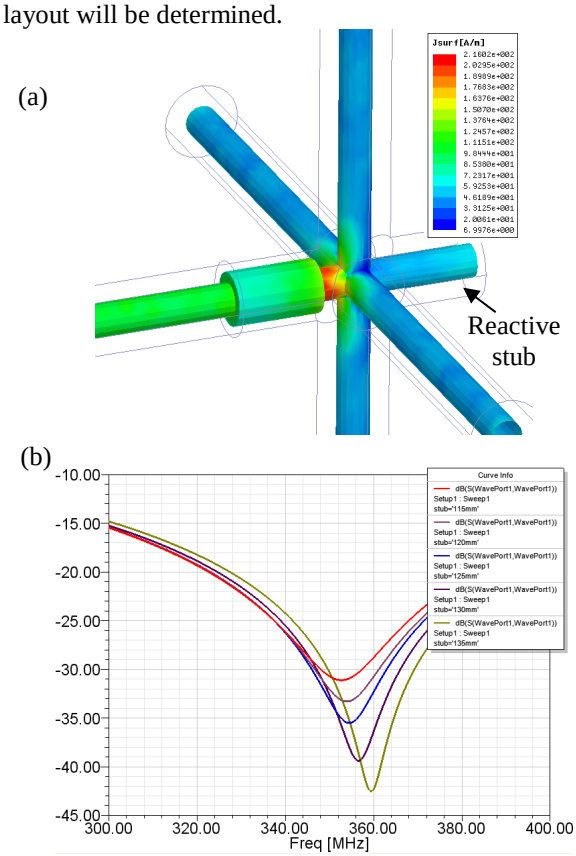

Figure 6: Four-way combiner with a stepped-impedance matching network and reactive stub: (a) magnitude of surface current and (b) return loss for variations of the capacitive and inductive element distributed lengths.

CONCLUSION

Preliminary performance test data indicate that the Freescale™ MRF6VP41KH LDMOS rf power transistor is capable of producing 1-kW cw output power at 351.93 MHz reliably under continuous service if adequate cooling is provided. Soldering the transistor directly to a water-cooled cold plate or a heat spreader thermal bonded to a water-cooled cold plate will be required for maximum thermal transfer and minimum transistor die temperature to achieve maximum device MTTF.

REFERENCE

[1] Jeff T. Collins, Craig M. Conley, John N. Attig, “Enhanced Heat Transfer Using Wire-Coil Inserts For High-Heat Load Applications”, Proceedings of MEDSI02, September 5-6, 2002, ANL-03/7, p. 409 (2003).