THE NEW-GENERATION POWER SUPPLIES FOR THE CIRCULAR POLARIZED UNDULATOR AT THE APS *

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Abstract

The Circular Polarizing Undulator (CPU) has been used for about ten years at the APS to generate X-rays with variable polarization (circular and linear) switching at rates up to 10 Hz [1-4]. The CPU consists of two main coils with maximal currents of 1600 A (about 30 kW power) and 400 A (4 kW power), and seven additional correcting coils.

Aging and obsolescence of some of the CPU power supply (PS) critical components resulted in deterioration of its performance and elevated maintenance. To resolve the issue and to comply with the new requirements for the beam stability at the APS storage ring, new PS and control electronics for the CPU have been proposed.

INTRODUCTION

The CPU's unique capability to produce an internal helical trajectory in the electron beam for providing circularly polarized photons is in great demand by APS users for polarization studies. The increasing requirements for beam stability at the APS storage ring necessitate that both the CPU power supply be improved and the stored beam properties be minimally affected during the CPU operation. The other CPU PS deficiencies are:

- An outdated mechanical design prevents timely maintenance and repair.
- Aging of some of the critical components has led to increased downtime.
- Control electronics performed with outdated low-density integrated circuits scattered over all cabinets makes them susceptible to electromagnetic interference.
- Too many different incompatible chassis are used due to the evolutional development of the CPU, which has led to ineffective control interface with a lack of synchronization.
- Modules with similar functions are not interchangeable.
- Voltage readback channels can not be used because they have a glitch overshoot of about 50 Volts instead of the required 10 Volts.
- No synchronization between polarity switching and current readback, because the correction coils system was added later to the existing main current control system.
- A 4-kHz inverter in the CPU PS produces high-level acoustic noise, which disturbs personnel and is not compliant with OSHA requirements.
- There are presently four DC polarization states with four correction tables for full output current range from 0 to maximum value: clockwise (CW), counter-clockwise (CCW), horizontal (H), and vertical (V). The correction of a given ramp from 0 A to full range depends on the previous state. So there is a need for 16 states as shown in Table 1.

Table 1: DC Polarization States.

Present state	Previous state			
	CW	CCW	H	V
CW	X	-	-	-
CCW	-	X	-	-
H	-	-	X	-
V	-	-	-	X

"X" denotes the present capability of the system
"-"denotes the required capability.

- For better integration with storage ring RTFB system CPU corrector sampling clock should match RTFB clock. Polarization state should be included in RTFB reflective memory, so that DSP scope can collect this information.

To eliminate the existing deficiencies and satisfy new requirements, we formulated the following redesign goals:

- Provide time-efficient diagnostics, maintenance, and repair with contemporary mechanical and electrical designs.
- Provide better integration with the storage ring RTFB system.
- Replace horizontal poles to provide stronger and more uniform field.
- Improve the correctors control system, making it dependent on the previous polarization state.
- Improve correctors by increasing strength of the vertical field.
- Reduce the acoustic noise to a level that does not disturb personnel.

THE NEW PS SPECIFICATION

The CPU PS has nine outputs: one 1600-A unipolar output for the horizontal field coil, one ± 400-A bipolar output for the vertical field coil, and seven ± 10-A outputs for correctors.

The Main Coils Power Supply Specification

The Main Coils PS was built at DANFYSIK (Fig. 1) with the following parameters:

- Maximum output current for horizontal field coil: 1600 A

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Figure 1: The main coils PS.

- Maximum output current for vertical field coil: ±400 A
- Output current switching frequency: DC to 10 Hz
- Output ripple voltage (max): 1 Vpp @ 30 kHz or greater
- Absolute current setting accuracy: less than 100 ppm
- Current setting reproducibility: less than 50 ppm
- Current drift stability:
  - Better than ± 3 ppm (30 minutes)
  - Better than ± 10 ppm (8 hours)
- Output sensitivity to AC input line:
  - ± 10% slow: < 0.5 ppm
  - ± 1% fast variation (T >20 ms): < 0.5 ppm
- Ramp time from 0 to 100% is adjustable from 10 ms to 60 s and can be programmed in either local or remote mode. During the ramping of the power supply, the supply is operating in constant di/dt.
- Temperature coefficient: 1 ppm/°C
- AC mains input: 480 V ± 10%, 50/60 Hz, 3 phase and ground
- Load parameters for horizontal coil:
  - Inductance – 100 μH ± 5%
  - Resistance – 15 mOhm ± 5%
- Load parameters for vertical coil:
  - Inductance – 720 μH ± 5%
  - Resistance – 24 mOhm ± 5%

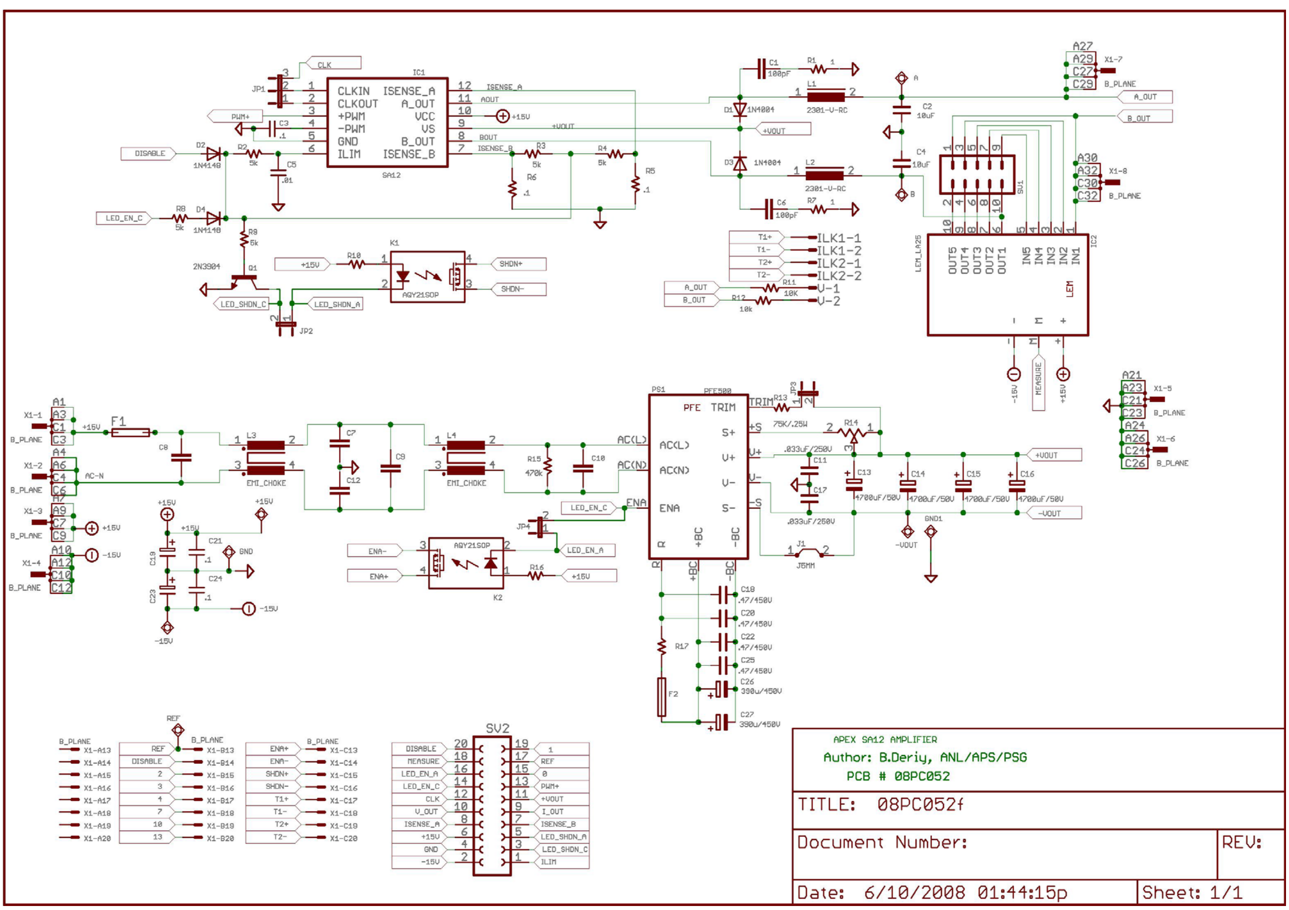

Figure 2: The CPU corrector's PS.

Remote Control:

- A programmable control unit will be provided to fully control power supply in remote mode.
- Current setting, installed options:
  - 18-bit DAC
  - Analog signal 0 to ±10 V
- Current readback, installed options:
  - 16-bit ADC
  - Analog signal 0 to ±10 V
- Communication, installed options:
  - RS-232 / RS-422 / RS-485

Correction Magnets PS

Since the CPU has very strong nonlinearities, especially during transients, and the fields are very sensitive to misalignment [1], the existing correction system had to be improved to correct all measurable CPU perturbations. The correction system consists of seven channels. Four channels serve to compensate the first and second field integrals of both planes (two dipole magnets at the upstream end and two more at the downstream end). Three other channels were implemented for correcting higher-order multipole components: the normal quadrupole, and two skew quadrupoles.

In the existing system, KEPCO power supplies BOP 20-10M were used to drive the correctors. Occupying the whole cabinet in the storage ring mezzanine, they provided insufficient 4-A/ms slew rate and were not compatible with inductive loads in excess of 0.5 mH. An in-house design was made to replace this bulky, outdated equipment. The new design was based on an APEX SA12 pulse-width modulation amplifier that can supply 3000 W to a load at 200 kHz switching frequency (Fig. 2). Each single-channel 3U module is independently powered from 120VAC through an AC-DC module PFE500-28 (TDK-Lambda). All seven modules are contained in a 19" crate.

THE CPU PS CONTROLS

The simplified controls diagram is shown on Figure 3. We have two VME modules designed to control the PS—the CPU PS Controller to control main coils power supply and the arbitrary function generator (AFG) to program seven channels of corrector magnet currents [2]. In the CW/CCW switching mode, the AFG produces arbitrary waveforms for each transition synchronized to a switching pulse (i.e., one waveform for CCW → CW and another waveform for CW → CCW). The last point of the arbitrary waveform represents the DC value held by the AFG until the next switching pulse. In DC mode, the AFG produces seven constant values updated when the CPU setpoint is changed.

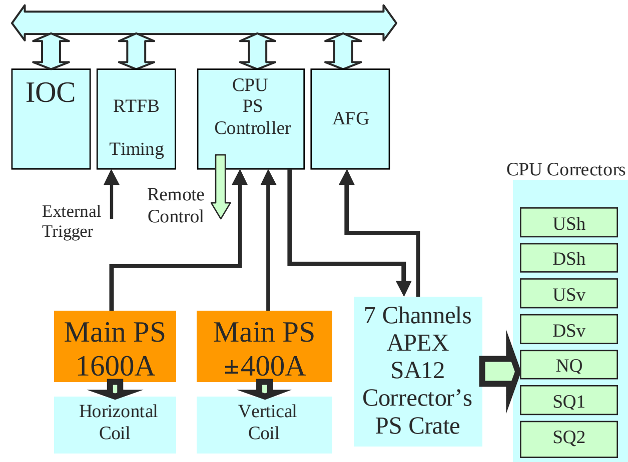

Figure 3: The CPU PS controls.

An EPICS IOC dedicated to the CPU handles the updating of AFG waveforms from stored tables of correction data specific to each operating mode. The tables are linearly interpolated.

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