A HIGH-RESOLUTION DPWM GENERATION TOPOLOGY FOR DIGITALLY CONTROLLED PRECISION DC/DC CONVERTERS AT THE APS*

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Abstract

The APS storage ring uses DC/DC converters to power the magnets. High resolution for current regulation is desired for future improvement. It is calculated that at least 20- to 21-bit digital pulse width modulation (DPWM) is required in the proposed digital control system. This paper proposes a digital control system that adopts a new DPWM topology to achieve 21-bit DPWM without gigahertz system clock. The proposed topology uses a combination of a field-programmable gate array (FPGA) and a serializer chip TLK2541 from TI. The FPGA calculates the desired PWM signals and sends them to the TLK2541 chip. Then, the TLK2541 generates corresponding high-resolution DPWM pulses. An FPGA development board has been used to develop a prototype system to verify the proposed DPWM generation topology. This paper discusses the circuit topology and the experiment results.

INTRODUCTION

There are more than 1300 DC/DC converters used in the Advanced Photon Source (APS) storage ring (SR). At present, an analog control system is utilized to regulate the output current of the power converters. As part of the APS upgrade project, high-resolution current regulation is desirable for future improvement.

In addition, the improvement of stability and reliability of power converter control are also important goals for the upgrade project. In recent years, digitally controlled power converter systems have become more attractive due to such advantages as high programmability, high flexibility, high system integration, reduced development time, fewer components, less susceptibility to environmental variations, and better reliability.

In this paper, an FPGA-based digital control system for SR DC/DC converter is presented. In the proposed digital control system, a new DPWM generation topology using serializer circuit is proposed to achieve 21-bit DPWM resolution. The test results verified the effectiveness of the proposed DPWM generation topology.

DPWM RESOLUTION REQUIREMENTS

An SR sextupole power converter is utilized as the test bench. Its configuration can be simplified as a buck converter topology without the output filter capacitor (shown in Figure 1). The load magnet is composed of inductor L and resistor R. The design goal is to achieve 18-bit resolution for the magnet current regulation.

The parameters of the SR sextupole power supply are: L = 28 mH, R = 110 mΩ, Io(max) = 250 A, Vin = 62V, and the switching frequency f_{sw} = 20 kHz.

An 18-bit ADC is utilized in the magnet current feedback loop. The equivalent full measurement range of ADC is 250 A. Therefore, the equivalent LSB of the A/D converter is

$$\Delta I_{ADC} = 250\text{A}/2^{18} = 0.9537\ \text{mA}. \quad (1)$$

To eliminate the limit cycle ring, the required effective DPWM resolution should be selected as [1]

$$N_{DPWM,eff} \geq \log_2 \frac{V_{in}}{R \cdot \Delta I_{ADC}} = 19.1728. \quad (2)$$

Therefore, at least a 20-bit resolution for DPWM is needed to achieve 18-bit current resolution. In the proposed digital control system, a 21-bit DPWM is selected to fit the resolution requirements for all types of DC/DC converters in the storage ring.

THE CONFIGURATION OF THE DIGITAL CONTROL SYSTEM

Figure 2 shows the block diagram of a prototype digital control system for SR power converters. The system is composed of five parts: an Altera Cyclone III DSP development board, an interface board, an IGBT driver card, a current-sensing circuit, and an ADC card.

The ADC card utilizes 18-bit ADC converters (AD7634) to convert the sensed current/voltage signal into 18-bit digital data. The Interface board contains a TLK2541 serializer circuit, which is used to realize the proposed new DPWM generation topology. The key part of the proposed digital control system is the FPGA

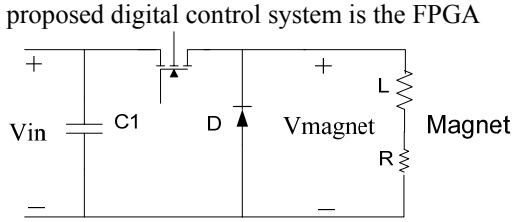

Figure 1: Scheme of storage ring sextupole DC/DC converter with magnet load.

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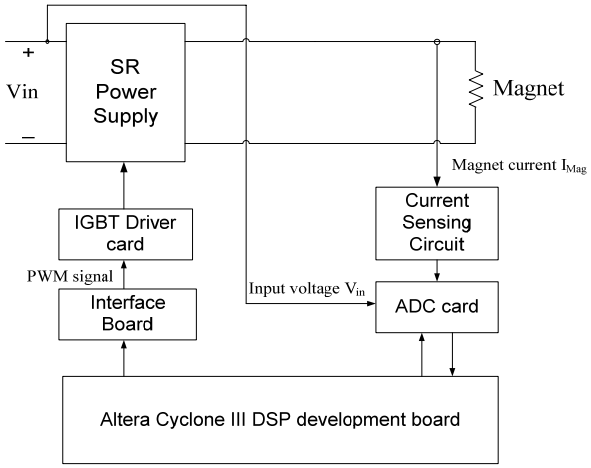

Figure 2: Digital controller prototype for storage ring power converters.

development board. It calculates the duty cycle values based on the sensed magnet current and input voltage.

In the digital control system, the digital filter module filters out the noises and ripples in the sensed data by using a low-pass filter and an averaging method. The regulator used in the control system is a discrete PI controller. In cooperation with the interface board, a DPWM signal is generated and sent out to the IGBT driver card (shown in Figures 2 and 3).

In the proposed serializer modulation DPWM topology, the DPWM generation is realized by a TLK2541 serializer chip on the interface board. The TLK2541 chip can convert a 20-bit parallel input signal into a serial output signal. Therefore, the DPWM resolution can be improved by a factor of 20.

However, the maximum output series data rate of the TLK2541 serializer chip is 2.6 Gbs. The switching frequency of the DC/DC converter is 20 kHz. Therefore, the maximum DPWM resolution that can be achieved by only using the serializer circuit is $\log_2$ (2.6 G / 20 K) =17 bit. In order to get 21-bit DPWM resolution, a ∑-Δ DPWM modulator is added to cooperate with the serializer modulation topology (shown in Figure 4).

The principle of ∑-Δ modulator is illustrated in [2]. As shown in Figure 5, the input of the ∑-Δ modulator is an M+N bit duty cycle signal d[n]. The least N bits of d[n] are truncated by the ∑-Δ modulation to get the M bit output duty cycle signal $d_{HR}[n]$ for DPWM. The residual error $d_{LR}[n]$ is accumulated and then added back to the input of the modulation circuit. Using this modulation method, the resolution of DPWM generation is increased by N bits without increasing the system clock frequency.

In the proposed DPWM generation topology, a 4-bit ∑-Δ modulator is utilized. The input of the ∑-Δ modulator is the 21-bit duty cycle value. The output of the ∑-Δ modulator is the truncated 17-bit duty cycle value, which is sent to the serializer code generation module (shown in Figure 3).

The principle of serializer code generation can be illustrated as follows:

In PWM waveform, the signal only has two states, either "on" or "off". The "on" state of PWM can be implemented by serial data "111···111". The "off" state can be interpreted by serial data "000···000". Therefore, the serial code for one switching cycle can be presented as "111···111000···000". The width of the on-time and off-time of PWM waveform can be regulated by changing the data length of the serial code "111···111" or "000···000".

In the proposed digital control system, the input bus to the TLK2541 serializer chip is 20-bit. The clock frequency for the FPGA board is 125 MHz. Therefore, the output serial data rate of the TLK2541 is 125M*20=2.5 Gbs. The switching frequency of the DC/DC converter is 20 kHz. Then, the serial code in one switching cycle is 2.5G/20K= 125000. These serial codes are divided into 125000/20=6250 groups. Each group contains a 20-bit serial code.

The output data format of the TLK 2541 serializer chip in one switching cycle is shown in Figure 5. Only three types of serial code forms are used in the output data. They are "111···111" (type 1), "111···000" (type 2), and "000···000" (type 3) (shown in Figure 5). The type 2 code only has one group of data. How to determine the group number for the type 1 serial code, and the number of bit "1" in the type 2 code is the key issue in the proposed serial code generation.

On the other hand, the digitalized duty cycle value d[n] can be interpreted as the length of serial code "111···111", where the duty ratio value is equal to d[n]/125000.

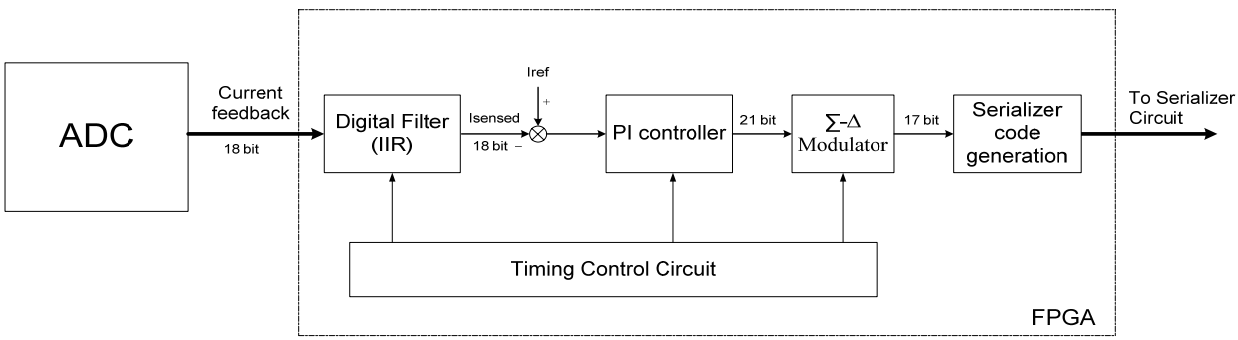

Figure 3: Digital control system using serializer modulation DPWM topology.

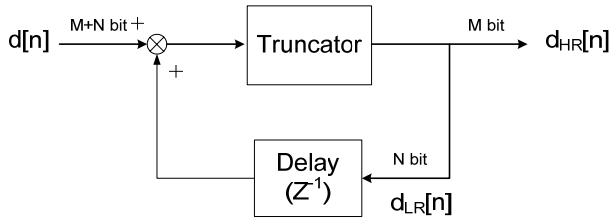

Figure 4: ∑-Δ modulator implementation block diagram.

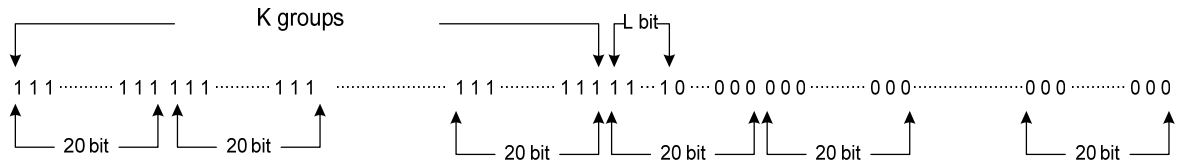

Figure 5: Data format of the output of the TLK2541 serializer chip.

Dividing d[n] by 20, we can get the quotient value K and the residual value L. The quotient K determines the group number of the type 1 serial code "111…111". The value of residual L determines the number of bit "1" in the type 2 serial code "111…000" (shown in Figure 5). Therefore, the data format for one switching cycle is obtained by calculating the duty cycle value d[n].

EXPERIMENTAL RESULTS

A sextupole DC/DC converter with magnet load has been set up as the test bench. Their parameters are listed in the DPWM Resolution Requirements section.

Figure 6 illustrates the DPWM waveform generated by the serializer modulation DPWM topology. Figure 7 shows the regulated output current by using the proposed serializer modulation DPWM topology. The reference current is set to be 10 A. It is shown in Figure 7 that, under the control of the proposed digital control system, the current ripple during the steady state is around 5.5 mA. Since Io(max) of the DC/DC converter is 250 A, the current regulation resolution achieved is 250 A/5.5 mA = 45454, which is approximately 15.47 bits. After analysis of the experimental data and the test bench, it is found that the EMI noises in the feedback loop deteriorate the system performance. Further research will be conducted to resolve this problem and improve the current regulation resolution to 18 bits.

CONCLUSION

In this paper, a digitally controlled precision DC/DC converter system is proposed to improve the current regulation resolution of the APS storage ring power converters. In the proposed digital control system, a new DPWM generation topology using a serializer circuit is implemented. A spare sextupole power converter is being used to verify the proposed control topology in the real circuit. Experimental results show the effectiveness of the proposed DPWM generation topology.

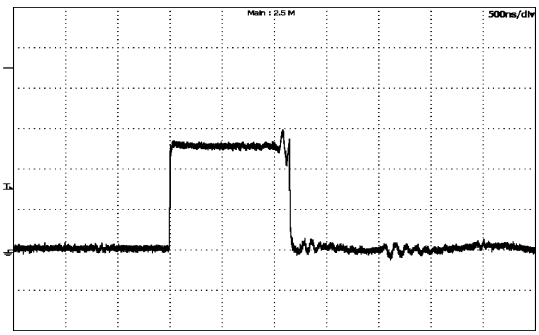

Figure 6: PWM waveform of the proposed serializer modulation DPWM generation topology.

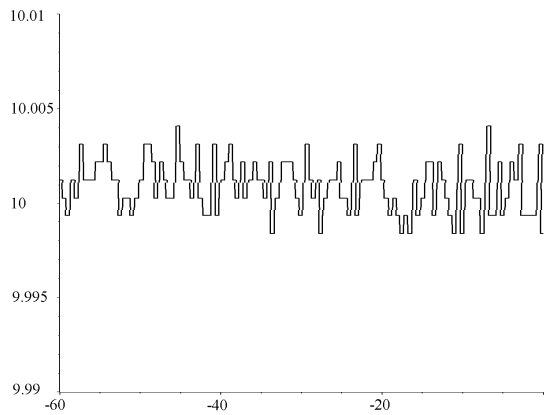

Figure 7: Output current waveform during steady state under the control of the proposed digital control system. x axis: time (seconds), y axis: current (amps).

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