

ALS FPGA-BASED DIGITAL POWER SUPPLY CONTROLLER FOR RAMPED POWER SUPPLIES IN THE BOOSTER*

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Abstract

The Advanced Light Source (ALS) is a third generation synchrotron light source that has been operating since 1993 at Berkeley Lab. Recently, the ALS was upgraded to achieve Top-Off Mode, which allows injection of 1.9GeV electron beam into the Storage Ring approximately every 30 seconds. Modifications required for Top-Off operation included replacing the booster dipole and quadrupole magnet power supplies to increase the peak booster beam energy from 1.5GeV to 1.9GeV. Each new power supply was originally controlled by an analog controller that performs the current regulation and, in concert with other modules in the control chassis, determines the output of the ramped power supply. The new digital power supply controller performs the current regulation digitally to provide greater output stability and resolution. In addition, it provides remote monitoring of current regulation signals, interlocks, and status signals, as well as remote control of the power supply operation via Ethernet. This paper will present the ALS Digital Power Supply Controller module requirements and design.

INTRODUCTION

The Advanced Light Source (ALS) currently operates for users in Top-Off Mode, in which electrons are injected into the Storage Ring (SR) on energy at 1.9GeV approximately every 30 seconds [1]. The Booster Ring (BR) bend and quadrupole magnet power supplies were replaced to provide the peak current and accurate tracking required to achieve Top-Off operation. Each new power supply was provided with a bin of control electronics, including an analog controller module that performs the current regulation. This module is sufficient to run Top-Off, but does not provide remote control, visibility, and diagnostic capability. To achieve these functions, ALS designed a new Digital Power Supply Controller (DPSC), including a Field Programmable Gate Array (FPGA) and high resolution data converters.

The DPSC must be pin compatible with and the same physical dimensions as the analog controller. For adequate current regulation performance, the current reference input must have at least 20mA of resolution and a 50kHz update rate, with programmable gain and offset. The current regulation must track the reference to within 0.2% when operating above 20A. It must also contain an interface to the ALS Timing System for synchronization purposes, and be accessible to the control system remotely via Ethernet.

In addition to the requirements, it is desirable to have

data capture capability, for both online status monitoring and post-mortem analysis. It is also possible with the proper wiring changes to incorporate the voltage regulation and pulse-width modulation (PWM) drive to the Insulated-Gate Bipolar Transistors (IGBTs) into the DPSC functionality. These functions require additional measurement, development, and minor modifications to the control bin circuitry; therefore a phased approach will be used to implement these additional capabilities. The DPSC prototype is shown in Figure 1.



Figure 1: The DPSC prototype board.

DESIGN STRATEGY

As mentioned above, the functions of the DPSC will be implemented in phases. Phase 1 is divided into two parts. In phase 1A, The DPSC replaces the functionality of the existing analog controller directly, generating an analog voltage reference output. The DPSC digitizes an analog reference from an external input and perform the current regulation digitally at 100kHz. The power supply is controlled locally only, and gain and offset parameters are fixed. In phase 1B, a digital reference waveform is downloaded via an Ethernet control system interface. Waveform readback is provided at 5kHz continuously and 100kHz after a single-shot trigger. Control and interlock status are also available remotely. Gain and offset parameters are remotely programmable.

In phase 2, the DPSC is also responsible for the voltage regulation. The voltage feedback is digitized and both current and voltage regulation are performed digitally. Voltage regulation waveforms are available remotely, and gain and offset parameters are remotely programmable. The DAC provides the analog reference to the existing PWM module. This function replaces the existing voltage regulation module, and must also perform its interlock and control functions. In phase 3, the DPSC converts the voltage regulation output to a digital PWM waveform to drive the IGBTs directly, replacing the existing PWM module. Upon completion of this phase, all data processing and power supply control is performed digitally.

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IMPLEMENTATION

Hardware

The DPSC hardware consists of a commercial FPGA module and a custom board. The FPGA module is a Mamec Virtex-4 FX12 Mini Module [2]. This module is the basic building block for several recent ALS systems including the ALS Mini IOC [3], and the Extraction Trigger Inhibit Interlock System [4]. It features a Xilinx Virtex-4 FX12 FPGA with an embedded PowerPC processor, 64MB of RAM, 4MB of Flash, Ethernet PHY, and over 70 general purpose digital I/O lines on an expansion connector. The RAM is used to store the current reference table, readback waveforms, and software code. The Flash is used to store boot software so the system can boot from a remote server via Ethernet. A block diagram of the hardware is shown in Figure 2.

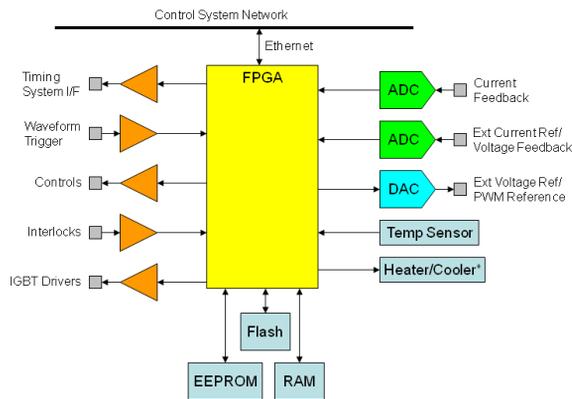


Figure 2: DPSC hardware block diagram.

The custom board contains the power regulators, analog interfaces, temperature control circuit, and various digital interfaces. The current feedback is sampled by the AD7767 24-bit 100ksps ADC. The external current reference (phase 1A) or voltage feedback (phases 2, 3) is sampled by the AD7691 18-bit 250ksps ADC. The voltage reference (phase 1) or PWM reference (phase 2) output is driven by the AD1955 24-bit 100ksps DAC. The current feedback ADC is located in a temperature controlled copper box. The temperature inside the box is measured by a 10-bit digital temperature sensor, and a 16-bit 1Msps DAC drives a Peltier thermal element attached to the box. Another 16-bit DAC drives a buffered current reference to the voltage regulation control module, which uses the signal in interlock circuitry.

The board also contains several digital interfaces. A 4kb EEPROM stores unique serial number and Ethernet configuration data. An RS-232 port is used for console display and debugging. A MAX7313 serial-parallel 16-bit I/O port expander reads the various system interlock status. IGBT drivers and timing system interfaces are also buffered and level-shifted on this board.

Firmware

The FPGA firmware is built using the Xilinx Platform Studio and Embedded Development Kit (EDK) tool set [5]. Figure 3 illustrates the required logic cores for each design phase. Many of these cores, such as the Ethernet, RAM, Flash, RS-232, and CPU, are provided by Xilinx and are configurable at a high level in the EDK environment. EDK also provides a wizard to import custom cores, such as the current regulation, voltage regulation, power supply control, and IGBT control cores. These custom cores are designed with flexible external interfaces so they can be reconfigured, not redesigned, as each design phase is implemented.

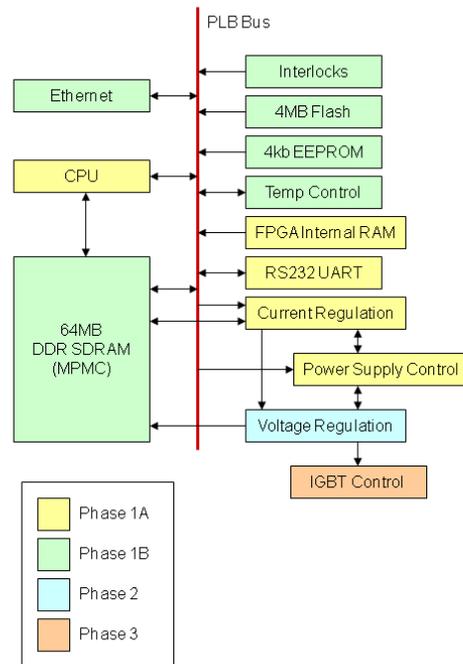


Figure 3: DPSC firmware top level block diagram.

Software

The PowerPC embedded processor in the FPGA runs the control system interface software EPICS on the real-time operating system VxWorks. The EDK environment supports pushbutton board support package generation for several versions of VxWorks, simplifying the integration of software with the custom firmware on an FPGA [6]. This process has already been used to implement a complete hardware plus software system for the ALS Mini IOC [3].

BENCH TEST

The hardware prototype has been built, along with a test module that emulates transfer functions of the voltage regulation, the power supply, and the magnet, from current regulation output to current feedback input. The current regulation firmware for phase 1A was developed and tested on the prototype.

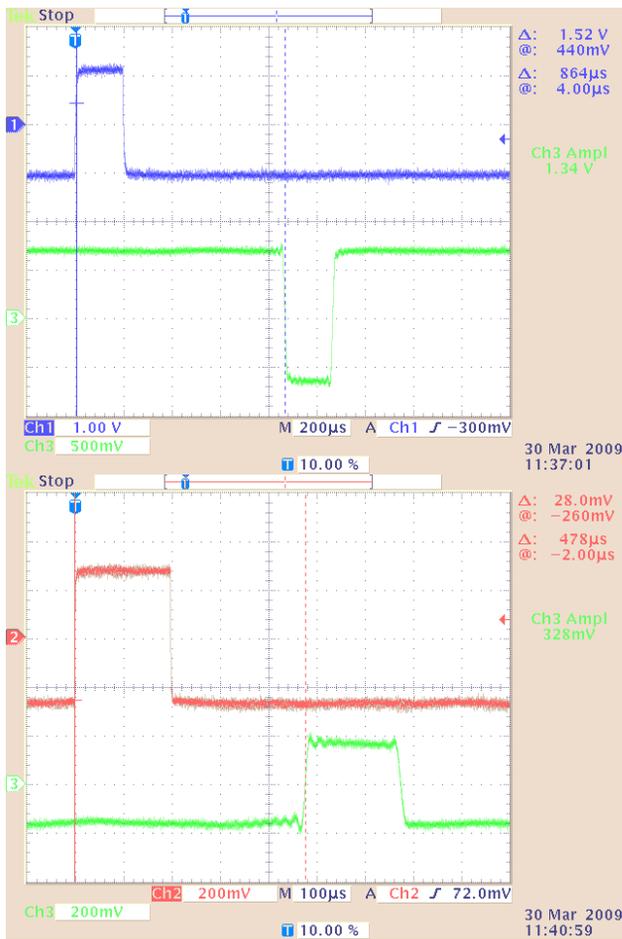


Figure 4: DPSC system step response.

The step response of the system is shown in Figure 4. At the top is the step response measured at the DAC output to a pulse at the current feedback 24-bit ADC input, and is measured to be 864 μ s. This delay is well within the bandwidth required for current regulation of the magnet, which contains a dominant pole at about 6Hz. By comparison, Figure 4 bottom shows the step response to the external current reference/voltage feedback 18-bit ADC input to be 478 μ s. Both ADCs have an SAR architecture, but the 24-bit ADC has a digital anti-aliasing filter that accounts for the difference in response time. In

both cases, the DAC accounts for about 475 μ s of the system delay.

CONCLUSION

The replacement of the existing analog current regulation module with a digital controller has several advantages, including accessibility via the control system, synchronization with the timing system, and improved accuracy and tracking. The DPSC also has the flexibility to integrate the voltage regulation and PWM generation to drive the IGBTs directly, replacing much of the existing analog circuitry performing these functions with a flexible and programmable digital system in a single module.

Early testing of the prototype DPSC on the bench reveals adequate system response to perform the current regulation. The next step will be to tune the gains and offsets of each current regulation signal to match the existing system, and then an in-situ test will be performed on one of the booster quadrupole power supplies. The performance of the DPSC can then be measured in greater detail. Then, work can begin to incorporate design phase 1B functions.

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