

A HIGH VOLTAGE, HIGH REP-RATE, HIGH DUTY FACTOR STACKED TRANSFORMER MODULATOR*

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Abstract

A high voltage modulator has been built and installed at Fermi National Accelerator Laboratory for the purpose of driving the gun anode of the Tevatron Electron Lens (TEL1 and TEL2) [1]. It produces a defined voltage for each of the 36 (anti)proton bunches. This modulator employs five transformers to produce high voltage at a high repetition rate and high duty factor. It is capable of outputting sustained complex waveforms having peak voltages over 6 kV and average periodic rates up to 450 kHz with voltage transitions occurring at 395 ns intervals. This paper describes key aspects of the hardware design and performance.

INTRODUCTION

The TELs were proposed for compensating adverse beam-beam effects of colliding beams in the Tevatron [1]. Regardless of the type of compensation desired, implementation needs to be done on a bunch-by-bunch basis. For the Tevatron, that means each of the 36 (anti)proton bunches would pass through an electron beam of an appropriately defined density. Beam-beam compensation of either the protons or antiprotons is done to improve the luminosity. Electron current is generated by the electron gun following the relation: $I_{gun} = kV_{anode}^{3/2}$. This requires the electron anode driver (modulator) output a unique voltage for each of the 36 bunches. Bunches are spaced 395 ns apart.

The modulator driving the electron gun anode needs to be essentially a 6 kV output, arbitrary waveform generator that transitions to different voltages in 395 ns intervals. The 36 bunches are grouped in three equally spaced bunch trains containing 12 bunches and an abort gap. The pattern of defined voltages for one 12-bunch train and abort gap represents a ‘waveform’. One waveform period is 7.1 μ s. The pattern of bunch-by-bunch adverse beam-beam effects is nearly the same for each of the three bunch trains in the Tevatron, although the pattern is different with each store. Therefore, it was agreed to be acceptable to repeat the same modulator waveform three times every Tevatron revolution to compensate all 36 (anti)proton bunches.

Additional requirements for a modulator are:

1. Applied gun voltage needs to be stable with time—low ripple ($\ll 1\%$).
2. Ample voltage, 5 kV minimum.
3. Load on the modulator is the 60 pF gun anode.
4. Requirements for flat top voltage slope are not

exactly known, but several Volts per ns is probably acceptable.

DESIGN APPROACH

The design approach followed the line of reasoning that transformers lend themselves to high duty factor waveforms, and the AC coupling nature of transformers is of no consequence since the output—out of necessity—must be capacitively coupled to the gun anode floating at high voltage anyway. Pulse transformers can easily produce fast enough rise times, and stacking the secondaries of a number of them in series constructs higher voltage. Figure 1 shows the circuit topology for this modulator built with five transformers. No real power is delivered to the load. Priority in the design approach was to minimize transformer leakage inductance to achieve 5 kV. Power dissipation from parasitic capacitance came second in consideration with the cost of transformer core material. The modulator needs to be located as close as possible to the electron gun to keep the output lead capacitance to a minimum.

Each H-bridge driver either applies DC input voltage V_{IN} (in one direction or the other) to the primary or shorts it out. Employing a number of transformers will enable a variety of discretely different voltage levels to be produced when V_{IN} and 0 V are applied to transformer primaries in combinations. At any given time, the output voltage is the sum of the transformer secondary voltages. The maximum voltage is a multiple of the V_{IN} value. For any V_{IN} value there are always 16 equally spaced discrete output voltages that can possibly be produced from minimum to maximum given the five transformers in this modulator. All voltage transitions occur synchronously with the 395 ns spaced bunches.

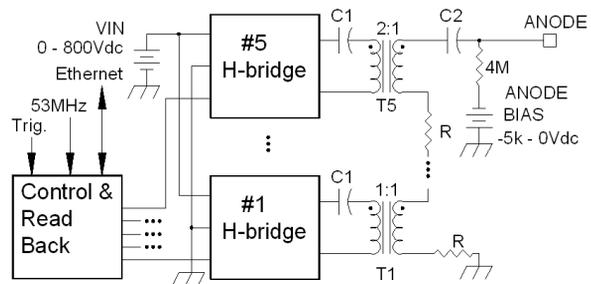


Figure 1: System block diagram.

During the modulator design phase, measurements revealed that the anode voltage required to compensate the largest beam-beam tune shift effects in the Tevatron could be relaxed down to 5 kV (or even lower). However, the 12-bunch tune shifts pattern that needed to be compensated was found to be more complex than

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originally anticipated. During some stores, the tune shift pattern among a 12 bunch pulse train returned to zero as many as three times. This means parasitic capacitance would be driven to elevated voltages and back to zero three times during a 7.1 μs waveform—not just once. As a result, various aspects of the hardware are designed to handle average waveform repetition rates of, potentially, 420 kHz ($3 \cdot (1/7.1 \mu\text{s})$). Power dissipation to charge and discharge any given parasitic capacitance is $C \cdot V^2 \cdot f$. For example, 375 Watts is dissipated driving 100pF from zero to 5 kV at 148 kHz, 1.1 kW at 420 kHz. The resulting internal power dissipation was estimated to be upwards of 2kW, worst case, distributed between FETs, transformer cores and secondary side series resistors.

Certain commercial components were chosen for speed and low power. IXZR08N120 FETs for the H-bridges were chosen from IXYS for having speed and low output capacitance, C_{oss} . MN8CX transformer core material from Ceramic Magnetics, Inc. was chosen for having high enough μ and low loss at hundreds of kilo-Hertz.

Parasitics Modeling

Bench tests were done to verify formulas of parameters for pulse transformer anticipated to be built in house. Also, measured pulsed transformer pulse rise times were compared to SPICE simulations to verify the model of a single transformer. Results went into SPICE simulations of the whole secondary side circuit as well as numerous iterations of transformer design calculations using MathCAD. The transformer model that proved to be quite accurate was that of a simple series RLC circuit. Figure 2 shows the SPICE circuit using this transformer model. V_n are the secondary voltage pulses. The parameters L_{LK_n} and C_{sn} are the transformers' measured leakage inductance referred to the secondary side and the measured stray capacitance, respectively.

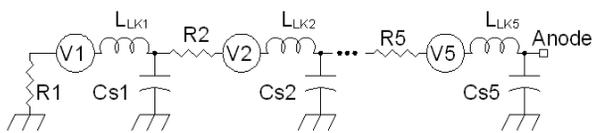


Figure 2: Secondary side parasitics model.

Without damping resistors, transformers stacked in this manner do nothing but ring terribly. Resistors of properly chosen values placed between each secondary winding result in a well controlled composite output pulse shape regardless of which or how many transformers are contributing voltage.

For the test, the damping resistor value was calculated from measured parasitic values by the expression $R = 2 \cdot \sqrt{L_{LK}/C_s}$. The damping resistor value was then adjusted from the calculated value to the point of being critically damped. Critically damped rise times of measured versus modeled show the measured faster than the SPICE model by 20%. SPICE data was also used to calculate and predict damping resistors power dissipated.

Employing Transformers

Use of transformers takes advantage of the fact that the modulator output needs to be offset anyway. Also, the Stacked Transformer Modulator makes full use of the transformers by driving them with V_{IN} in a bipolar manner. For a given input voltage V_{IN} , the maximum the output voltage can be made to swing is the difference in voltage between all the transformers driven positive at the same time minus the voltage with all the transformers driven negative at the same time. A transformer, in practice, will never be driven in the opposite direction than the other transformers at the same time.

For this design, transformers 1, 2 and 3 are wound 1:1, while 4 and 5 are wound 2:1. The H-bridge drivers are controlled to apply three voltages to a primary: $+V_{IN}$, $-V_{IN}$ and 0 Volts. Having transformers of two different turns ratios is what is responsible for there being 16 distinctly different voltages that can be produced from minimum to maximum output. The maximum output voltage that can be produced for a given V_{IN} value is $V_{OUT_{max}} = 8 \cdot V_{IN}$ V peak-peak. Thus, 6.4 kV peak-peak will be output for $V_{IN} = 800$ Vdc.

Bias voltage needs to be applied to offset any given waveform to maximize the use of modulator's output. Anode voltage that swings below the cathode cuts the gun off—only voltage above the cathode produces gun electron emission. The bias voltage must be adjusted to raise the waveform voltage above the cathode DC voltage such that the most negative voltage value in the waveform is just equal to that of the cathode. Doing this enables the anode to be driven 6.4 kV above the cathode.

Figure 1 shows the C1 primary series capacitor that provides a couple of benefits:

- 1) This capacitor eliminates the threat of core saturation. When the Volt \cdot second product of drive in the positive direction is different than in the negative direction over the waveform period, a non-zero voltage develops across the series capacitor that automatically averages out the AC voltage across the primary winding.
- 2) The H-bridge switch between three voltage states: $-V_{IN}$, a shorted primary and $+V_{IN}$. This capacitor allows $-V_{IN}$ to be the default voltage drive condition. Switching from $-V_{IN}$ to the "shorted primary" causes the output to transition positively V_{IN} Volts. Switching from $-V_{IN}$ to $+V_{IN}$ causes the output to transition $2 \cdot V_{IN}$ Volts. This scheme makes the modulator seem as though it is unipolar. It also makes narrow, high voltage, low duty factor pulses possible using transformers (see Figure 4).

Control

The embedded controller is an assembly of several PCBs. It contains a commercial 8-bit microprocessor core module from Rabbit Semiconductor that handles communications with the ACNET control system. H-bridge switching control logic is configured into Altera MaxII complex programmable logic (CPLD) ICs. Waveform descriptions are downloaded into the CPLDs.

Switching patterns are synchronized with the external 53 MHz Tevatron clock and are triggered every machine revolution. Temperatures of the ferrite cores and a FET heat sink on every H-bridge board and input DC current are monitored. Individual H-bridge driver boards can be switched out of operation for any reason and only limits maximum possible output voltage. Diodes in the H-bridge clamp the disconnected stage so that it always contributes 0 V.

Mechanical Design and Cooling

Components requiring cooling are the H-bridge FETs, the transformer cores and secondary side damping resistors. The H-bridge driver board and its transformer were made to be single module to minimize lead inductance which also formed a common path for cooling. One of the five modules is shown in Figure 3.



Figure 3: H-bridge driver and transformer module assembly.

The chassis is designed with six bays in which the transformer modules are installed. Three bays are located above the other three. Located close behind the bays are the secondary side resistors that have short connecting leads to their respective secondaries. The chassis is designed to minimize electrical path length of the secondary side connections.

For cooling, air is forced from the front of the chassis, through the transformer assembly to cool both the FET heat sinks and the transformer core then past the damping resistors. One single 300 CFM fan was used in the chassis.

RESULTS

Figure 4 shows the modulator output of a complex waveform created to compensate protons in Tevatron store #5162. Voltages transition to different levels for every one of the 12 bunches with the exception of #1 and #2 which are the same. Input voltage V_{IN} is set to 600 V, and the maximum voltage produced is 4800 V at bunch #12. (This waveform is showed without bias offset voltage applied.) Not observable at this time scale is a 50 ns window of maximum flatness existing for every bunch.

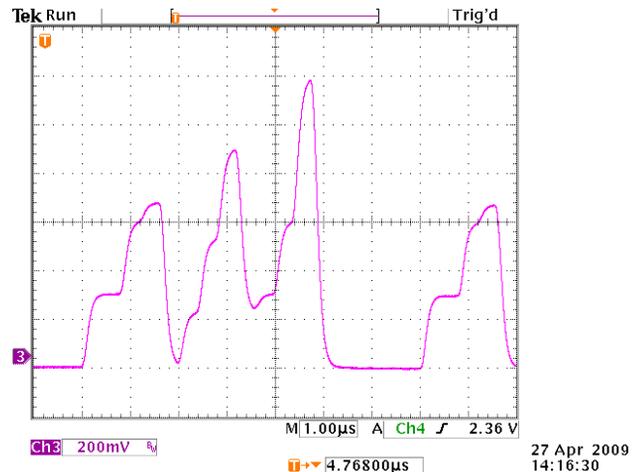


Figure 4: High duty factor, complex voltage waveform displayed at 4000V/V. Shown is one 12-bunch train, 2.3 ms wide abort gap and the start of the same waveform for the following 12-bunch train.

Proton transit time through the TEL is 6 ns, and the voltage slope during this 50 ns window is less than 3 V/ns worst case for a voltage that is applied for only 395 ns.

The maximum output voltage of 6.4 kV should not be produced within waveforms that have periodicity greater than 148 kHz due to excessive internal power dissipation. There exists a voltage/frequency trade off that needs to be made for operating at the upper ends of switching rate and voltage.

Other output plots are shown in [2].

CONCLUSION

The Stacked Transformer Modulator has been installed that enables the TEL2 to provide beam-beam compensation of any (as well as all 36) (anti)proton bunches when desired. This modulator can output complex, arbitrary waveform generator-like performance with 16 definable voltage levels proportional to the input DC voltage with output voltage up to 6.4 kV.

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