FPGA UTILIZATION IN THE ACCELERATOR INTERLOCK SYSTEM (ABOUT THE MPS DEVELOPMENT IN THE LIPAc)

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Abstract

IFMIF (International Fusion Material Irradiation Facility) will generate 14 MeV neutron flux for qualification and characterization of suitable structural materials of plasma exposed equipment of fusion power plants. IFMIF is an indispensable facility in the fusion roadmaps since provide neutrons with the similar characteristics as those generated in the DT fusion reactions of next steps after ITER. IFMIF is presently in its EVEDA (Engineering Validation and Engineering Design Activities) phase.

As part of IFMIF Validation Activities, LIPAc (Linear IFMIF Prototype Accelerator), designed and constructed mainly in European labs (CIEMAT, CEA, INFN and SCK CEN) with participation of JAEA, is currently under installation at Rokkasho (Japan). LIPAc will accelerate a 125mA CW and 9MeV deuteron beam for a total beam average power of 1.125MW. The Machine Protection System (MPS) of LIPAc provides the essential interlock function of stopping the beam in case of anomalous beam loss or other hazardous situations, particularly critical for investment protection reasons in high power accelerators.

High speed processing is indispensable to adequately achieve the MPS main goal. This high speed processing of the signals, distributed alongside the accelerator facility, is based on FPGA technology. This paper describes the basis of FPGA use in the accelerator interlock system through the development of LIPAc´s MPS.

INTRODUCTION

LIPAc is a prototype accelerator that will reach a beam average power of 1.125 MW with deuterons in CW at 125 mA and 9 MeV. It will validate the accelerators of IFMIF [1] (125 mA in CW at 40 MeV) by demonstrating that the space charge issues can be overcome at its lowest 1st energy superconducting accelerator stage (the 40 MeV will be achieved in three additional SC stages at 14.5, 26 and 40). The involved high power and beam nature entails investment protection arguments and radiation safety aspects. The control system for LIPAc is responsible of its safety functions, the control and monitoring functions to realize these tasks efficiently target the minimization of activation induced by beam losses (driven by 'hands-on' maintenance principles) and potential hazard to the investment. In light of these requirements, the control system of LIPAc is broken down as follows: 1) Central Control System (CCS), 2) Local Area Network (LAN), 3) Personnel Protection System (PPS) to avoid unnecessary exposure to radiation, 4) Machine Protection System (MPS) for the accelerator subsystems and the facility, 5) Timing System (TS), 6) Local Control System (LCS) for the accelerator subsystems.

The remote operation for LIPAc is performed by CCS, LAN and the different LCS. The high level data (using EPICS) is transmitted by using LAN (Ethernet). All subsystems with synchronization for pulse operation are realized by using TS signals. The radiological safety for the personnel is established by PPS. And the beam inhibit (fast and slow) is realized by MPS in order to protect the accelerator and its components. This paper describes the outline and development status of MPS [2].

OUTLINE OF MPS

LIPAc produces a powerful CW deuteron beam [3] with high average beam current of 125 mA. The 9 MeV deuteron beam with its MW range beam power will be absorbed on a Cu beam dump water cooled. If an excessive beam loss event happens in an undesired manner on an accelerator component, the power would potentially cause a fatal damage. Additionally, the high inelastic cross sections of deuteron would lead, in case of excessive beam losses, to an increase of neutron and gamma induced dose rates in the radiation controlled area, with a potential dramatic impact of the targeted 'hands-on maintenance' approach. The Machine Protection System (MPS) is defined as the safety system against the accelerator troubles for the protection of the investment. The MPS has interfaces with other LIPAc subsystems, including the PPS (Personnel Protection System) Accelerator subsystems. It comprises the beam stop interlock signal from each accelerator subsystems, each of which presents interfaces with the MPS, PPS, EPICS, and emergency stop logic of subsystem. MPS realizes the beam rapid stop to minimize the effects on the beam pipe by beam loss. The target time of MPS signal transfer, which is the time taken from "MPS unit receives the interlock signal from accelerator subsystem" to "MPS sends the beam stop signal to the injector", is less than 10 μs. To achieve this fast response time, FPGA technology has been chosen.

The backbone of MPS for LIPAc is the already consolidated successful MPS unit used at J-PARC Linac. In the case of MPS for J-PARC Linac, the "Beam rapid stop" is achieved within 5 μs after "MPS units receives the interlock signal from accelerator subsystem" with high reliability experienced [4].

Therefore, the use of J-PARC Linac's knowhow as the basis of LIPAc's MPS unit is suitable for the interface between MPS and accelerator subsystem; MPS itself will realize the logic for beam stop and beam restart.

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CONFIGURATION OF MPS

The MPS consists of hardwired units (MPS unit, FPGA based for the fast logic processing) and PLCs (for the communications through EPICS to the CCS), as shown in Figure 1. The Interlock signal can be any relevant status signals coming from the subsystems (vacuum, temperature, cooling, RF, LVPS, valves, slits, BLOMs…).

The means of action are stopping the beam. Each MPS unit is connected by hardwire (metal or optical cable). An interlock signal received by an MPS unit is sent to the unit for Injector within the 10 μs specified speed. Next, the unit for Injector sends the "beam stop signal" to Injector, and Injector will stop injecting the beam. The PLC connected with the MPS unit does not participate in stopping the beam process; the PLC is independent from MPS logic, so that it is only status monitors and reset the interlock latch of the MPS units. The MPS logic is separated from the PLC. The interlock logic function of MPS is realized using FPGA, because high speed signal processing is necessary. Since I/F with the external interlock signal of MPS correspond to transmission noise, it is isolated by the photo-coupler. Furthermore, the digital filter in FPGA removes noises.

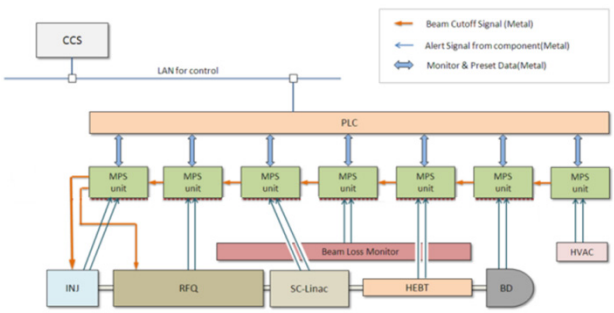

Figure 1: Principle of MPS.

MPS Unit and Interlock Module

The MPS unit is the basic structure, where modules and a power-supply module are united. Different modules are installed for each type of interlock signals. The unit can install 5 modules at maximum. There are interface terminals at the back panel. Figure2 shows how the MPS modules are functionally linked together, arranged by type of signal. (slow/fast stop, etc) The modules are installed for each of the interlock signals. In turn, Figure 3 shows the functional configuration of the standard module of MPS. A standard module has the function to summarize and transfer the interlock signals. The standard module consists of a FPGA with some devices of interface to external signals. The communication between one MPS unit and another uses differential signal transmission protocol, to maximize the reliability of the link and increase the maximum available distance. The FPGA is rapid speed processing of summarized interlock signals. There are some interlock signal types from a subsystem; one is sent to the MPS unit directly after a fast response circuit, and the other is sent to the MPS unit after a slow response circuit. An interlock Beam Inhibition (BI) signal made by fast response circuit is defined as "FBI signal" because the signal is sent to the MPS unit (and transmitted through it) in the tens of μs order. In turn, a similar signal made by slow response circuit in the subsystem, is defined as "SBI signal" because the signal is sent to the MPS unit (and transmitted through it) in the hundreds μs order. The standard module of MPS corresponds to these two types of interlock signals (FBI and SBI), and presents two kinds (fast, slow) of interlock I/F and mode change by jumper settings.

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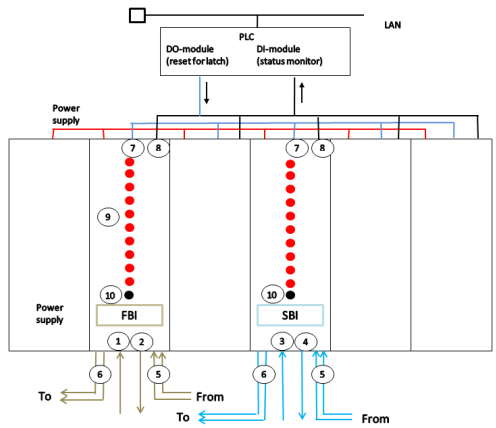

Figure 2: Functional arrangement of the MPS.

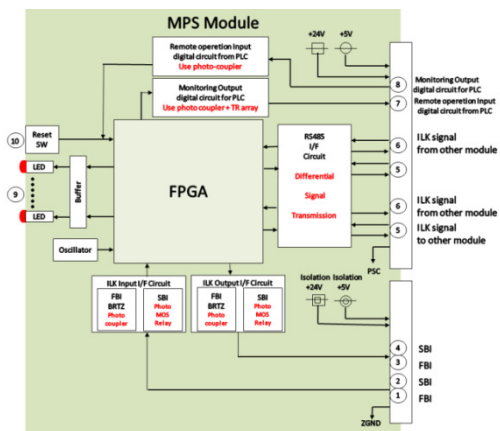

Figure 3: Functional Configuration of standard module of MPS.

DEVELOPMENT STATUS

Figure 4 shows the over view of the stopping beam methods on the MPS. The MPS stops the beam at its origin by the interception of RF (2.45 GHz) at the ECR ion source. The RF can be intercepted by three different approaches: 1) intercepting the timing gate, 2) intercepting the high voltage power supply, and 3) activating a crowbar. The MPS chooses the method depending on the

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interlock classification: 1) Beam Reset To Zero (BRTZ), 2) SBI, and 3) FBI.

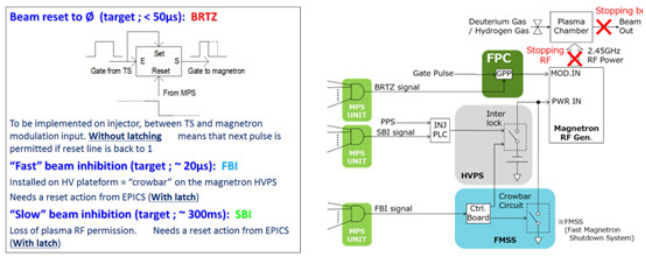

Figure 4: Over view of the stopping beam methods on the MPS.

The standard module of MPS is applied to FBI and SBI. For the BRTZ, it is necessary to add the beam stop logic on the standard module and its development is described next.

Beam Reset To Zero (< 50 µs)

This beam stopping method will be available only in pulsed operation mode and low duty cycle. The principle is that upon a MPS request, the beam pulse will be reset to zero as fast as possible by resetting the signal sent to the RF modulator (magnetron) of the ECR ion source, as shown in Figure 5. By this way, the duration of the selected beam pulse is shortened but the next pulses are again permitted as soon as the MPS signal line is back to normal state. The delay between the MPS request and the actual stop of the beam will be shorter than 50 µs. The request for this beam stopping mode could come from the RF cavities control system, etc. Such a way of stopping the beam will become a key tool during the optimization phases especially when using automatic computer-assisted tuning or RF system conditioning procedures.

For an efficient BRTZ, it is required that the timing signal of the Injector is controlled by the summarized beam stop signal which is not latched. So it is unrealizable with the MPS unit. To overcome this difficulty, we have developed a specific beam stop logic (Fast Procedure Circuit (FPC) using FPGA as additional I/F) without changing the basic configuration of MPS, which already has been used successfully in J-PARC. The reason it twofold: 1) requirement of response time is very high speed with 50 µs, and 2) additional function will be assumed. So FPGA was adapted such that high speed processing and change of logic is flexible.

Figure 5 shows the functional configuration of FPC and MPS and the functional chart.

Fast Procedure Circuit

The gate pulse for Magnetron Modulation is controlled by a BRTZ interlock signal from MPS. So we developed the FPC, as a functional addition to MPS. A gate pulse is controlled by a BRTZ interlock signal combining the standard module of MPS and FPC. FPC consists of two parts. There is an Interface (I/F) converter and a Gate Pulse Processor (GPP). An I/F converter cooperates with a MPS standard module, and performs signal processing of the received interlock signals. A GPP controls a gate pulse signal by the BRTZ signal outputted from the I/F converter.

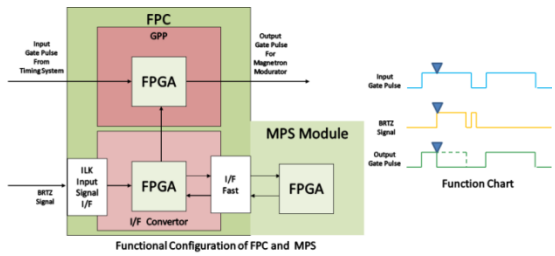

Figure 5: Functional configuration of FPC and MPS and Functional Chart.

Results of the Last Interface Tests of BRTZ

Tests between a MPS module and LIPAc injector were successfully carried out in CEA Saclay in November 2012. We measured the processing delay time, the response time of beam inhibit procedure for injector. The alert signal was measured with the help of an oscilloscope, and the response time was determined. The results obtained of these performance tests yielded for the response time of BRTZ an average of 40 µs, faster than the target 50 µs.

CONCLUSION

This paper describes the status of development of MPS using FPGA. The FPGA is an indispensable device of MPS that allows a rapid beam stop within 50 µs in compliance with the machine requirements for investment protection and 'hands-on' maintenance. The basic composition of MPS is not changed since the new interface which uses FPGA is added to MPS. It is not to be forgotten that we have already the beam stop time shorter than 30µs by FBI, in compliance with the required specifications from beam dynamics. The quick restart after a beam stop has also been taken into consideration. There is still margin for future enhancements towards a faster process to beam restart using by FPGA.

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