NEWS FROM THE FAIR CONTROL SYSTEM UNDER DEVELOPMENT

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Abstract

The control system for the FAIR (Facility for Antiproton and Ion Research) accelerator facility is presently under development and implementation. The FAIR accelerators will extend the present GSI accelerator chain, then being used as injector, and provide anti-proton, ion, and rare isotope beams with unprecedented intensity and quality for a variety of research programs.

This paper summarizes the general status of the FAIR project and focusses on the progress of the control system design and its implementation. This paper presents the general system architecture and updates on the status of major building blocks of the control system. We highlight the control system implementation efforts for CRYRING, a new accelerator presently under re-commissioning at GSI, which will serve as a test-ground for the complete control system stack and evaluation of the new controls concepts.

FAIR

FAIR is a unique new international accelerator facility for the research with antiprotons and heavy ions. When finished (planned for 2019), FAIR will be a host laboratory for basic research for about 3000 scientists from approximately 50 countries.

The FAIR accelerators are a major extension of the present GSI accelerators then being used as injectors. Figure 1 gives an overview of the full FAIR accelerator complex. FAIR will be built in a modular approach, starting with the synchrotron SIS100, two consecutive storage rings CR and HESR and the p-linac proton injector.

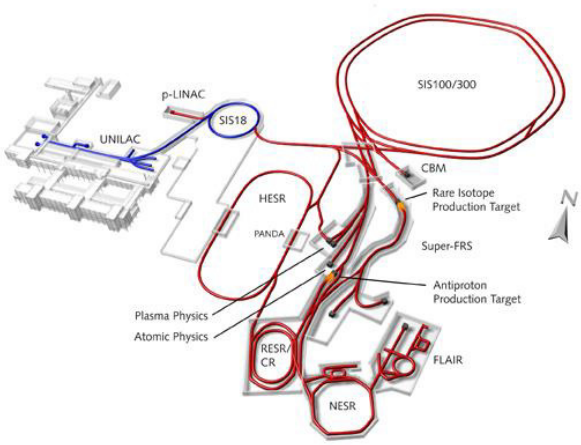

Figure 1: Schematic overview of the GSI (blue, existing) and FAIR (red, to be built) accelerator complex.

Civil Construction

The FAIR complex will cover an area of 20 hectares and require 600,000 cubic metres of concrete as well as 35,000 tons of steel [1]. Construction teams will be building a tunnel to house the heart of the complex, the SIS-100 ring accelerator with a circumference of 1.1 kilometres. The 24 buildings and several tunnels provide sufficient room for a total of 3.5 kilometers of beam-lines as well as huge detectors and a complex technical infrastructure.

Figure 2 gives an impression of the construction site. After clearing and preparing the construction area, approximately 1350 bore piles have already been built to stabilize the subsoil, minimize building settlement and ensure that buildings will settle evenly.

Moreover, several kilometers of access roads have already been built across the site for the construction site traffic.

Figure 2: Aerial photo of the construction site taken on May 25, 2014 (photo: J. Schäfer, FAIR).

CONTROL SYSTEM OVERVIEW

The FAIR accelerator control system comprises the full electronics, hardware, and software to control, commission, and operate the GSI/FAIR accelerator chain with multiplexed parallel beams. The development of the control system takes advantage of several collaborations with CERN by using, adapting and improving framework solutions like the settings management framework LSA, the front-end software framework FESA and the White Rabbit (WR) based timing system as core components.

The general structure of the FAIR accelerator control system is organized in three layers. The equipment layer consists of equipment interfaces, embedded system controllers, and software representations of the equipment. A dedicated real-time network based on White Rabbit is used to synchronize and trigger actions on equipment level. The middle (business) layer provides

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service functionality to both the equipment layer and the applications layer. The application layer combines the applications for operators as GUI applications or command line tools written in Java. The next paragraphs especially focus on several systems out of these three layers.

EQUIPMENT CONTROL HARDWARE

The standard equipment controller for most accelerator devices, with the exception of beam instrumentation DAQ systems and industrial type accelerator infrastructure systems (e.g. vacuum components), is the Scalable Control Unit (SCU). The SCU provides a uniform platform connected to both the timing- and Ethernet communication network and is designed to real-time control and synchronize equipment actions of up to 12 purpose-built slave cards, connected in a proprietary 3 HU crate by a parallel backplane bus.

Slave boards provide additional functionality and the necessary hardware interfaces to control the actual accelerator components, e.g. a wide range of magnet power converters, RF components, etc.

Status

After intensive testing of 50 SCU engineering samples in a dedicated test environment last year, a minor redesign was recently performed to address some remaining issues and slightly modify the front plate interface. Presently a first batch of 100 pre-series SCUs is being produced. The production of 600 units for FAIR is presently prepared and shall be completed by the end of 2015.

As part of the SCU solution toolkit several slave boards have been developed. Besides a general purpose AD/DA board (2 channels each) a complex FPGA rear board has been developed that can be equipped flexibly with a set of low-complexity front-side interface boards (see Figure 3). This approach greatly reduces development effort and was inspired by the need to produce several DIO and DA boards to control legacy CRYRING equipment. Furthermore, a board was developed that features the MIL-1553 field-bus that allows to connect to the present GSI timing system and control present (non-FAIR-standard) GSI equipment with SCU controllers as part of our future strategy to control “legacy” equipment.

In order to feature real-time data supply for ramped accelerator equipment, a Function Generator (FG) functionality was developed. Up to 12 function generators can be implemented in slave-board FPGAs and can be controlled from one SCU [2].

FRONT-END SOFTWARE FRAMEWORK

Software for the Front-End equipment control computer will be developed using the FESA (Front-End Software Architecture) framework, which was originally established by CERN. In collaboration between CERN and GSI the framework was redesigned completely. The new version, FESA3, is now ready to be used in a production environment.

Emphasis in the redesign was on customization to specific needs of the contributing institutes. In all layers of the framework, a common core can be extended by site specific packages [3]. This modular allows establishing a GSI-specific set of standard properties, common for all devices, and to integrate the FAIR timing system with its proposed multiplexing concept. Providing the framework as set of RPM packages easily supports installation at any location where front-end software is developed.

First FESA3 front-end software has already been developed for an ion source test-bench. Several FESA classes are under development now and will be used in the CRYRING which will be the first machine to be operated completely with the FAIR control system.

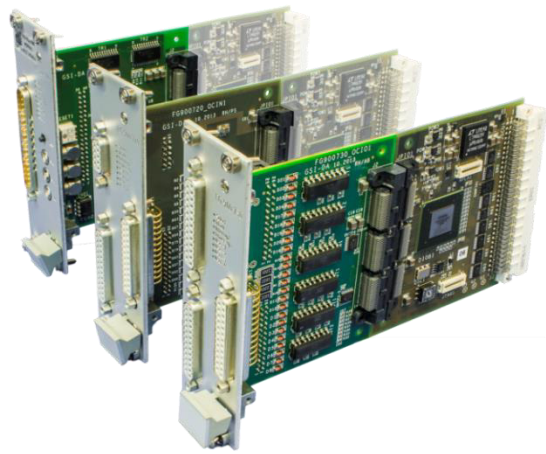

Figure 3: Modular SCU slave board concept: Complex rear-board with several types of simple front-interfaces.

SETTINGS MANAGEMENT

LSA (LHC Software Architecture) is the settings management framework which originates at CERN and since a few years is being enhanced in collaboration with GSI. This framework is used for settings management within the FAIR accelerator control system. The services written in Java are located in the control system’s middle (business) layer. They support offline generation of machine settings, management of these settings and sending them to all involved equipment controllers as well as programming the schedule of the timing system. The settings management is based on a physics model of the accelerators. This includes optics, twiss, machine layout, a parameter hierarchy and overall relations between parameters including calculation rules. A standardized API allows accessing data in a common way as basis for client applications for all accelerators. A set of generic client applications is already being provided that allows accessing all features of the system. They can be used as expert programs and serve as basis for institute specific application development.

LSA is already being used at GSI for certain machine development experiments at the existing synchrotron SIS18. For FAIR, the LSA system is currently being enhanced to support the demanding flexible beam

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operations [4]. It is planned to use these new features and verify them even before FAIR will be commissioned.

TIMING SYSTEM

For hard real-time control of all components of the GSI and FAIR accelerator complex, a first version of a General Machine Timing system has been implemented.

Overview

The GMT is based on a common notion of time of all connected nodes, provided by the White Rabbit Precision Time Protocol (WR-PTP) [5]. A dedicated network, based on WR switches distributes commands broadcasted by a Data Master to all Timing Receivers. Relevant commands are decoded and enqueued for timely execution. One time, none, one or more specific actions on the local configuration of the Timing Receiver are being executed. A central Clock Master serves as grand-master clock to which all nodes in the WR network synchronize their clock, phase and time. As the GMT is a time-based system, the precision for synchronising actions only depends on the quality of clock and phase synchronisation via WR-PTP and not the propagation time of commands distributed by the Data Master.

Nodes of the Timing System

The focus of the past two years has been the development of nodes of the timing system in all aspects: Hardware, Gateware (VHDL code), Firmware (embedded CPU code), drivers and software. The hardware for the form factors PCIe, VME and standalone has been implemented. Another form factor, the Scalable Control Unit (SCU) [3] has been integrated into the GMT too. On-time actions such as digital output, complex I/O via the SCU bus or signalling actions to the FESA software is not provided by the GMT. The key feature common to all nodes is the Event-Condition-Action (ECA) unit [6].

Data Master

The Data Master schedules actions by broadcasting commands to Timing Receivers via the WR network. A first Data Master has already been implemented based on the WR node of the form factor PCIe. The key component of the Data Master is a Lattice Micro 32 multicore cluster of soft-CPUs embedded in the FPGA of the PCIe module [7].

Status

A first version of the GMT is "ready for installation" at CRYRING. Besides, a timing network connecting six GSI buildings has been set up with about 15 WR switches. This allowed also for merging the GMT and DAQ systems and provided a decisive test on the potential stability of WR based timing systems.

NEXT STEPS: CRYRING

As Swedish in-kind contribution to FAIR, the heavy-ion storage ring CRYRING has been decommissioned in Stockholm, transported to GSI, and is presently being installed behind the existing GSI Experimental Storage Ring (ESR) [8]. CRYRING (see Figure 4) can decelerate, cool and store heavy, highly charged ions that can come from ESR down to a few 100 keV/nucleon. It is equipped with its own injector line that will allow CRYRING operation even while the full GSI accelerator chain is shut-down until mid of 2017 for necessary FAIR upgrade and civil construction work.

As CRYRING has been dedicated as a test ground for the FAIR accelerator control system (as well as for a variety of other technical subsystems), the next step is to set up the control system for re-commissioning CRYRING in the next months. The main intention is to test and validate fundamental concepts, technologies and gaining experience under real conditions in order to identify possible design flaws or limitations, and to assure the quality of the control system components involved. While in the beginning the control system and its building blocks will only provide basic features, the intention is to add more and more functionality in the coming control system releases.

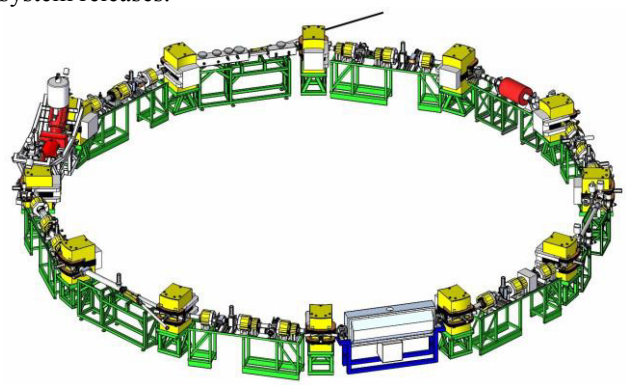

Figure 4: Overview of the storage ring CRYRING under installation at GSI (injection lines not shown).

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