

Recent Highlights From Cosylab

Mark Plesko
mark.plesko@cosylab.com

October 16th 2014

Your **TRUSTED** Control System Partner



It Began A Long Time Ago At A PCaPAC Workshop

ANKA Control System Takes Control



IGOR VERSTOVSEK
J. Stefan Institute
igor.verstovsek@ijs.si
<http://kgb.ijs.si/KGB>

Presented at the PCaPAC
Workshop, 9.-12.10.2000









They certainly won't
get any business with
DOOCS





Mr. Barroso, just
sign here for a
Billion EUR
project...



But can it
be done?

EPICS, TANGO,
LabView, whatever!
We'll do it!

EU
Commissioner

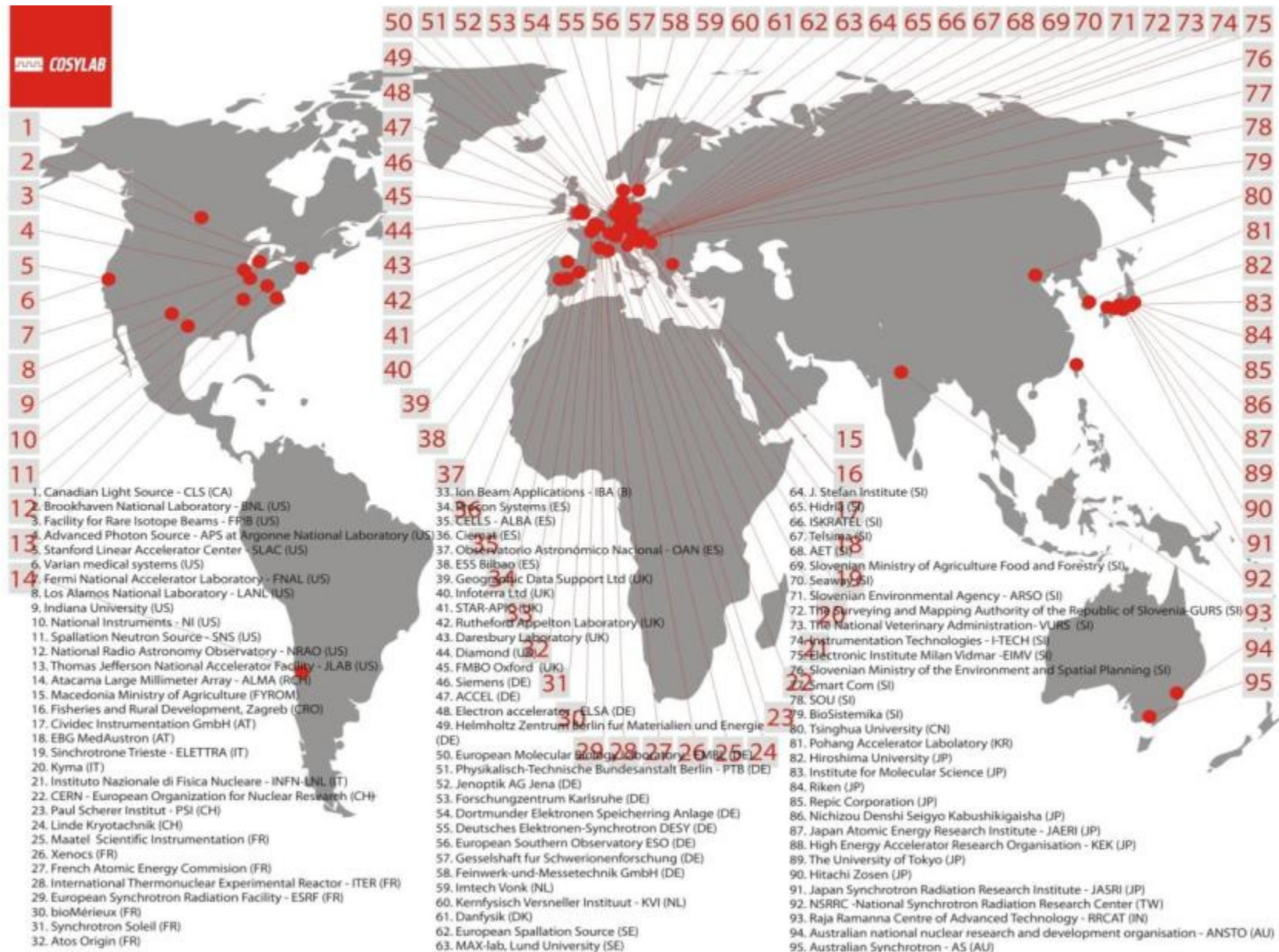
Chinese
Minister

And Somehow, They Did....

- ❑ 95 employees
 - 70 „production“ FTEs effectively
 - additional ~30 students in the pipeline
- ❑ Branches in the USA, Sweden, Japan and China



Customers From All Major Laboratories Worldwide



Turnkey Control System with TANGO: Build a Complete CS in 1.5 years!



- ❑ Cosylab integrates control system of the first Polish synchrotron lightsource facility



- ❑ Why it works:

- Open-source frameworks vs. proprietary systems: different support systems
 - Cosylab is a long-time active member of TANGO community = guarantee for repeated results

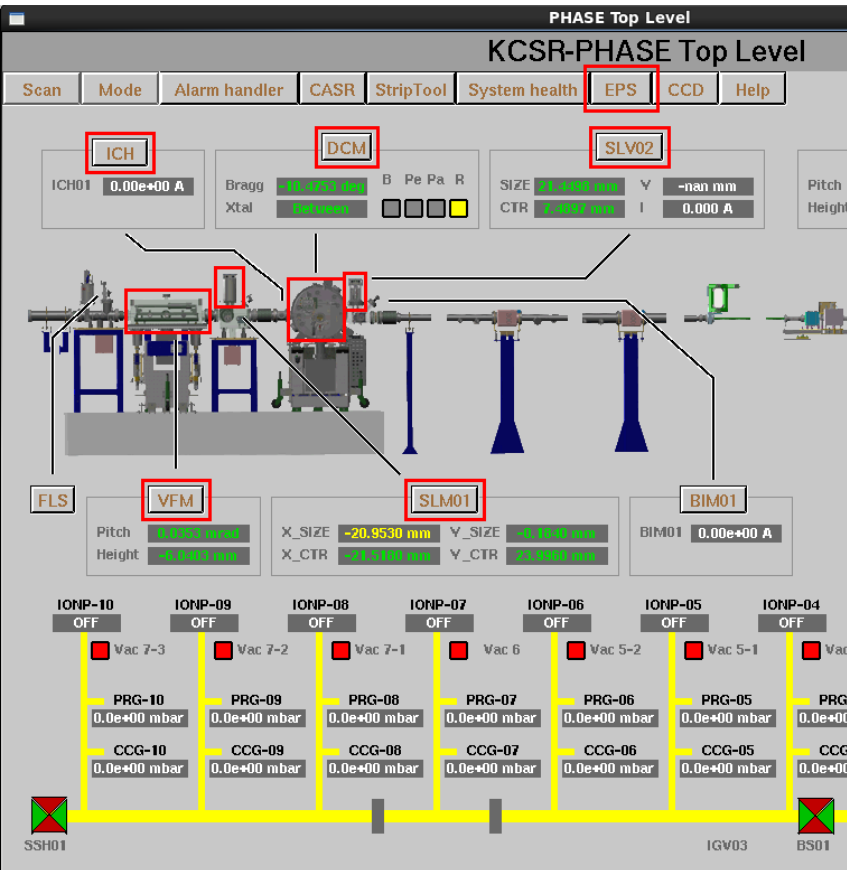
- Other examples of Cosylab Tango work
 - EPU-61 Undulator integration for MAX-IV
 - French Wind Tunnel Experiment
 - Onsite Tango training, basic and advanced

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Turnkey beamlines (EPICS and TANGO)

12



- ❑ Beamlines for Kurchatov (Russia) and INDUS (India) in 2012 via FMB Oxford
 - ❑ PMAC motion controller (Delta Tau), motor record
 - ❑ Pre-fabricated software components (cheaper cost)
 - ❑ Most work with configuration, integration and testing
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Core System Packaging For ITER and ESS



☐ Packaging infrastructure:

- ☐ builds and packages CCS components to provide **CCS distribution**
- ☐ builds and packages I&C projects developed by plant system I&C **suppliers**
- ☐ coherent RHEL RPM based packaging compliant with **CODAC** and **RHEL standards**
- ☐ easy to use interface (*mvn package* does it all)
- ☐ supports multiple CCS version installation with version switching



☐ Build integration infrastructure:

- ☐ dependency and configuration management for CI **Jenkins** jobs
- ☐ automated deployment on distribution server (**RHN Satellite Server**)

Make NI Cards Useable in Linux

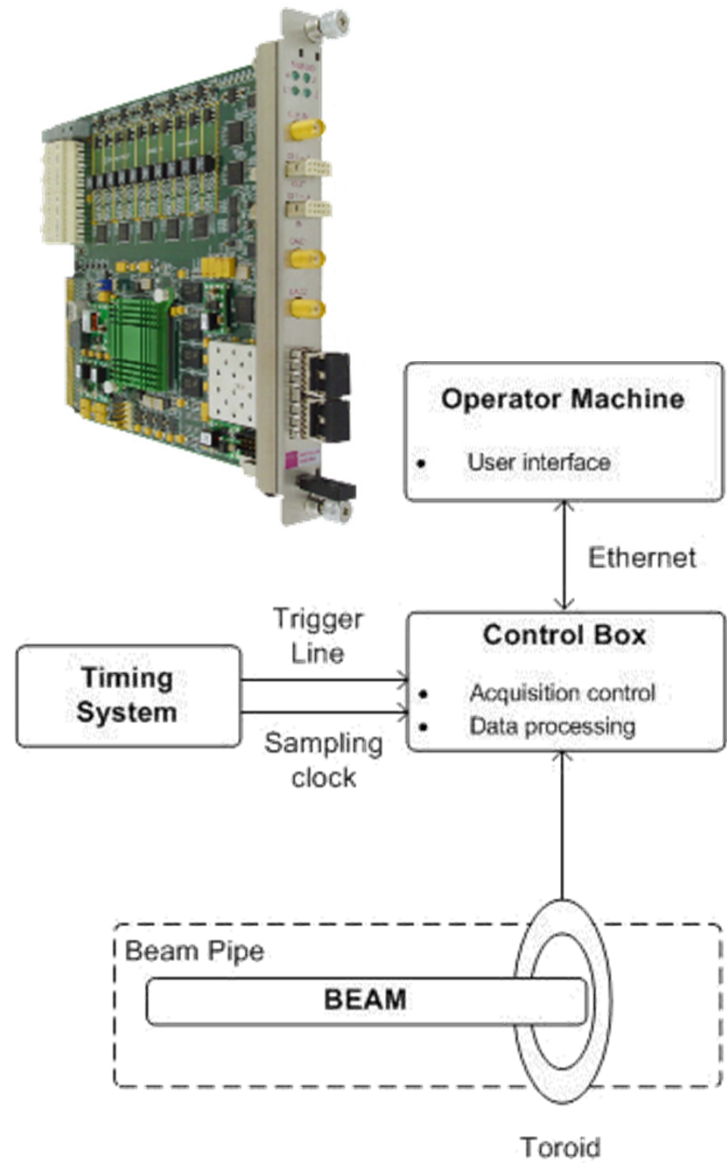


- ❑ Native Linux drivers for Data Acquisition and time&synchronization devices (PXI-6882, PXI-6259, PXI-6528, PXIe-6368, PCI-1588)
- ❑ Linux versions >2.6.20, including pre-emptive RT patch support
- ❑ Complete support of hardware capabilities
 - Initialization
 - Configuration through registers
 - Data exchange using interrupts and/or DMA
 - Health monitoring
- ❑ Interaction with drivers through C API and EPICS
- ❑ Heavily tested in Lab and real environment

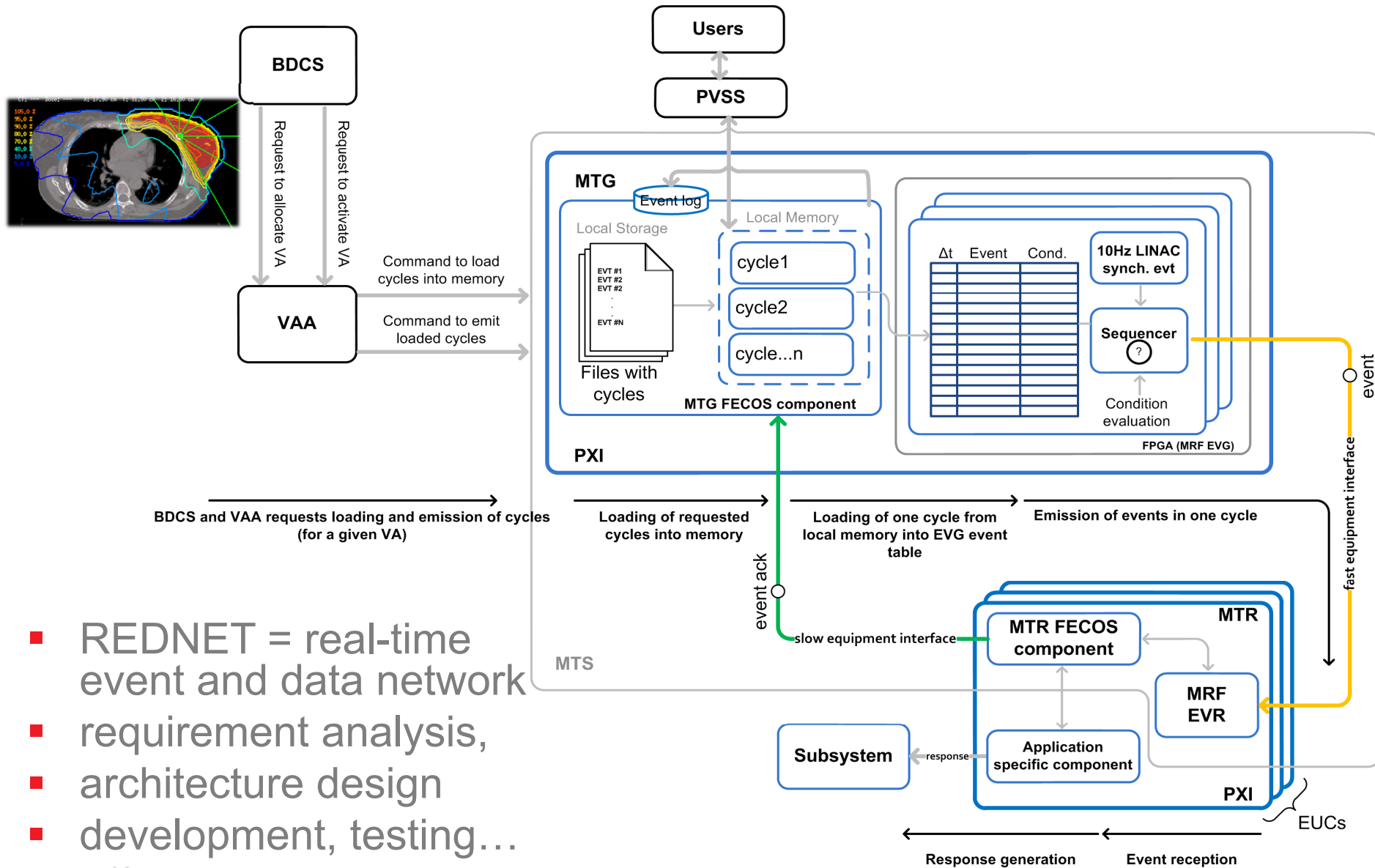


ESS BCM:

- ☐ Beam current measurement with a ACCT transformer.
- ☐ Triggers and clock from timing system.
- ☐ Process data between pulses.
- ☐ Implemented on Struck SIS8300 fast digitizer with SIS8900 RTM.
- ☐ Integrated into EPICS using NDS.
- ☐ **Firmware modifications in FPGA** to allow differential current measurements.



MedAustron: Timing System

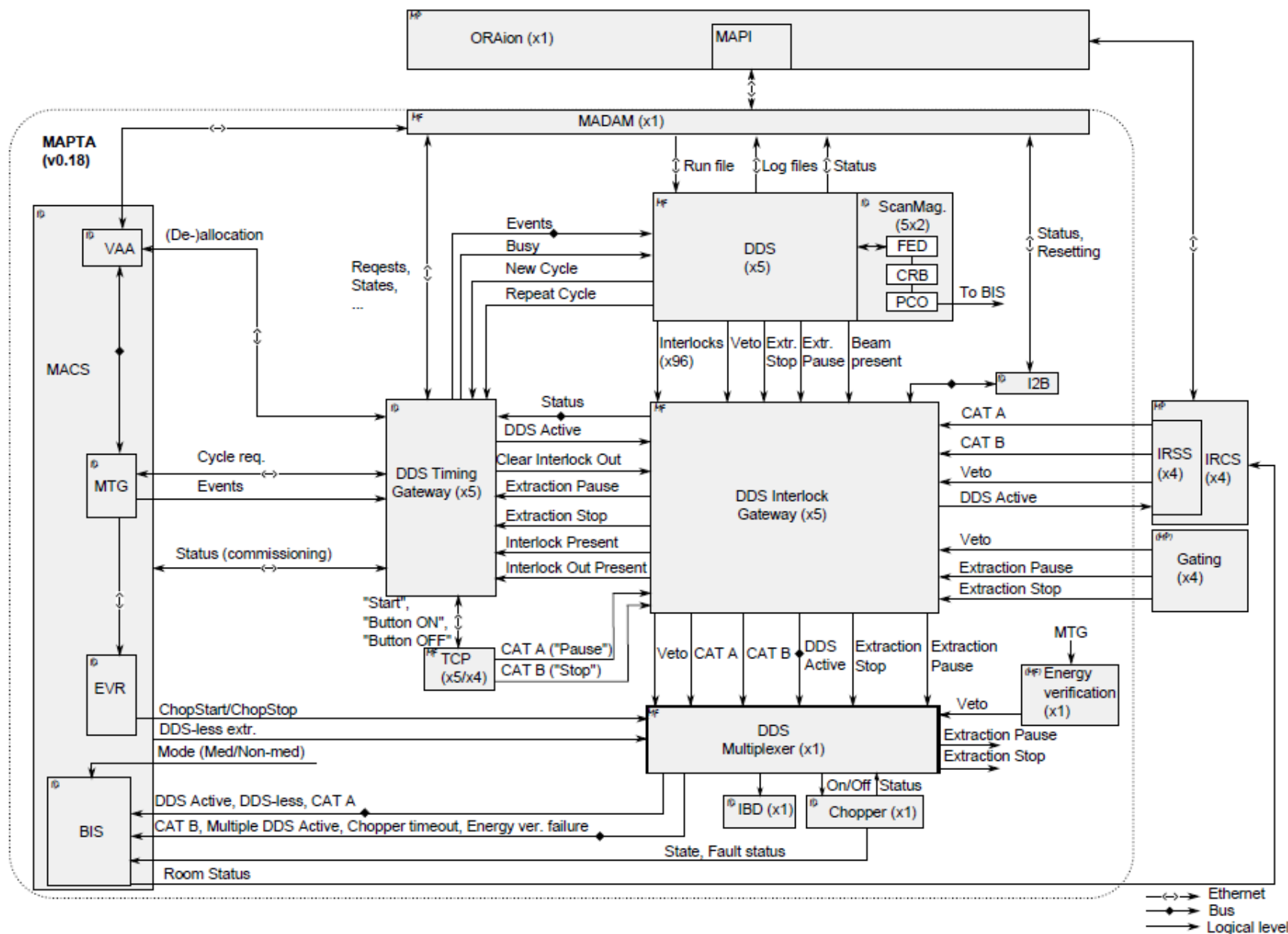


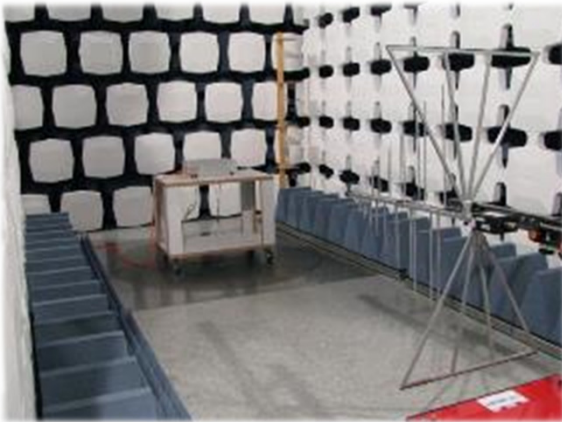


- REDNET = real-time event and data network
- requirement analysis,
- architecture design
- development, testing...

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Dose delivery system: 4x more effort than just programming





- Synchronous control of 300 different power supplies; static and waveform



HOW TO MANAGE ALL THOSE PROJECTS?

Top Level Engineering Process for Full Scale, Turnkey CS

Accelerator Development

conceptual design

Simulation

Simulation

Simulation

Machine

lattice v0.1

lattice v1

lattice v2

lattice v3

Detailed Study

Project Execution

Commissioning

Operation

Control System

High Level CS Reqs

Design v1.0.

Top Down Design Refinement Process

iterations

Middleware based Blueprint

Requirements Elicitation and Management

Control Box

standardized building block

Bottom up realization Process

Control System

Vertical Prototypes

dB Blueprint

database expansion

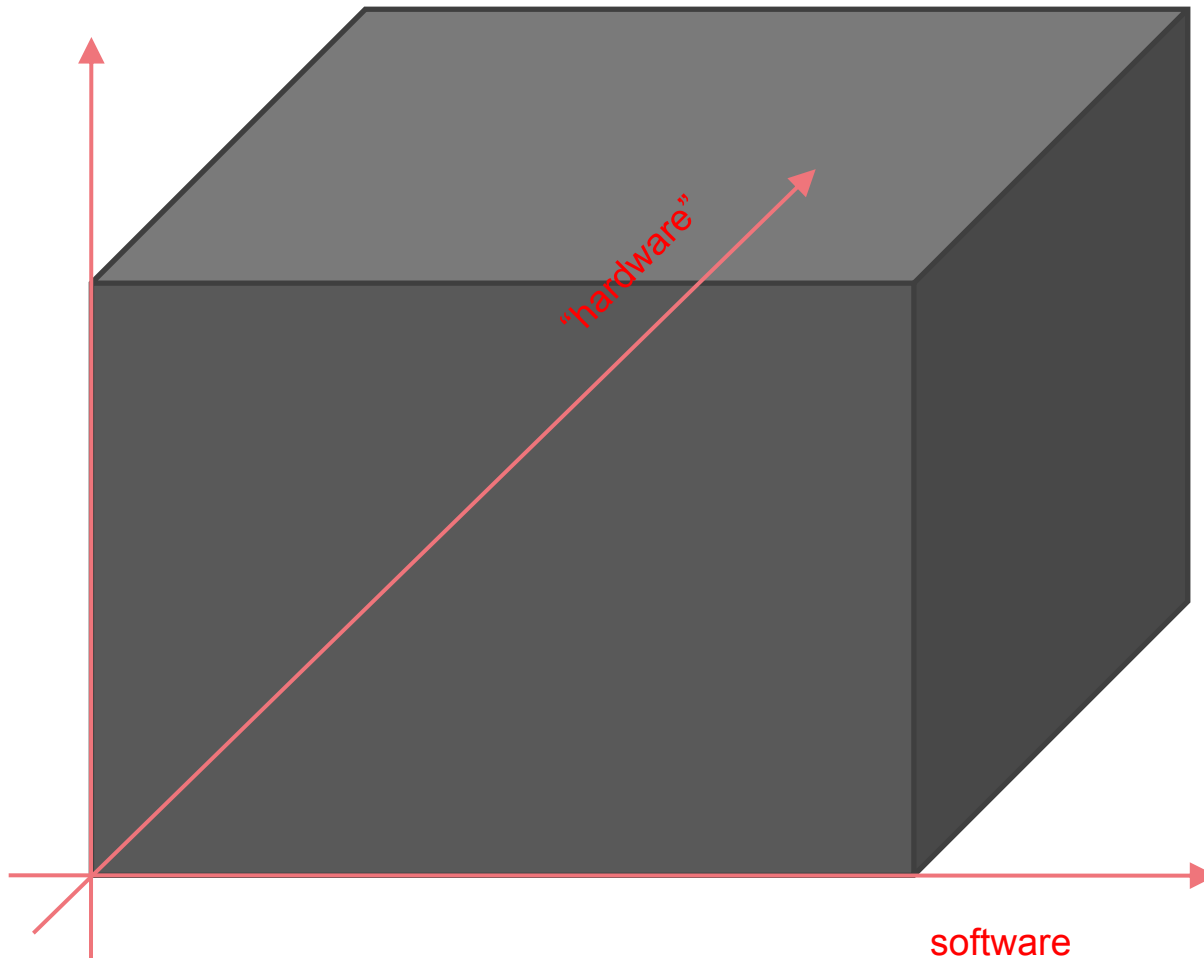
Support Process

Staff Training

Let's talk dimensions



integration know-how



Your **TRUSTED** Control System Partner

Let's talk dimensions

integration know-how

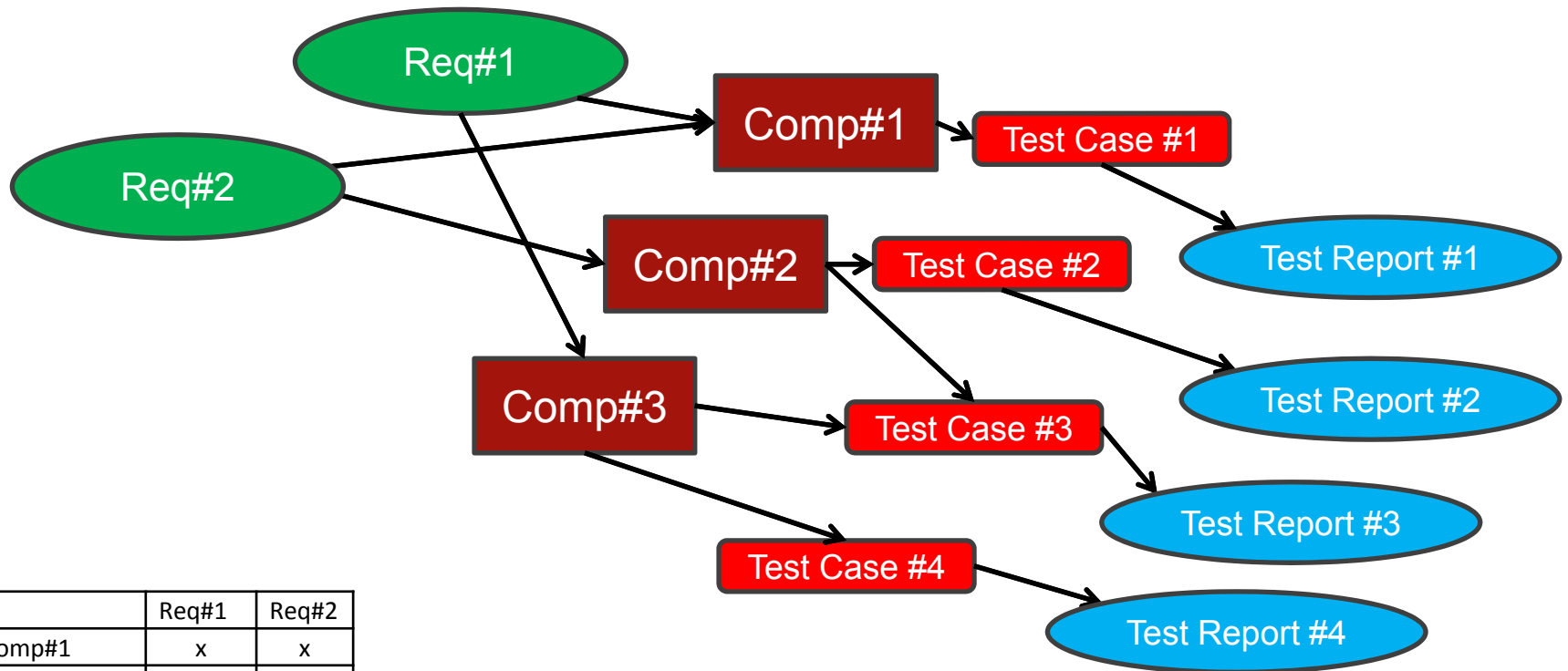


Let's talk dimensions

integration know-how



All requirements must be met



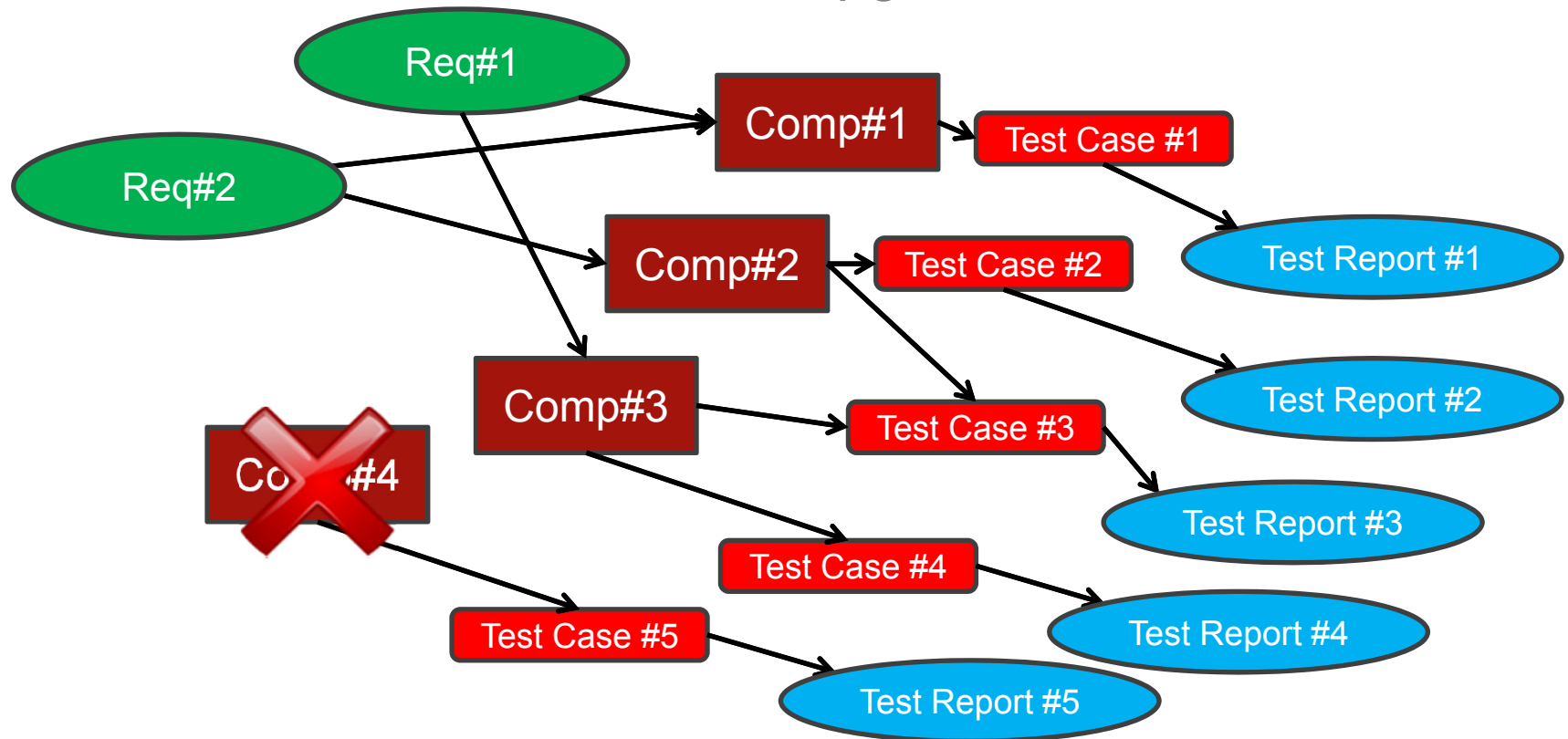
	Req#1	Req#2
Comp#1	x	x
Comp#2		x
Comp#3	x	

	Comp#1	Comp#2	Comp#3
Test Case #1	x		
Test Case #2		x	
Test Case #3		x	x
Test Case #4			x

Every component of the system must be there for a reason

- ❑ Prevent over-engineering
- ❑ Reduce maintenance and upgrade

	Req#1	Req#2
Comp#1	x	x
Comp#2		x
Comp#3	x	
Comp#4		



Traceability matrix



Source: Requirements Model

...

Type: <All>

Link Type: Realization

Profile:

Target: Technical Specifications

...

Type: <All>

Direction: Both

Refresh

Options

	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific materials::FS-DT-SM#	Specific signals::FS-FG-SS#01	Specific signals::FS-FG-SS#02	Specific signals::FS-FG-SS#03	Specific signals::FS-FG-SS#04	Specific signals::FS-FG-SS#05	Specific signals::FS-FG-SS#06	Specific signals::FS-FG-SS#07	SPI interface::FS-FG-C#04	SPI interface::FS-FG-C#05	SPI module::FS-FG-FPGA#11	SPI module::FS-FG-FPGA#12	Storage conditions::FS-DT-ET#	Storage conditions::FS-DT-ET#	Storage conditions::FS-DT-ET#	Technical Specifications::Apper	Technical Specifications::Apper	Technical Specifications::Design	Technical Specifications::Functi	Technical Specifications::Introdu	Technical Specifications::Purpo	Temperature measurement::FS	Testability::FS-DT-T#01	Testability::FS-DT-T#02	Visual signalling::FS-FG-VS#01	Working conditions::FS-DT-ET#	Working conditions::FS-DT-ET#	Working conditions::FS-DT-ET#	
On board peripherals::#R16																																					
On board peripherals::#R17																																					
On board peripherals::#R18																																					
On board peripherals::#R19																																					
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Start Page

Relationship Matrix

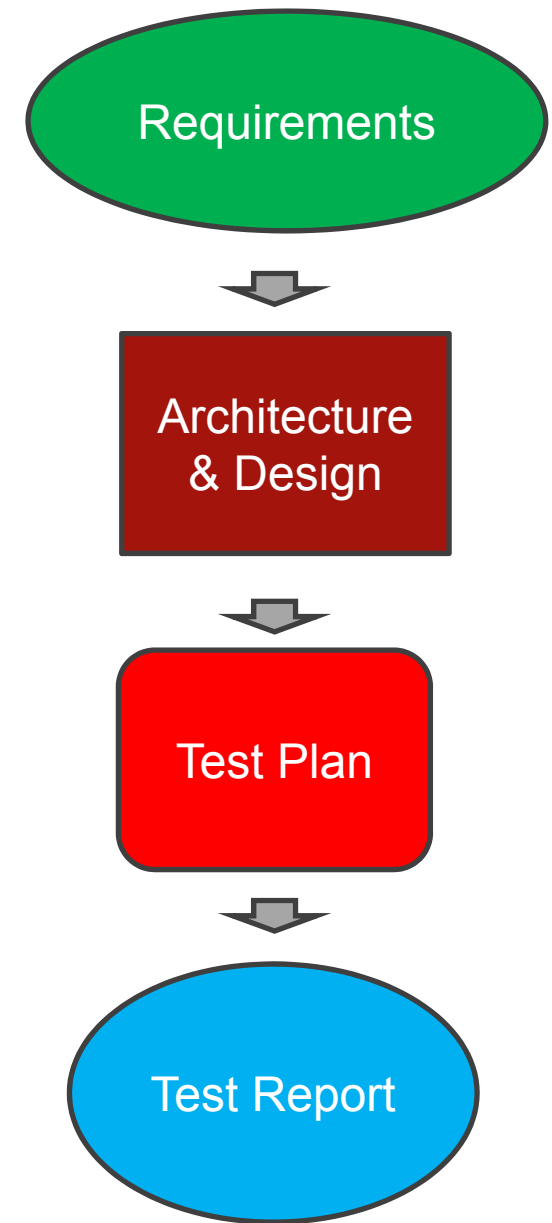
Start Page



Relationship Matrix

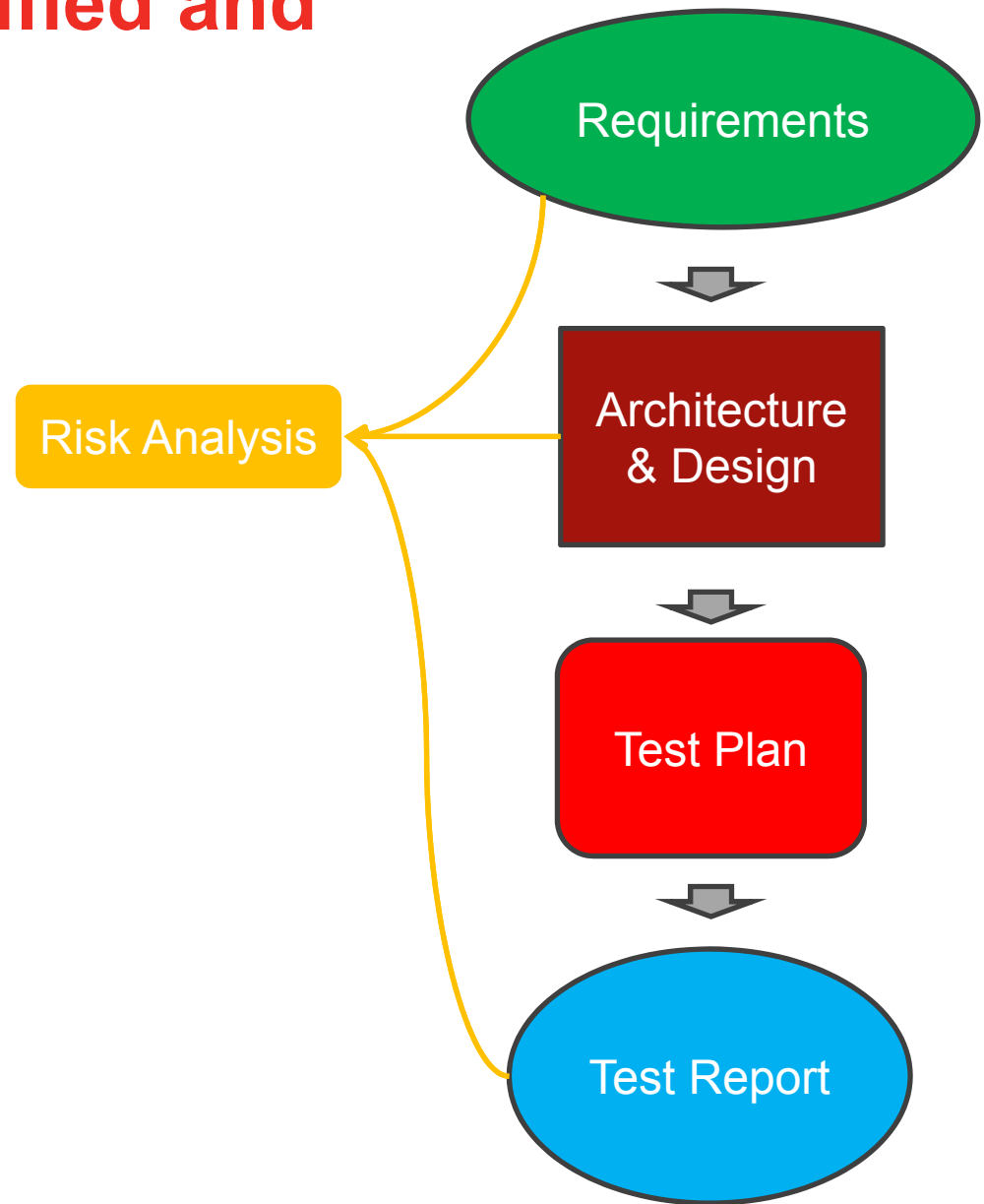
Risks must be identified and mitigated

- ☐ Certain device risks can result from faults
- ☐ Take appropriate actions to minimize the risks
- ☐ Verify that taken actions minimize the risks



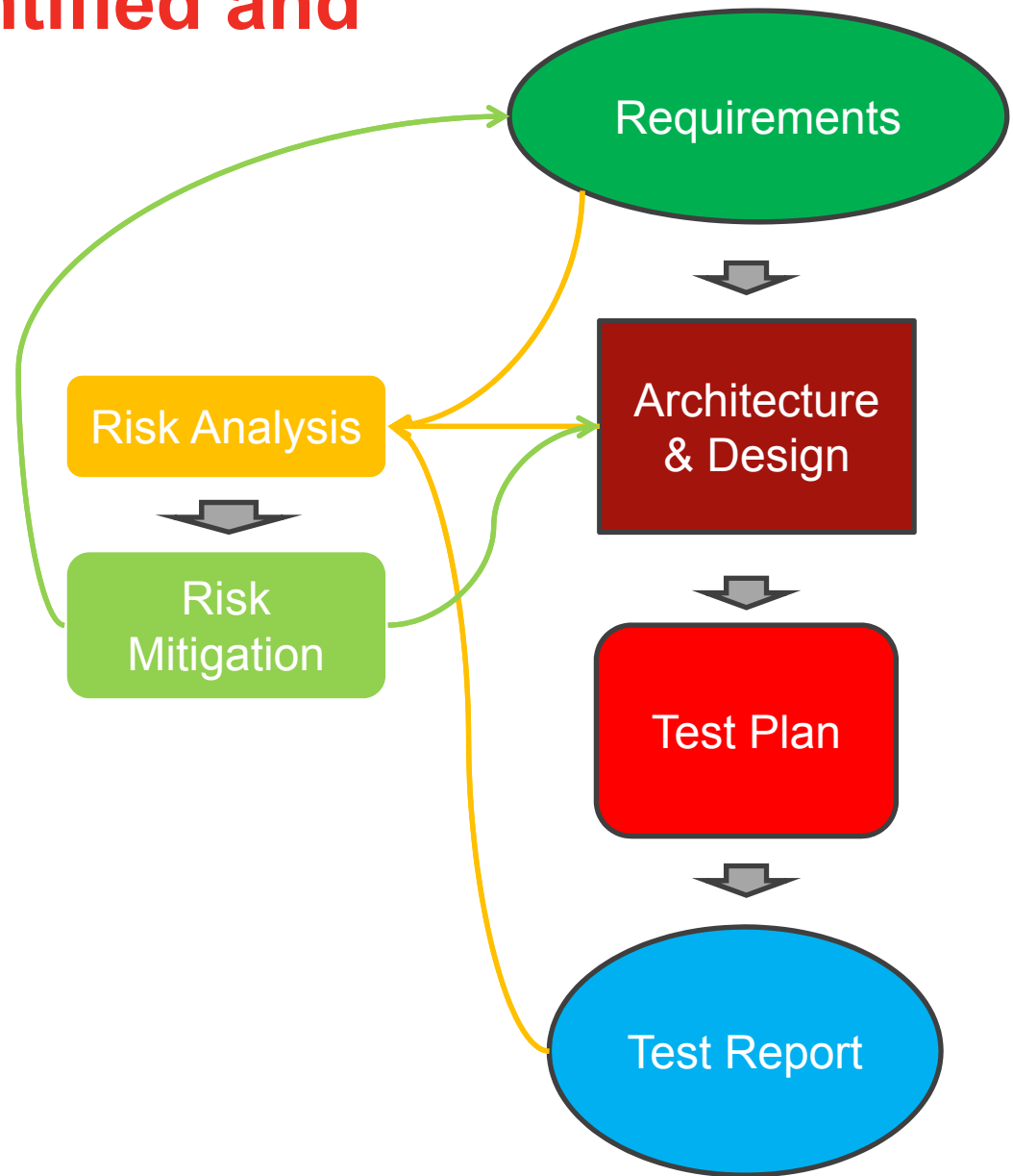
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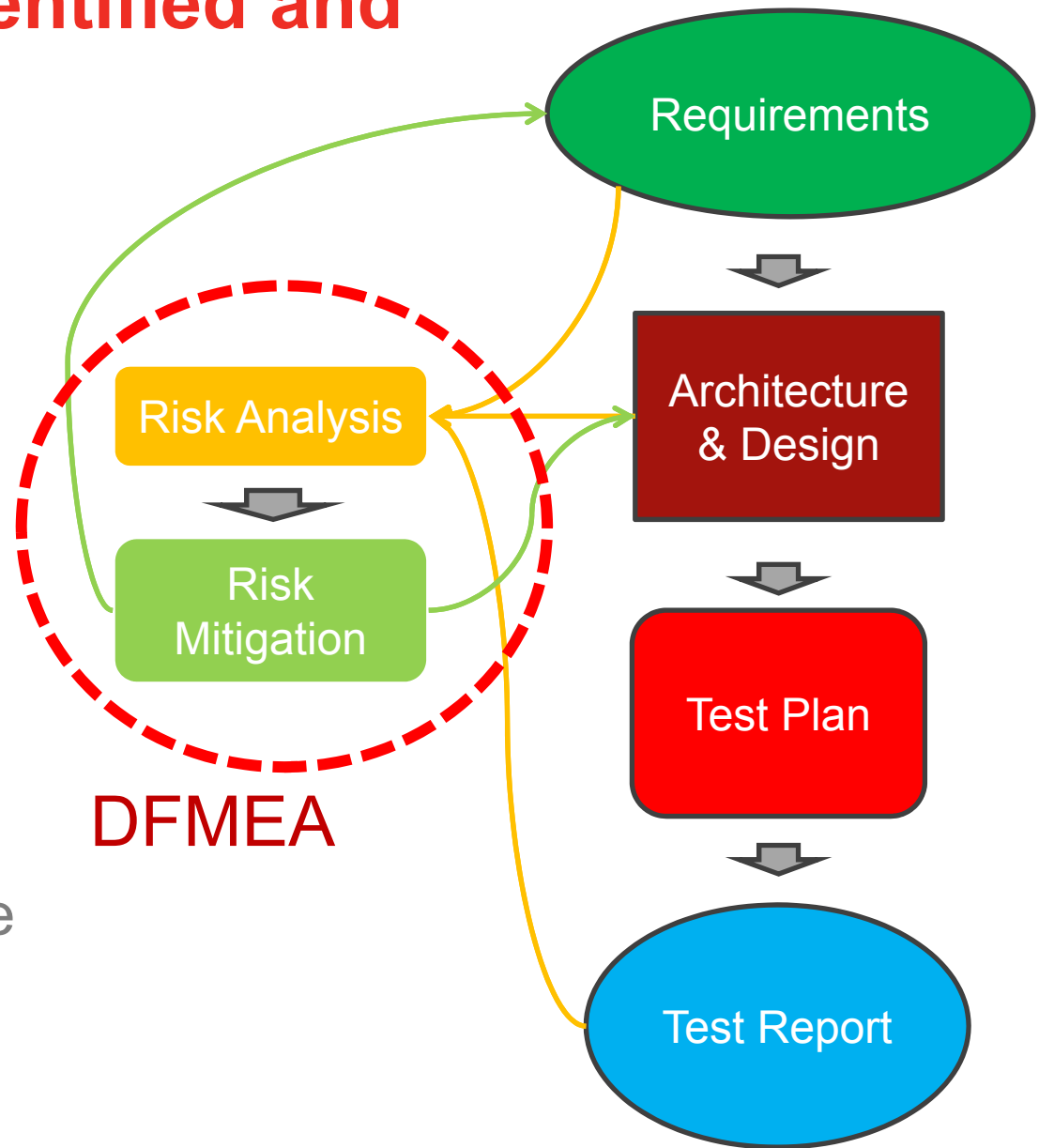
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DFMEA Design Failure Mode and Effects Analysis



- ❑ Key functions of the design are inspected
- ❑ Primary potential failures and causes of each failure are identified
- ❑ Actions are taken to reduce final risk

ID	Potential Failure Mode	Potential effect(s)	S	Potential cause(s) of failure	O	Detection Method / Current Design Controls	D	RPN	Initial Risk	Recommended action(s)	Responsibility	Action Taken	Completion Date	Final S	Final O	Final D	Final RPN	Final Risk
Identification number for each Failure Mode	How failure may occur?	Potential consequence of the failure	Initial Severity (1-5)	Functional root cause of the listed Failure Mode	Initial Occurrence (1-5)	Planned method for detecting or limiting a failure	Initial Detectability (5-1)	Initial Risk Priority Number (S x O x D)	Initial Risk Level: Minor, Moderate, Major	Action(s) to reduce severity, occurrence, detection	Responsible person or area	Description or doc reference	Date of completion	Final Severity (1-5)	Final Occurrence (1-5)	Final Detectability (5-1)	Final Risk Priority Number (S x O x D)	Final Risk Level: Minor, Moderate, Major
section 1: CAN Interface																		
1.1	Unable to communicate with Section Controller board	Instrument unable to complete current analytical test or test not started.	3	CAN transceiver chip failure due to ESD	2	Supervisor Board is designed in order to be mounted into an instrument which has to be compliant with EN61000-4-2	4	24	Minor	1. Add CDA4C20GTAESD protection diodes 2.CAN Interrupt for BUS Error Management (Supervisor FW)	1.Supervisor HW - Cosylab design team 2.FW Supervisor - bMx design team	TBD	TBD	3	2	1	6	Minor
1.2	Unable to communicate with Section Controller board	Instrument unable to complete current analytical test or test not started.	3	CAN connector failure	3	Connector suitable for the number of disconnection/ connection cycles expected in instrument life.	5	45	Moderate	1.FW communication control between Supervisor and Section Controller Boards	1.FW Supervisor - bMx design team	TBD	TBD	3	3	1	9	Minor
1.3	Unable to communicate with Section Controller board	Instrument unable to complete current analytical test or test not started.	3	CAN connector pulled out	3	None at the PCB level	5	45	Moderate	1.FW communication control between Supervisor and Section Controller Boards	1.FW Supervisor - bMx design team	TBD	TBD	3	3	1	9	Minor
1.4	Data errors on received data	Incorrect results	4	CAN lines are not properly terminated	4	CAN bus exhibits HW data integrity	2	32	Minor	1.CAN Interrupt for BUS Error Management (Supervisor FW)	1.FW Supervisor - bMx design team	TBD	TBD	4	4	1	16	Minor
section 2: SPI 1 Interface																		

Before the start of a project

Proposal

Open a
project

Active
project
supervision

Support

Closing a
project

WBS

WBS #	Phase	Task	Effort [md]	Subtask effort [m]	Comment	Effort [%]	Start	End	2003.03	2003.04	2003.05	2003.06	2003.07	2003.08	2003.09	2003.10	2003.11	2003.12	2004.01	2004.02	2004.03	2004.04	2004.05	2004.06	2004.07	2004.08	2004.09	2004.10	2004.11	2004.12
1		Specifications & Design	17			9%	29.03.12	02.04.12																						
1.1	A	One person to GSI to get requirements		3	go on site and get the specs. cover the scope of SW support, define interfaces		29.3.12	02.04.12																						
1.2	A	Write up specifications, SW		3	defining HW issues: different encoders, 200m cables, mechanics precision, required interfacing		4.4.12	08.04.12																						
1.3	A	Write up specifications, HW		3	Tender specifications, customer and third party documentation		8.4.12	10.04.12																						
1.4	A	Understanding specifications and studying		5	Presentation of acquired specs and proposed solution. GSI accepts the proposed solution		4.4.12	10.04.12																						
1.5	A	Present document at GSI, discussions		3			12.4.12	16.04.12																						
2		Final Design Review	5			3%	17.04.12	23.04.12																						
2.1	B	Final Design Review		5	Visit		17.4.12	23.04.12																						
3		EPICS GUI	8			3%	25.04.12	26.04.12																						
3.1	C	Scanning		2	All scanning GUI		25.4.12	26.04.12																						
3.2	C	Scanning		2	All scanning GUI		26.4.12	29.04.12																						
3.3	C	Scanning		2	All scanning GUI		27.4.12	30.04.12																						
4		EPICS database	15			8%	15.06.12	21.06.12																						
4.1	C	DCM		5	standard motors, incl. energy move		15.6.12	21.06.12																						
4.2	C	DCM		5	standard motors, incl. energy move		15.6.12	21.06.12																						
4.3	C	DCM		5	standard motors, incl. energy move		15.6.12	21.06.12																						
5		EPICS drivers / device support	5			5%	23.06.12	28.06.12																						
5.1	C	Modbus/TCP PLC		2	Testing the ASP provided driver		24.6.12	25.06.12																						
5.2	C	Modbus/TCP PLC		2	Testing the ASP provided driver		24.6.12	25.06.12																						
5.3	C	Piezo Java serial interface		5	Very few parameters need to be controlled		23.6.12	28.06.12																						
6		PMAC work	10			5%	25.06.12	01.07.12																						
6.1	C	PMAC axes configuration		5	This work may well be best done at OD or at CSL when all different motors are available		25.6.12	01.07.12																						
6.2	C	PMAC axes configuration		5	This work may well be best done at OD or at CSL when all different motors are available		25.6.12	01.07.12																						
7		Configuration Management / IT tasks	5			3%	30.06.12	03.07.12																						
7.1	D	Establish a full build environment		3	For DLSMK we got it from DLS done!!		30.6.12	03.07.12																						
7.2	D	Establish a full build environment		3	For DLSMK we got it from DLS done!!		30.6.12	03.07.12																						
8		QA: Testing and installations	19			10%	06.06.12	26.06.12																						
8.1	E	Establishment of a test stand		8	Lots of different hardware, shipments, packing, electrical connections		6.6.12	17.06.12																						
8.2	G	Bug fixing and support after acceptance		11	Bug fixing, problem solving and telephone/e-mail support after acceptance		12.6.12	20.06.12																						
9		On-site work	40			21%	22.06.12	08.08.12																						
9.1	F	Integration tests in Oxford (FAT)		20	4 man weeks		22.06.12	19.07.12																						
9.2	G	Testing and acceptance test at ASP (SAT)		20	5 man weeks		12.07.12	08.08.12																						
10		Documentation	19			10%	23.06.12	10.07.12																						
10.1	E	GUI User Manuals		8			23.6.12	03.07.12																						
10.2	E	Installation Manual		3			24.6.12	26.06.12																						
10.3	E	Technical Documentation		8			30.6.12	10.07.12																						
11		Management	19			10%	29.03.12	17.04.12																						
11.1	X	Project plan		12			29.3.12	06.03.12																						
11.2	X	Administration overhead		7	Shipments included		17.4.12	08.08.12																						

2. Documents

N: the document is not applicable for a type of project

O: the document may apply for the type of project, but is not required to be provided. If it is not provided, no explanation is necessary.

A: the document is advised for the type of project. If it is omitted, an explanation needs to be provided.

R: the document is required for the type of project. It may not be omitted.

Document type		Link to project document:	templates:
Offer	A		https://internal.cosylab.com/svn/ss/finance/CSLO/Templates/eng_CSL_(customer)_(subject)_DFR_YY_NN.doc
Order or contract	R		Order from customer: SVN link to order or proposal ticket with order link or ticket number with verbal yes from customer
Project table / Cost breakdown	R		this document
Project table / Team and resources	R		this document or project members table in project editor
Project table / Documentation overview	R		this document or SVN location where project table is provided
Project table / Risk management plan	A		this document or SVN location where risk analysis is provided
DFMEA	R		https://internal.cosylab.com/svn/acc/QA/Templates/DFMEA_risk_template.xlsx
Project proposal	N		
Customer requirements	A		location in SVN or RT ticket where requirements are stored
Requirements specification	R		RT ticket with requirements or requirements document: https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-RSP_project_name.docx
Requirements review record	R		RT ticket where review of requirements is done
Change request	R		RT ticket where this is specified
Architecture specification	R		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-DES_project_name.docx
Architecture review record	R		RT ticket where review of requirements is done
Detailed design	A		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-DES_project_name.docx
Test plan	R		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-TPL_project_name.docx
Design review record	R		RT ticket or https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-DRW_project_name.docx
Development plan	R		https://internal.cosylab.com/svn/acc/QA/Templates/T-CSL_Development_plan.docx
Code review report	R		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-CRV-Code_Review_Template.xls
User's documentation (User's manual; Reference manual; Tutorial; Developer's manual; Installation guide; Operator's manual)	A		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-MAN_project_name.docx
Test report	R		Document that can either be the output of the test plan or separate document prepared for testing
Post Mortem Report	R		https://internal.cosylab.com/svn/acc/QA/Templates/CSL_Post_Mortem.ppt
Site acceptance test report	A		validation from customer / signed test report or separate document provided by customer test report from
Validation record	R		validation from customer / signed test report or separate document provided by customer test report from
Released product	R		RT ticket where review of requirements is done
Release notes	R		https://internal.cosylab.com/svn/acc/TEMPLATE/trunk/doc/T-REI_project_name.docx
Maintenance plan	R		https://internal.cosylab.com/svn/acc/QA/Templates/Maintenance%20plan.docx

#80855: ITER: WO29 Drivers

LastEntry · Progress · Parent Time · Gantt · ProjectReport

Open · Steal ... Reply · Resolve · Meeting time

X Ticket metadata

X The Basics

Id: **80855**
 Status: **new**
 Priority: **15**
 Queue: **ACC-ITER-WO29_Drivers**

X Custom Fields

Ticket Type: *(no value)*
 Feedback: *(no value)*
 Severity: *(no value)*
 ProcessType: *(no value)*

X People

Owner: [redacted]@cosylab.com>
 Requestors: [redacted]@cosylab.com>
 Cc:
 Project Manager: [redacted]@cosylab.com>

X Dates

Created: **2012-07-19**
 Starts: **2012-07-16**
 Started: **Not set**
Last Contact: **2013-03-27**
 Due: **2013-01-31**
 Closed: **Not set**
 Updated: **2013-03-29** by [redacted]

X Links

Depends on:

Depended on by:

Hierarchy:   

80855: ITER: WO29 Drivers [new]

-  **80856: Management** [resolved]
-  **80857: Bugfixing** [resolved]
-  **80858: Documentation** [resolved]
-  **80859: Documentation** [resolved]
-  **80860: QA** [resolved]

Refers to:

80677: ITER: WO29 Drivers [resolved]

Master ticket
Contract task: cut the project in subprojects

X Links

Depends on:

Depended on by:

Hierarchy:   

80855: **ITER: WO29 Drivers** (kvc

[-] 80856: Management (kvc) [resolved]

79523: Ideas for future driver WOs (kvc) [resolved]

81578: Miscellaneous (kvc) [resolved]

81608: Driver team road-trip to ITER (kvc) [resolved]

[-] 81771: Correspondence with NI (kvc) [resolved]

81772: PTP stuff (kvc) [resolved]

81876: Project planning (kvc) [resolved]

[-] 82049: Presentations (kvc) [resolved]

82050: 2012-08-28 PTP synchronization (kvc) [resolved]

[-] 82055: Team meetings (kvc) [resolved]

82056: 2012-08-30 (kvc) [resolved]

82565: 2012-09-17 (kvc) [resolved]

83273: 2012-10-08 (kvc) [resolved]

84206: 2012-11-14 (kvc) [resolved]

84391: 2012-11-20 (kvc) [resolved]

84609: 2012-11-28 (kvc) [resolved]

87303: 2013-02-07: Preparing for SCCB (kvc) [resolved]

[-] 83050: Monthly reports (kvc) [resolved]

83051: WO29 monthly report - August 2012 (kvc) [resolved]

83948: WO29 monthly report - October 2012 (kvc) [resolved]

84794: WO29 monthly report - November 2012 (kvc) [resolved]

86355: WO29 monthly report - December 2012 (kvc) [resolved]

87421: WO29 monthly report - Januar 2013 (kvc) [resolved]

83536: Setup new KVM into test rack room 106 (kvc) [resolved]

[-] 84370: Customer meetings (kvc) [resolved]

87778: Post Mortem (kvc) [resolved]

88863: Post Mortem (kvc) [resolved]

[-] 80857: Bugfixing (kvc) [resolved]

[-] 80858: New features (kvc) [resolved]

[-] 80859: Documentation (kvc) [resolved]

[-] 80860: QA (kvc) [resolved]

☐ Only the 1st and 2nd level are planned

☐ The rest ist left to the project leader

Child tickets: work orders

[LastEntry](#) · [Progress](#) · [Parent Time](#) · [Gantt](#) · [ProjectReport](#)

Open · Steal ... Reply · Create new child ticket · Duplicate · Meeting tim

X Ticket metadata

X The Basics

ID:	81170
Status:	resolved
Estimated:	70 hours (4200 min)
Worked:	70 hours (4200 min)
Priority:	0
Queue:	ACC-ITER-WO29 Drivers

X Custom Fields

Ticket Type: (no value)
Feedback: (no value)
Severity: (no value)
ProcessType: (no value)

X Attachments

- **bug3184-1chan-f-fixed (2).bmp** (146.3k) by [REDACTED] 2012-11-23
- **PXI6259 AO Bugz.zip** (81.5k) by [REDACTED] 2012-10-18
- **bug3183-2-1chan-f-fixed.bmp** (146.3k) by [REDACTED] 2012-11-26
- **bug3184-1chan-f-faulty (2).bmp** (146.3k) by [REDACTED] 2012-11-23
- **ni6259-typo.patch** (814b) by [REDACTED] 2012-08-17
- **bug3183-2-1chan-f-fixed(old).bmp** (146.3k) by [REDACTED] 2012-11-26
- **bug3183-3184.patch** (14.5k) by [REDACTED] 2012-11-21
- **bug3183-2.c.patch** (2.5k) by [REDACTED] 2012-11-26

10 People

```
Owner: [REDACTED]@cosylab.com>
Requestors: [REDACTED]k@cosylab.com>
Cc:
Project Manager: [REDACTED]:@cosylab.com>
```

X Dates

Created:	2012-07-31
Starts:	2012-07-31
Started:	2012-07-31
Last Contact:	2012-12-14
Due:	2012-10-31
Closed:	2012-12-14
Updated:	2013-03-22 by l

X Links

Depends on:

Depended on by:

Hierarchy:

80855: ITER: WO29 Drivers () [new]

80857: Bugfixing (k...ec) [resolved] 📁

81170: Bug 3183 - M Series - GenerateWaveformOneChannel with Strange behaviour. () [resolved] 📌

Refers to:

Referred to by:

38 Ticket – work order



# 2012-11-14 13:04:0 Correspondence added	Back to 2193 specific problem. The problem in 2193 is the following: User starts AD and then inevitably stops AD and that breaks current DMA transfer (filling only part of on-board FIFO). When user switches to add new samples, a glitch appears on the output due to original samples still being present in on-board FIFO. One of the solutions is to explicitly clear AD FIFO buffer, but that might cause additional problems down the road (e.g. when someone wants retain the samples in FIFO buffer before startAD). An alternative is that we do not allow the user to break DMA transfer by returning EDOZY while the transfer is in progress. The problem I have is how to figure out whether the DMA transfer is in progress. I will discuss this options with gajdoh tomorrow...	[Reply] Download (untitled) [text/plain 364B]
# 2012-11-14 14:42:0 Correspondence added	1380 min We are finally making some progress with #264259 bugs (after a few review sessions with gajdoh, and after careful review of register traces). This is what is fixed now: > 1. vac kanalni AD. Ne da se samo se dodas extra kanal. E.g. The problem is, with higher frequency, according to R04259 specification, we should be able to output 280samples/s when using 2 channels, but we can not. It only works up to ca. 1.857samples/s. Since this is not directly related to 2193 I have stopped investigating why. > 2. nekonzistentni/nepredvidljivi/naladni startAD() in stopAD() > behaviour: > > conf.g > > unblock > > startAD() => signal f(x) > > sleep(400) > > stopAD() > > startAD() => still signal f(x) (as expected) > > conf.g > > unblock > > startAD() => signal f(x) > > usleep(400) > > stopAD() > > startAD() => signal g(x) != f(x). Polovica FIFO/DMA buffer, signal and > > da li se ga del duplicira > > (gaj screenshot) This is the actual 2193 bug. Within the scope of this bug alot of DMA code was changed so that it now works as expected. We now start the DMA transfer as soon as we have the samples in kernel buffer and we only after startAD was called. Furthermore when calling startAD with FIFO behaviour enabled we wait till DMA transfer has finished. > 3. Start DMA bl se morali vratit pred start AD > > Ker se dma prenos zacene sele ko klicemo startAD pride do (pomocjo) > > nevarnostnega odziva > > => FIFO na kartici je na zacetku prazen (ker se start DMA klice sele > > ko klicemo startAD) > > => AD je konfiguriran v FIFO naizmeniku (torej se bodo samoli) > > generiral z repetitornim vzorcem kar je > > v kodu na kartici. >	[Reply] Download (untitled) [text/plain 364B]
	2012-11-22 13:57:57 Correspondence added 120 min I was capturing waveforms concurrently for the test plan (and for future reference). It seems that in program bug2194, I can (sometimes) only trigger the signal generation once. If I trigger the first time (by generating the first waveform), I can not re-trigger (using either an RTI) the output waveform. If I don't trigger the first waveform, I then trigger the second waveform. Attaching "Test1" and "Test2" wave forms. Download bug2194 when I fixed (3)bug [image/png 146.2K] Download bug2194 when I fixed (3)bug [image/png 146.2K]	[Reply] Download (untitled) [text/plain 422B]
# 2012-11-30 15:19:29 Correspondence added	Edits to sources	35 min [Reply] Download (untitled) [text/plain 16B]
# 2012-11-30 15:32:20 Correspondence added	t for reviews.	40 min [Reply] Download (untitled) [text/plain 14B]
# 2012-12-14 11:18:45 ic - Correspondence added	Resolving.	[Reply] Download (untitled) [text/plain 10B]
# 2012-12-14 11:18:45 ic - Status changed from 'open' to 'resolved'		

Control the status of project



Planned vs. Spent time?

Work load

1.1. Time

Project budget

Project size: 17.81 md : 3.56 mw : 0.89 mm

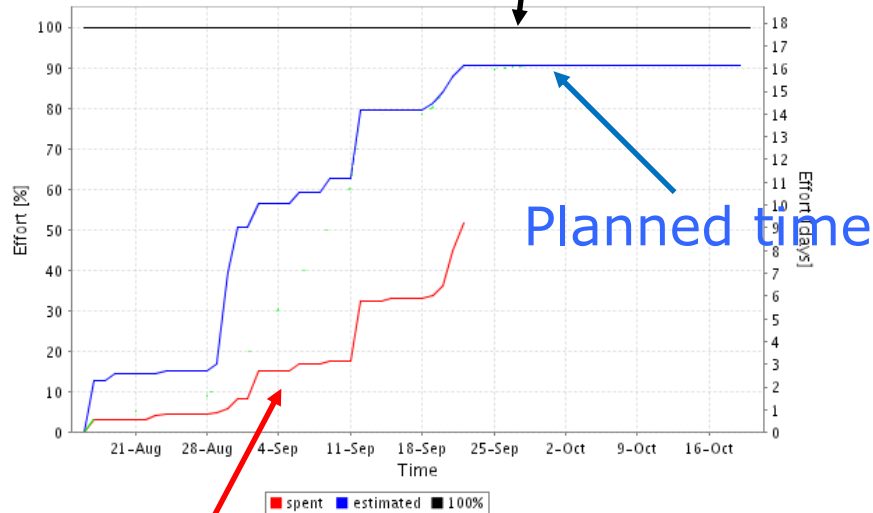
Time spent: 9.21 md : 1.84 mw : 0.46 mm (51%)

Time spent (4420/8550)



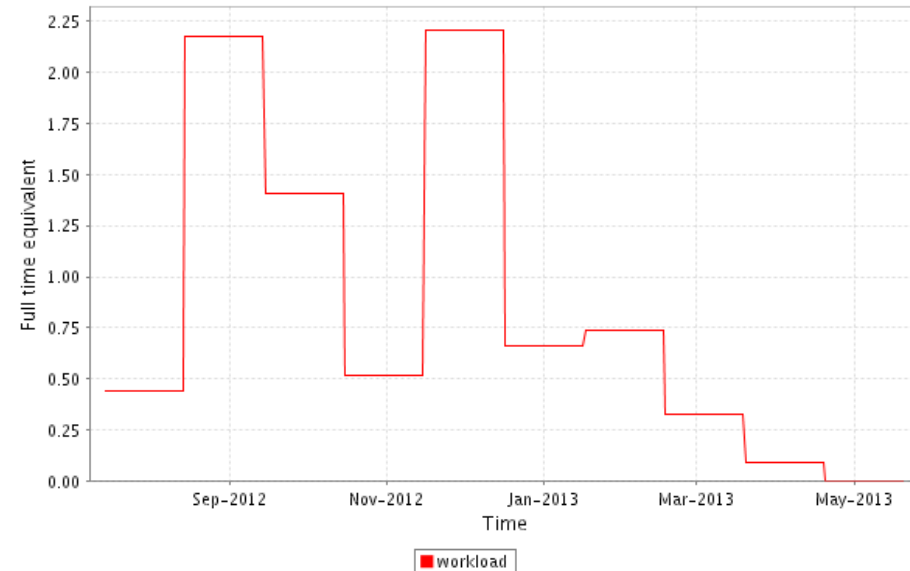
Estimated time to finish: 2.06 md : 0.41 mw : 0.10 mm

Project History

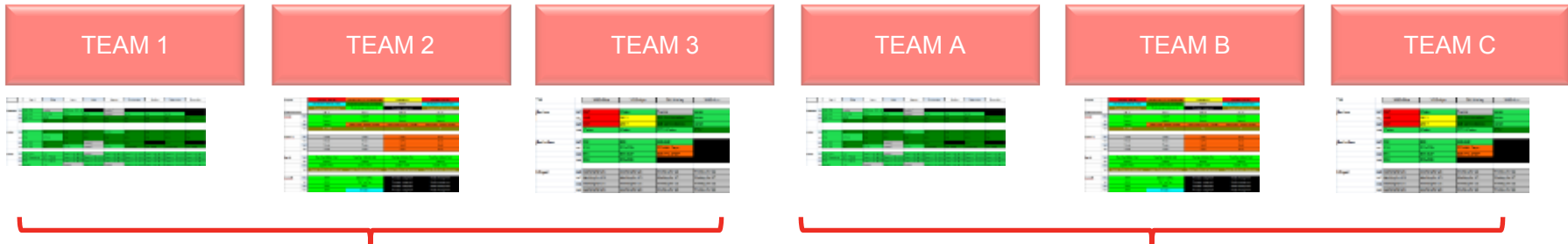


Spent time

Project Workload Chart (LF)



Planning For All Developers in Teams



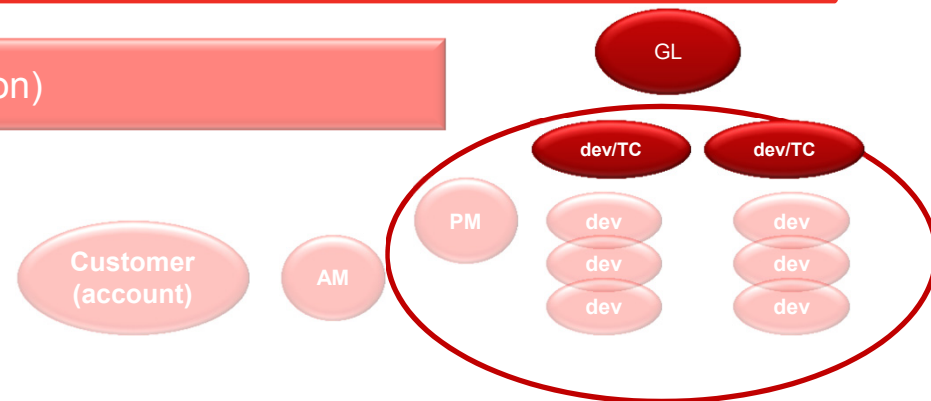
Group plan ("helicopter view" of team plans)

Group plan ("helicopter view" of team plans)

	week 20	week 21	week 22	week 23	week 24	week 25	week 26	week 27	week 28
Project events									
13.5.2013	20.5.2013	27.5.2013	3.6.2013	10.6.2013	17.6.2013	24.6.2013	1.7.2013	8	
ESS - SDO usecase	VMS - ACS/BTS/PP	ESS - SDO usecase	VMS - ACS/BTS/PP	ESS - SDO usecase	VMS - ACS/BTS/PP	ESS - CB 2013	VMS - ACS/BTS/PP	VMS - ACS	
ESS - Struck	ESS - Struck	ESS - Struck	ESS - WScanner	ESS - CB 2013	ESS - CB 2013	ESS - CB 2013	ESS - CB 2013	MYRRHA	
ABB - Prototype	ABB - Prototype	ABB - Prototype	ABB - Prototype	empty	empty	empty	empty	empty	
ESS - WScanner	ESS - WScanner	ESS - WScanner	ESS - WScanner	ESS - WScanner	ESS - WScanner	ESS - WScanner	MYRRHA - LEBT	MYRRHA	
VMS - ACS/BTS/PP	ESS - GP ADDA	VMS - ACS/BTS/PP	ESS - GP ADDA	VMS - ACS/BTS/PP	ESS - GP ADDA	VMS - ACS/BTS/PP	ESS - GP ADDA	VMS - ACS	
VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS/BTS/PP	VMS - ACS	
vacation	vacation	vacation	vacation	vacation	vacation	vacation	vacation	empty	
VMS - ACS/BTS/PP	empty	VMS - ACS/BTS/PP	DESY - APPS	VMS - ACS/BTS/PP	empty	VMS - ACS/BTS/PP	DESY - APPS	empty	
ESS - VMS	ESS - RH	empty	empty	empty	empty	ESS - BLE	ESS - BLE	ESS - BLE	
VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	
VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	VMS - RH	
GL	GL	GL	GL	GL	GL	GL	GL	GL	
FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On site	FAIR - On	
ESS - On site	ESS - On site	ESS - On site	ESS - On site	ESS - On site	ESS - On site	ESS - On site	ESS - On site	ESS - On	
VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	VMS - SPTC	



COO plan (resource utilization)

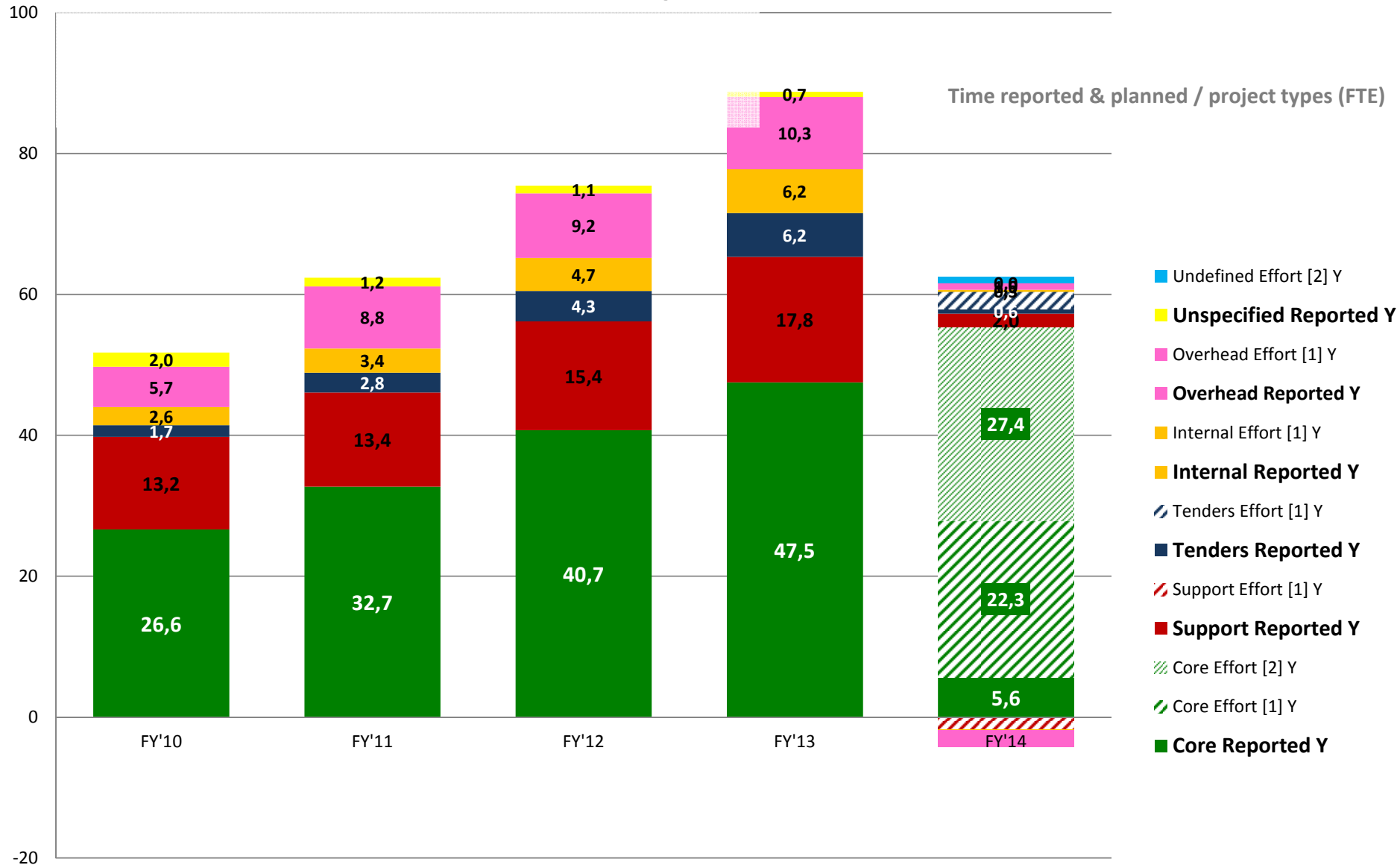


Time reported & planned / FYs (CSL)



COSYLAB

□ note: FY'14 isn't finished yet



Analyse overhead + internal work by group, team and individual person

TC	jdedic	146.4	77.1%
factor	0		
Row Labels	Sum of TimeWorked[h]	Sum of by developer	
gcuk	117.9	72.3%	
ACC div Cosylab_China_F	11.4	7.0%	
ACC-div-Education_2013	6.1	3.7%	
ACC-div-GL-2013	1.8	1.1%	
ACC-div-Overhead_2013	10.3	6.3%	
ACC-div-RP_KC_OpComm	24.9	15.3%	
ACC-div-RP_KC-STV	3.2	2.0%	
ACC-div-Sales_2013	60.2	36.9%	
jdedic	146.4	77.1%	
ACC-div-Cosylab_China_F	1.5	0.8%	
ACC div Education_2013	3.3	1.7%	
ACC-div-GL-2013	36.2	19.1%	
ACC-div-HRM_2013	4.9	2.6%	
ACC-div-MNG_2013	63	33.2%	
ACC div Overhead_2013	7.5	4.0%	
ACC-div-QA_2013	2	1.1%	
ACC-div-Sales_2013	26.8	14.1%	
ACC-div-Tavta_PhD	1.2	0.6%	
rtavcar	131.8	92.3%	
ACC div Cosylab_China_F	32.6	22.8%	
ACC-div-Education_2013	3.9	2.7%	
ACC-div-GL-2013	1.5	1.1%	
ACC-div-HRM_2013	10	7.0%	
ACC div Overhead_2013	18.6	13.0%	
ACC-div-Sales_2013	3	2.1%	
ACC-div-Tavta_PhD	40.3	28.2%	
ACC-div-White_Rabbit_Ev	21.9	15.3%	

TC	zkrotic	18.4	8.9%
factor	0		
Row Labels	Sum of TimeWorked[h]	Sum of by developer	
dperusko	18.4	8.9%	
ACC div Education_2013	2.8	1.5%	
ACC-div-GL-2013	0.5	0.3%	
ACC-div-Overhead_2013	15.1	7.3%	
dslovinc	23.8	14.0%	
ACC-div-Cosylab_China_F	1	0.6%	
ACC-div-Education_2013	1.4	0.8%	
ACC div GL 2013	0.5	0.3%	
ACC-div-Overhead_2013	20.9	12.3%	
gcijan	30.6	19.3%	
ACC-div-Education_2013	10.2	6.4%	
ACC-div-GL-2013	7.8	4.9%	
ACC div HRM_2013	0.8	0.5%	
ACC-div-Overhead_2013	10.6	6.7%	
ACC-div-Sales_2013	1.2	0.8%	
mmehle	7.1	5.1%	
ACC-div-Education_2013	0.3	0.2%	
ACC-div-GL-2013	2.9	2.1%	
ACC div Overhead_2013	5.9	2.8%	
zkrotic	34.5	20.4%	
ACC div Cosylab_China_F	1.5	0.9%	
ACC-div-Education_2013	2.2	1.3%	
ACC-div-GL-2013	17.3	10.2%	
ACC div HRM_2013	1.3	0.8%	
ACC-div-Overhead_2013	11	6.5%	
ACC-div-QA_2013	1.2	0.7%	

TC	mljevicnik	34.3	24.0%
factor	0		
Row Labels	Sum of TimeWorked[h]	Sum of by developer	
mljevicnik	34.3	24.0%	
ACC div Cosylab_China_Push_!	7.3	5.1%	
ACC-div-Diamond_Beam_Moni	1.8	1.1%	
ACC-div-Education_2013	2.2	1.5%	
ACC-div-GL-2013	1.8	1.3%	
ACC-div-HRM_2013	0.4	0.3%	
ACC div microIOC 2012	1.8	1.3%	
ACC-div-Overhead_2013	6.6	4.6%	
ACC-div-QA_2013	11.3	7.9%	
ACC div RP_CO_BIK_2012	0.4	0.3%	
ACC-div-Sales_2013	0.7	0.5%	
msitar	0.7	0.7%	
ACC div HW_2012	0.7	0.7%	

TC	Isopetavc	56.2	26.4%
factor	0		
Row Labels	Sum of TimeWorked[h]	Sum of by developer	
Isopetavc	56.2	26.4%	
ACC div Board_2012	0.2	0.1%	
ACC-div-Education_2013	16	7.7%	
ACC-div-GL-2013	10.5	5.0%	
ACC-div-HRM_2013	0.8	0.4%	
ACC-div-MNG_2013	1.8	0.9%	
ACC div Overhead_2013	23.6	11.3%	
ACC-div-QA_2013	2.2	1.1%	
ACC-div-Sales_2013	1.1	0.5%	
mklun	18.2	7.6%	
ACC-div-Education_2013	2.8	1.2%	
ACC div GL 2013	2.9	1.2%	
ACC-div-Overhead_2013	12.5	5.7%	
stuma	34.3	19.1%	
ACC-div-Education_2013	15.8	8.8%	
ACC-div-GL-2013	0.5	0.3%	
ACC div Overhead_2013	18	10.0%	

TC	rstefanic	48.6	19.0%
factor	0		
Row Labels	Sum of TimeWorked[h]	Sum of by developer	
rstefanic	48.6	19.0%	
ACC-div-Cosylab_China_Push_SINAP_Collab	5.9	2.3%	
ACC-div-Education_2013	1.2	0.5%	
ACC-div-GL-2013	17.2	6.7%	
ACC-div-HRM_2013	1.8	0.7%	
ACC-div-Overhead_2013	16.8	6.6%	
ACC-div-White_Rabbit_Evaluation	5.7	2.2%	
ulegat	50.6	35.1%	
ACC-div-Cosylab_China_Push_SINAP_Collab	52.8	31.1%	
ACC-div-Education_2013	2.8	1.6%	
ACC-div-GL-2013	1.5	0.9%	
ACC div Overhead_2013	2.5	1.5%	

Salary aligned with performance

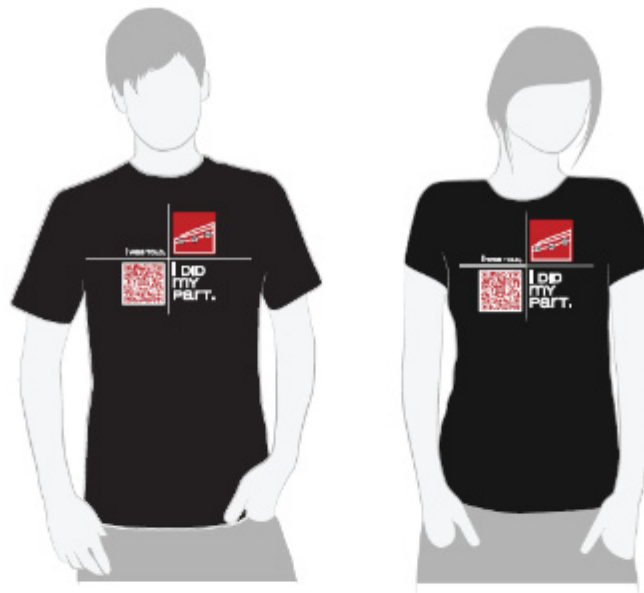


- ❑ Award pot that will be distributed on yearly basis is 200k (~15% of paid out profit).
- ❑ The longer you are at Cosylab, the more you will get
- ❑ Awards paid out quarterly, with increasing importance towards the end
 - 2013 Q3: 20% of allocated
 - 2013 Q4: 30% of allocated
 - 2014 Q1: 50% of allocated
- ❑ TC and management salaries
 - TC addition – 30% of monthly addition
 - 30% of base salary for management pay

Years at CSL	Bonus paid with salary of		
	October 2013	January 2013	April 2014
< 0,5	0	0	0
0,5	145	218	364
1	218	327	545
2	291	436	727
3	364	545	909
4	436	655	1091
5	509	764	1273
6	545	818	1364
7	582	873	1455
8	618	927	1545
9	655	982	1636
10	691	1036	1727
11	727	1091	1818
12+	727	1091	1818

But at least, acknowledge and praise their effort:

44



Your **TRUST**

Conclusion



- ❑ Project management excellence doesn't come over night
- ❑ We have the tools and skills for the control system development
 - setting standards how to do development
 - integrating numerous devices
 - responsible for accepting work from other co-suppliers (as CS developers, we understand operation of the entire machine)
- ❑ adapting internal processes (ISO 9001) to customer needs: requirements and risk management
- ❑ Not just planning, but skillful supervision in the course of the project
- ❑ We see early warnings sooner than anyone else

Thank you!

Mark Plesko
mark.plesko@cosylab.com

Your **TRUSTED** Control System Partner

