TestBed -- Automated Hardware-in-the-Loop Test Framework

COSYLAB

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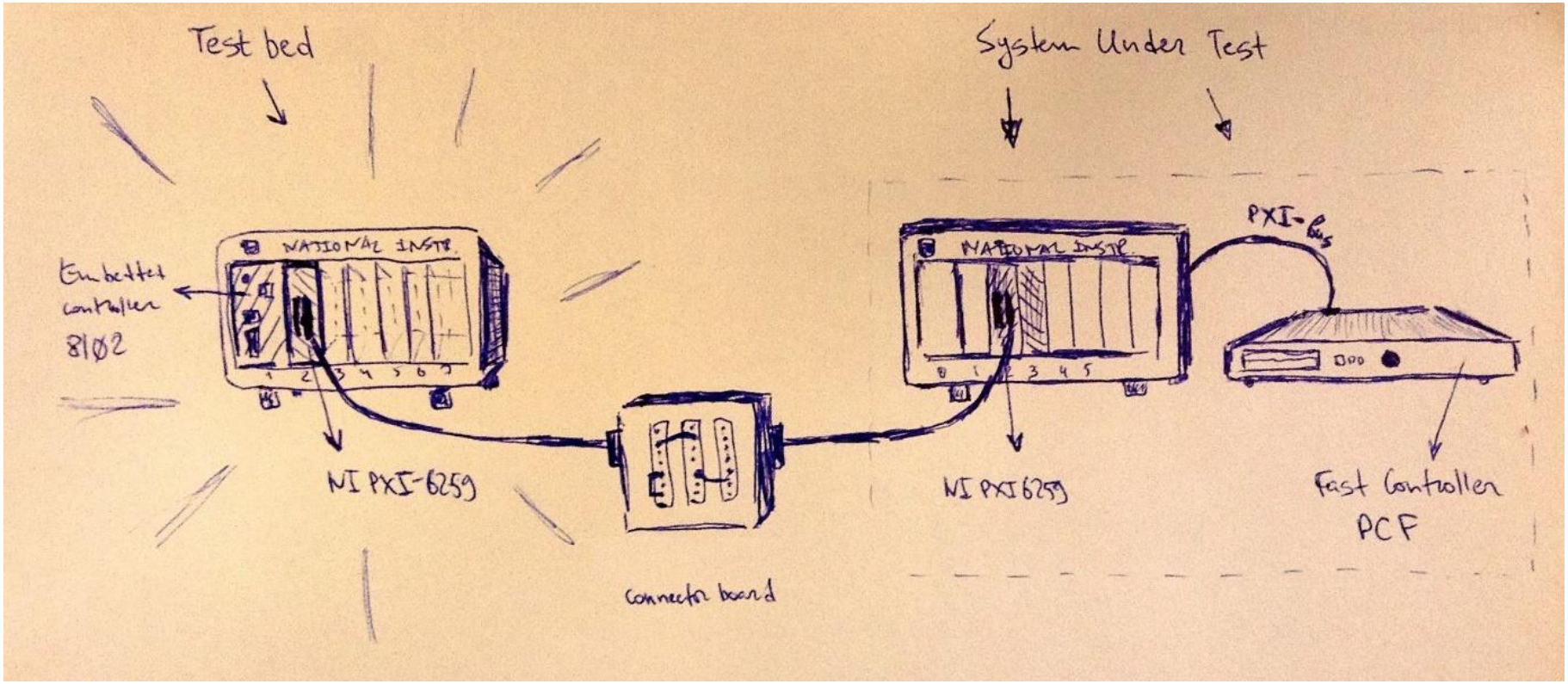
Intro

- Control system updates (>3 times/year)
- DAQ hardware tests:
  - manual (+ precise; - slow, infrequent)
  - automatic (+ fast, repetitive, liberating human resources)

HW architecture

- TestBed chassis is attached to System Under Test



- TestBed is running SL 6.3 and CODAC 4.1

SW architecture

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- The software part consists of 3 tiers:
  - Software that provides the desired functionality of a DAQ board:
    - C executables
    - EPICS device support (NDS driver + IOC)
    - *LabVIEW interface*
  - Python bindings in the form of a class
  - Automatic test cases written by the test-plan engineer

DAQ functionality

- The NI-PXI6259 functionality supported in TestBed:
  - Device reset
  - Digital input/output (static) on a desired line
  - DIO diagnostics: port mask and lines state
  - Configuration of the DIO port mask
  - Analog input/output (static) on a desired channel
  - Analog input (waveform) on a trigger
  - Analog output (waveform – sine/saw/square/file) on a trigger

SW architecture

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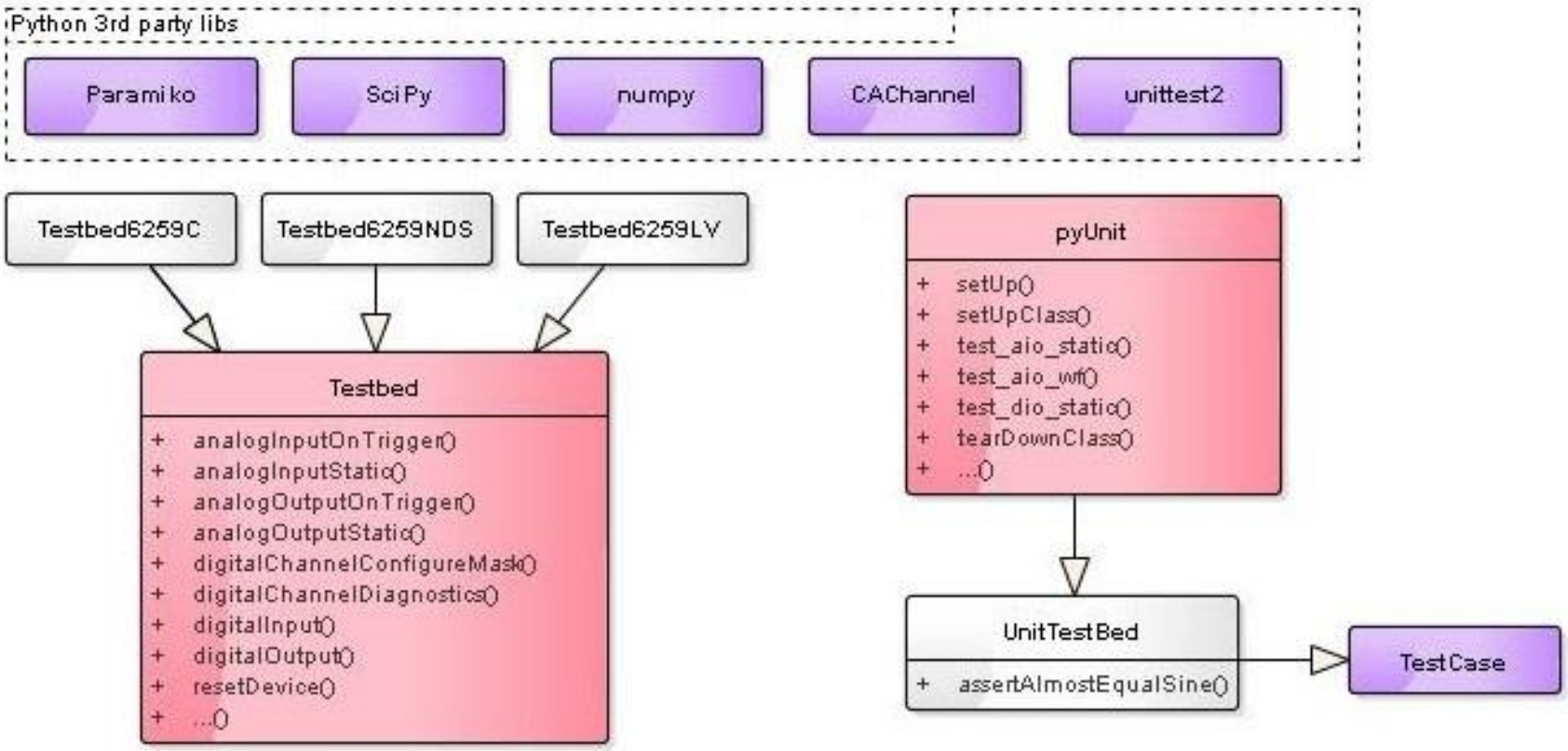
- Python class diagram:



Implementations

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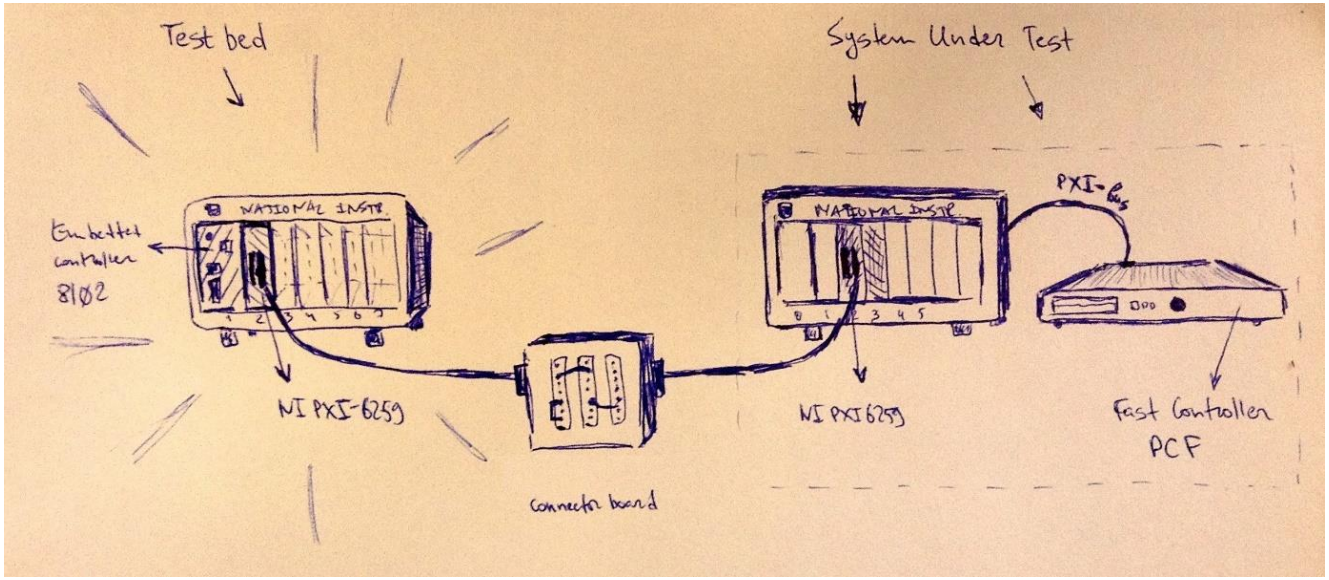
- C executables
  - Uses NI PXI-6259 Linux Device Driver (Cosylab)
- EPICS device support
  - Asyn based
  - NDS based
- *LabVIEW*
  - *NI-DAQmx driver supports the full functionality*
  - *start an IOC in LabVIEW (using CA Lab by BESSY)*

Test scenarios

- Generate on TB, acquire on SUT, check
- Generate on SUT, acquire on TB, check
- Generate on SUT, acquire on SUT



```
8  class TestNI6259(UnitTestBed):
9      # create SUT and Testbed
10     TB = testbed()
11     SUT = sut()
12
13     @classmethod
14     def setUpClass(self):
15         # setup SUT
16         self.SUT.server = "10.5.3.93"
17         self.SUT.username = "bled"
18         # setup TESTBED
19         self.TB.server = "10.5.3.175"
20         self.TB.username = "codac-dev"
21
22     def setUp(self):
23         self.TB.resetDevice()
24         self.SUT.resetDevice()
25
26     '''TESTING aio (static)'''
27     def test_aio_static(self):
35
36     '''TESTING dio (static)'''
37     def test_dio_static(self):
45
46     '''TESTING aio (waveform)'''
47     def test_aio_wf(self):
67
68     @classmethod
69     def tearDownClass(self):
70         self.TB.resetDevice()
71         self.SUT.resetDevice()
72         del self.TB
73         del self.SUT
```

test_aio_static

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```
26      '''TESTING aio (static)'''
27      def test_aio_static(self):
28          # generate constant voltage on the TB, ao1
29          Vreq = random.uniform(-10,10)
30          self.TB.analogOutputStatic(1,Vreq)
31          # acquire voltage on the SUT, ai0
32          Vact = self.SUT.analogInputStatic(0)
33          # compare the results
34          self.assertAlmostEqual(Vact,Vreq,1)
35
```

test_dio_static

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```
36      '''TESTING dio (static)'''
37      def test_dio_static(self):
38          # set do0 on the TB to a random state
39          STreq = random.randint(0,1)
40          self.TB.digitalOutput(0,STreq)
41          # get di32 on the SUT
42          STact = self.SUT.digitalInput(33)
43          # compare the results
44          self.assertEqual(STreq,STact)
45
```

test_aio_wf

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```
46      '''TESTING aio (waveform)'''
47      def test_aio_wf(self):
48          sample_rate = 500
49          nsamples = 1024
50          ampl = 2
51          offs = 1
52          phase = 1
53          # delta = [offset, ampl, freq, phase] mV
54          delta = [0.05, 0.05, 0.05, 0.05]
55          # create a waveform
56          wf_out = self.TB.generateWaveform(sample_rate, nsamples, "sine", ampl, offs, phase)
57          # on a rising edge of pfi1 line generate wf on ao1
58          self.TB.analogOutputOnTriggerWF(1, sample_rate, "pfi1")
59          # on a rising edge of pfi1 line acquire wf on ai0
60          self.SUT.analogInputOnTrigger(0, sample_rate, nsamples, "pfi1")
61          # trigger pfi1
62          self.TB.digitalOutput(0,1)
63          # get waveform from SUT
64          data = self.SUT.getAcquiredWaveform()
65          # compare the results
66          self.assertAlmostEqualSine(sample_rate, nsamples, ampl, offs, phase, wf_out, data, delta)
67
```

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PXI
RIGOL
DS1052D

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THANK YOU!

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