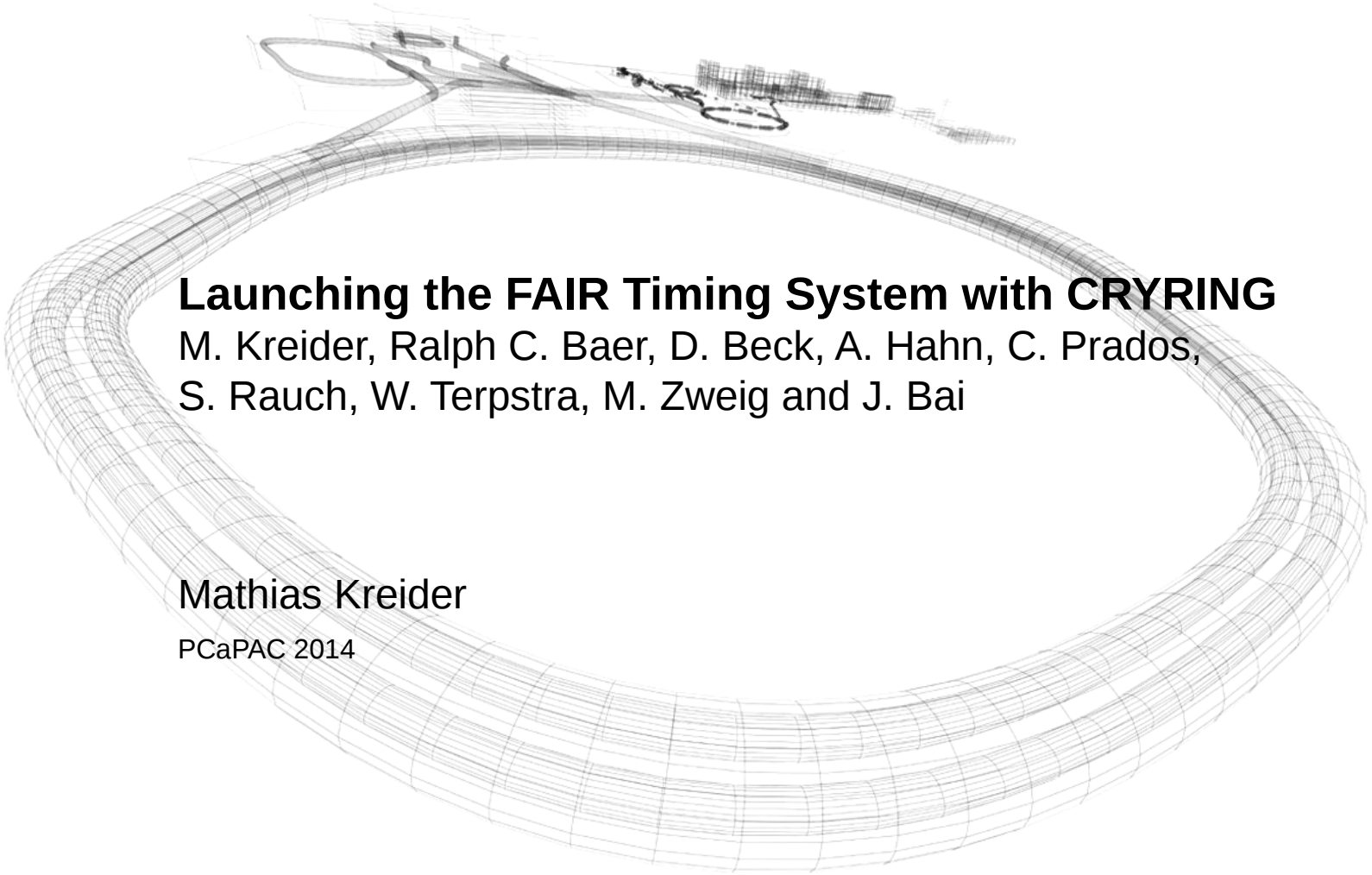


Launching the FAIR Timing System with CRYRING

M. Kreider, Ralph C. Baer, D. Beck, A. Hahn, C. Prados,
S. Rauch, W. Terpstra, M. Zweig and J. Bai

Mathias Kreider

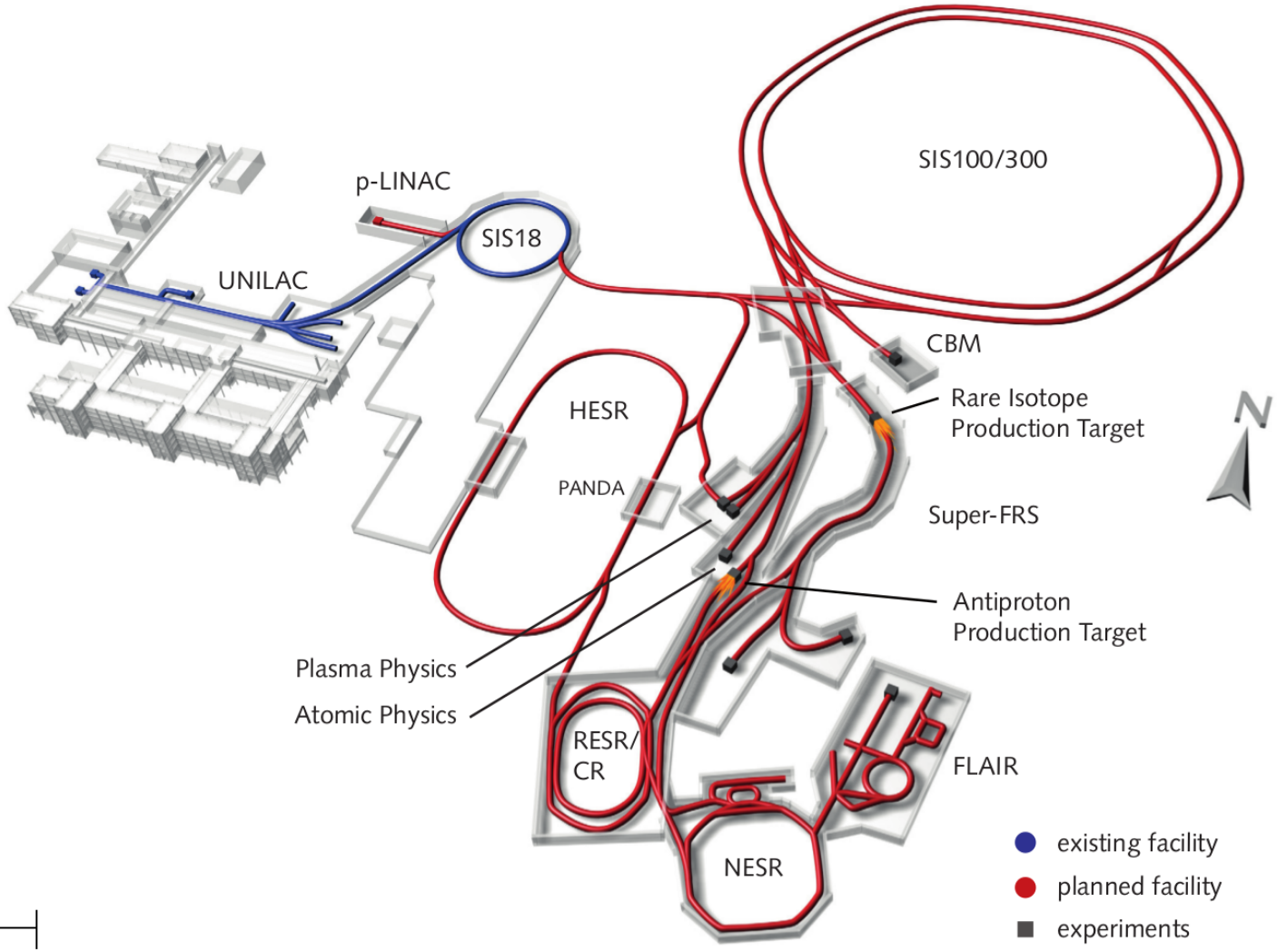
PCaPAC 2014

Overview

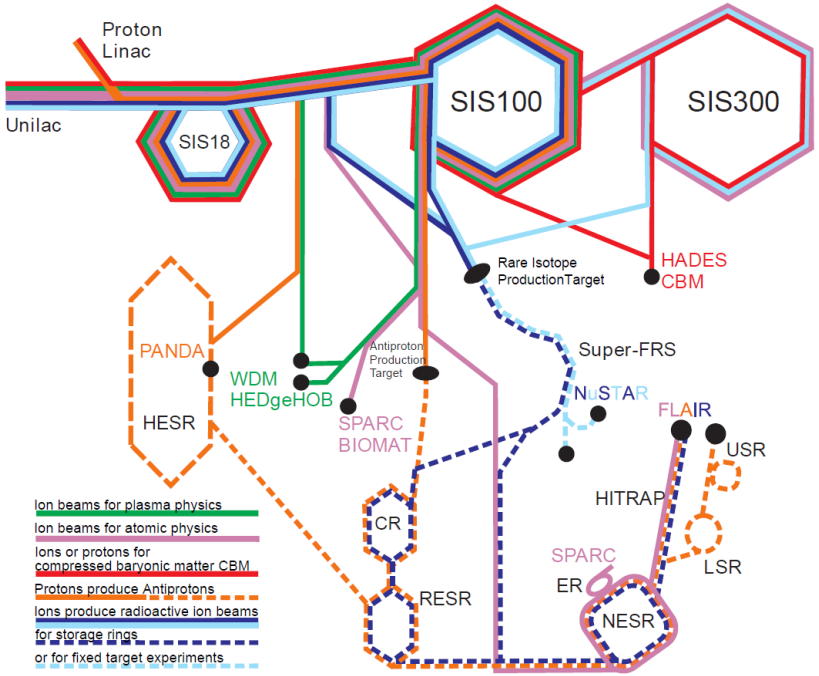
- Introduction
- FAIR Requirements
- Master
- Timing Network
- Timing Receivers
- Ongoing Tests
- Conclusions and Future Work
- Questions

Introduction

Future FAIR Facility



Challenge



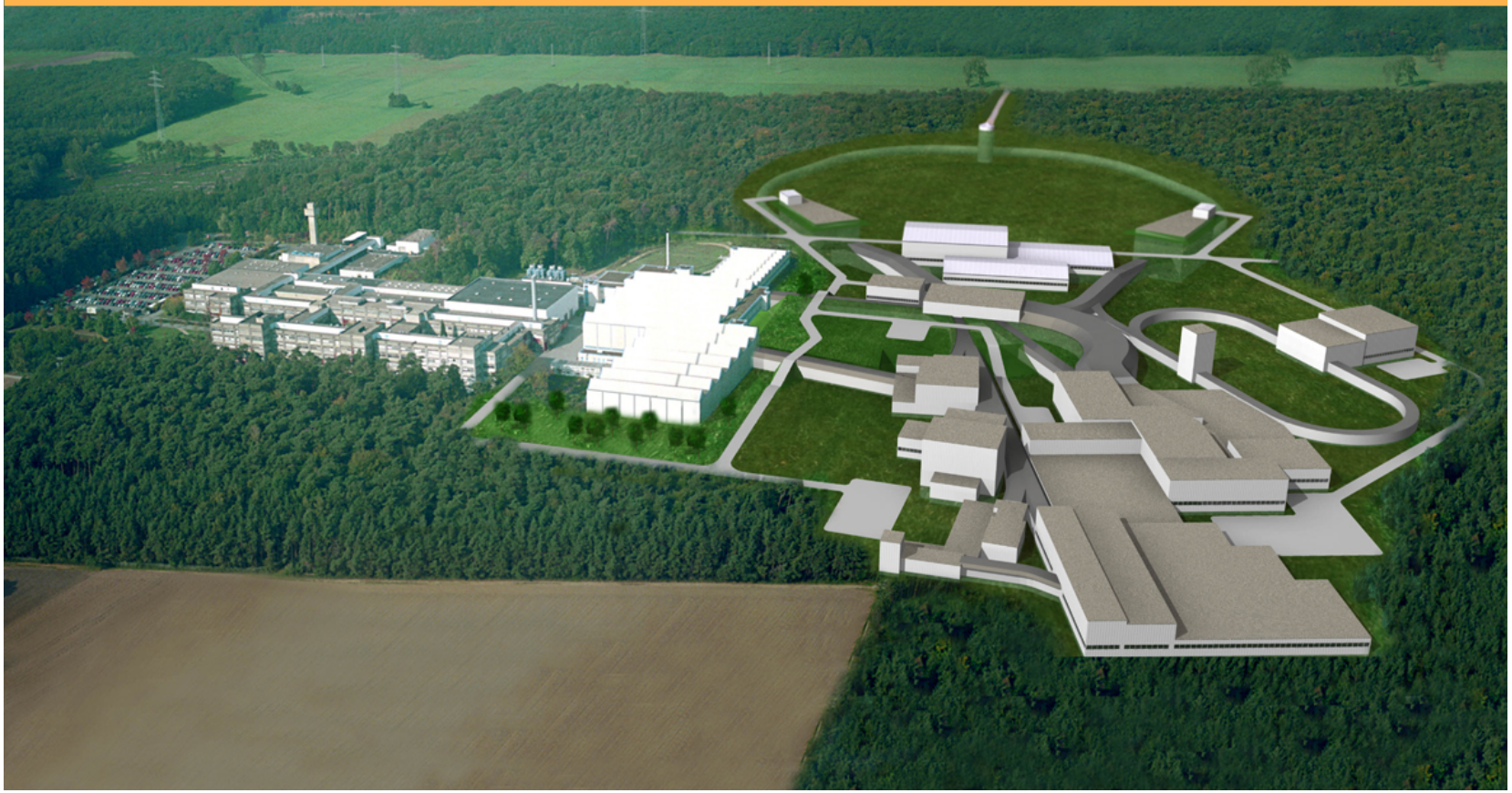
- Many different scenarios
  - … in parallel
  - … exactly on time
  - … and flexible

What makes a good control system?

FAIR Requirements

Conditions to meet on site

GSI - FAIR Facility



Requirements for Control System

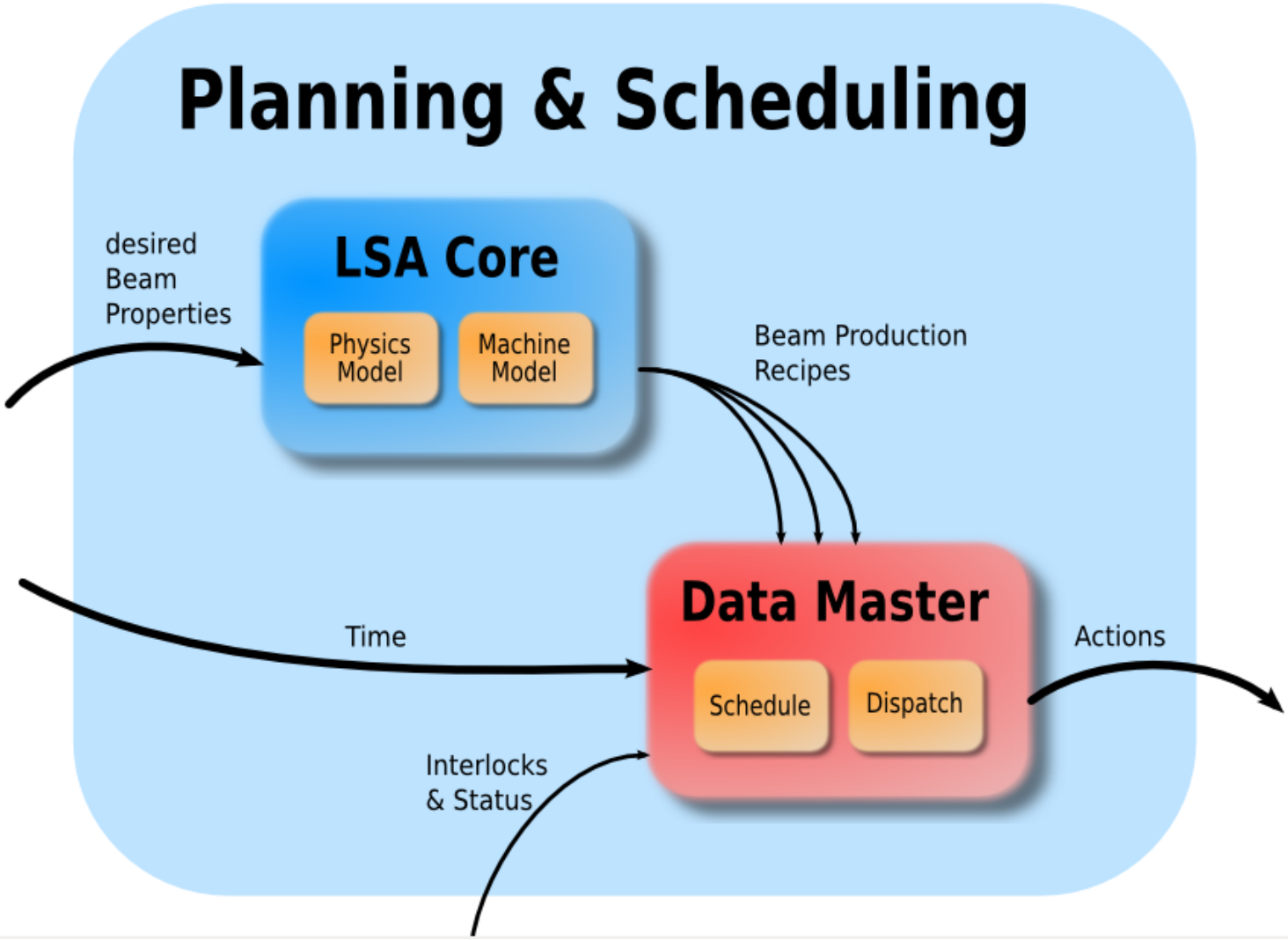
- Distance: up to 10 km
- Endpoints: 2000-3000
- Bandwidth: GbE
- Switch layers: 5+

- Accuracy: < 1 ns

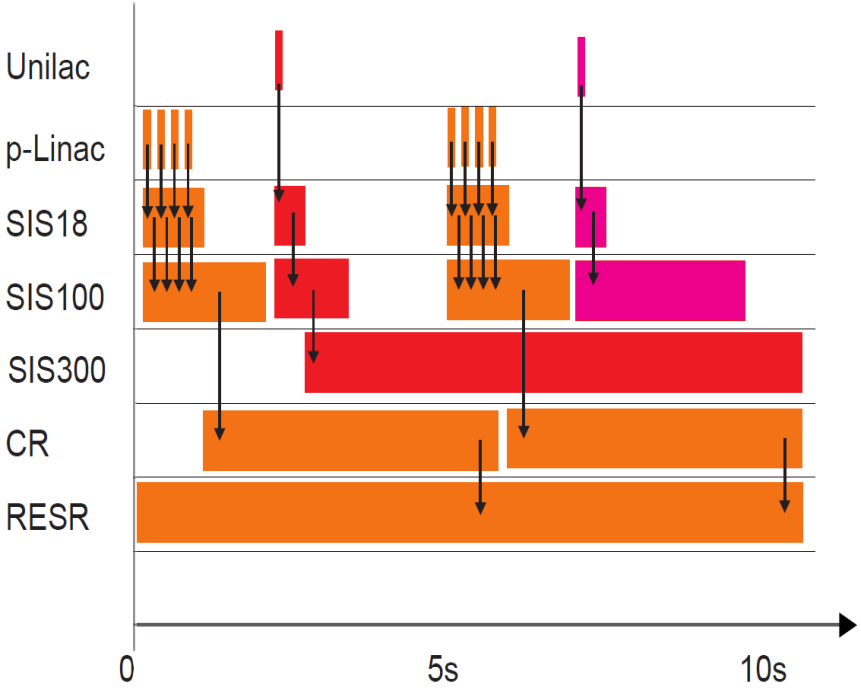
- Determinism: controls, networking and endpoints
- Reliability: less than 10^{-13} instructions lost
- Hard RT: no time for retransmission

Data Master

LSA and Data Master



Beam Production Recipes



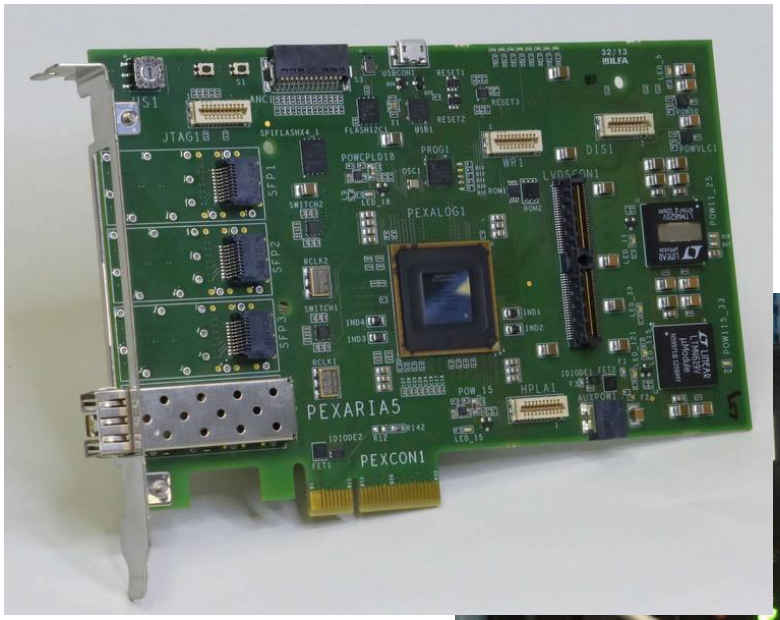
- Vast number of possibilities
- Dependencies
- Recurring patterns

→ transform to monotone sequence of actions

Transport Protocol

- **EtherBone**
  - Here: UDP based
  - Fast network wrapping of WB SoC bus
  - As close to hardware as possible
  - In our case: broadcast
- **Forward Error Correction**
  - Reed-Solomon
  - Fountain codes

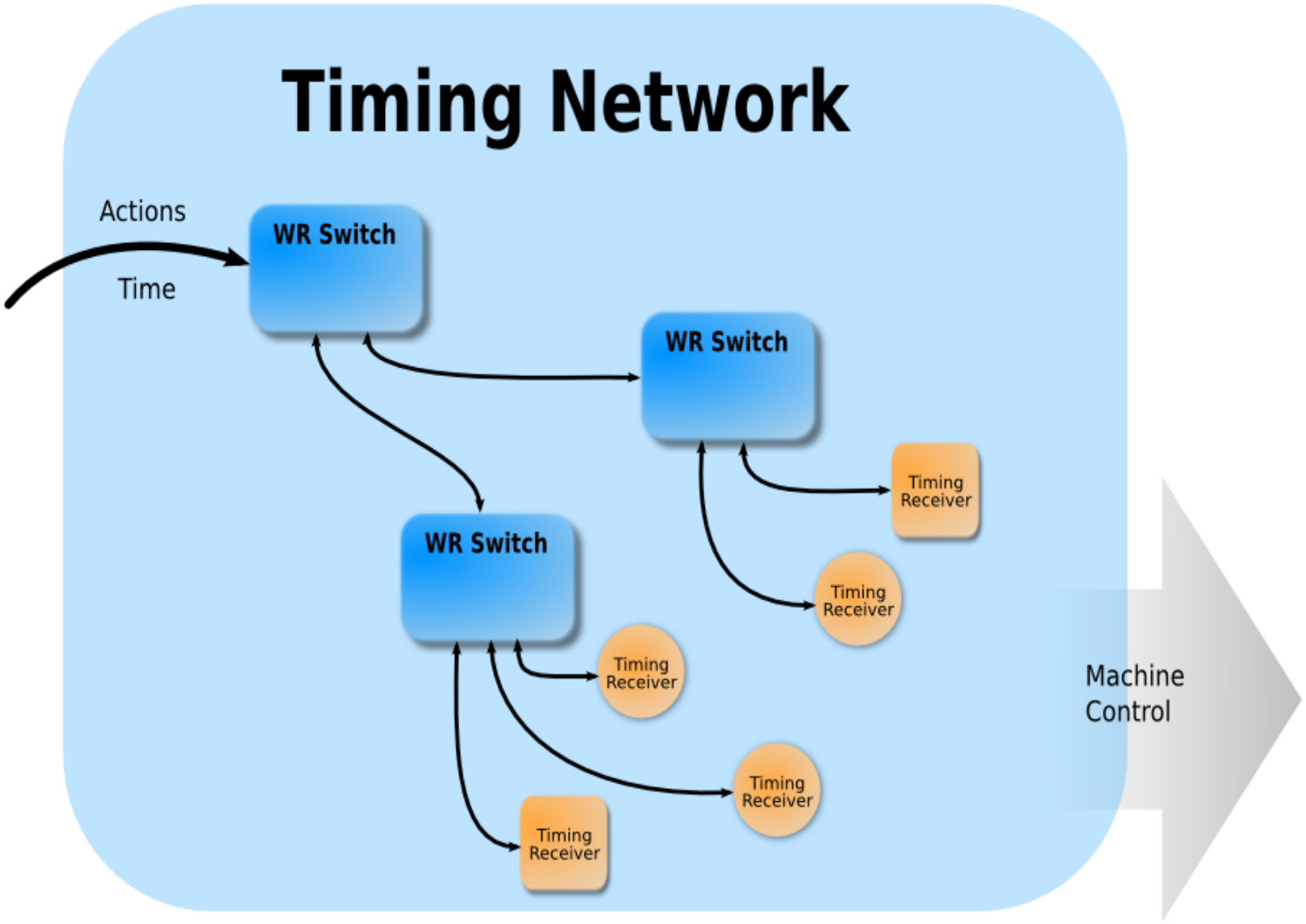
Data Master Prototype



Data Master - Industrial PC with PCIe
FPGA board and Timing Interface

Timing Network

Switches and Endpoints



Time & Clock Distribution

- Absolute Time
  - Where do we get a stable time source ?
  - How to make switches deterministic?
  - How to compensate for link delays ?
- Clocks
  - How to adjust frequency to master clock ?
  - How to measure & correct phase offset?

WhiteRabbit Protocol

- Absolute Time
  - GPS master to compensate long term drift
  - Fast Path & QoE in Hardware
  - PTP protocol
- Clocks
  - SyncE
  - Hardware phase alignment on fiber GbE

White Rabbit Switch

FPGA based 18 Port
White Rabbit Switch

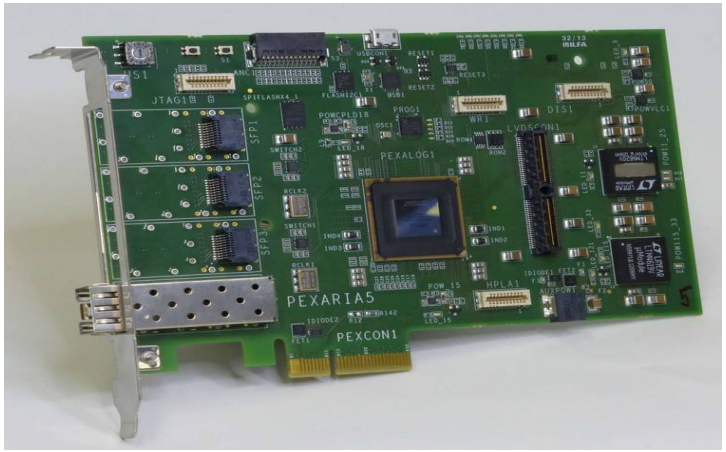
Timing Receivers

Endpoints - Event-Condition-Action Model

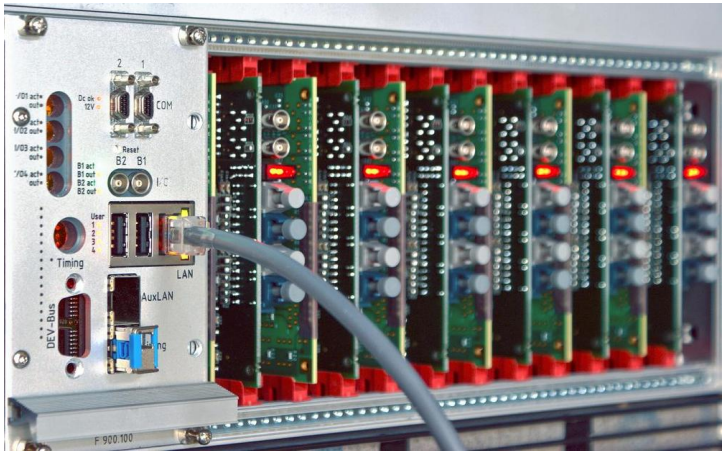
- Impossible to send all instructions deterministically over network!
- **ECA Unit** in Endpoints:
  - Pre-programmed:
    event (received ID),
    condition (mask/time),
    action (bus / IO)
  - Receive ID and execution time
  - Local hardware carries out action on time

FAIR Timing Receivers – Form Factors

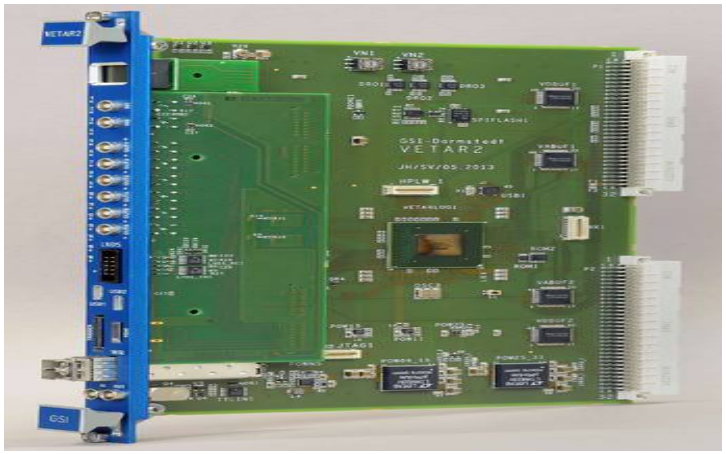
Standalone - Exploder



PCIe – Pexarria



SCU Bus - SCU



VME - Vetar

Ongoing Tests

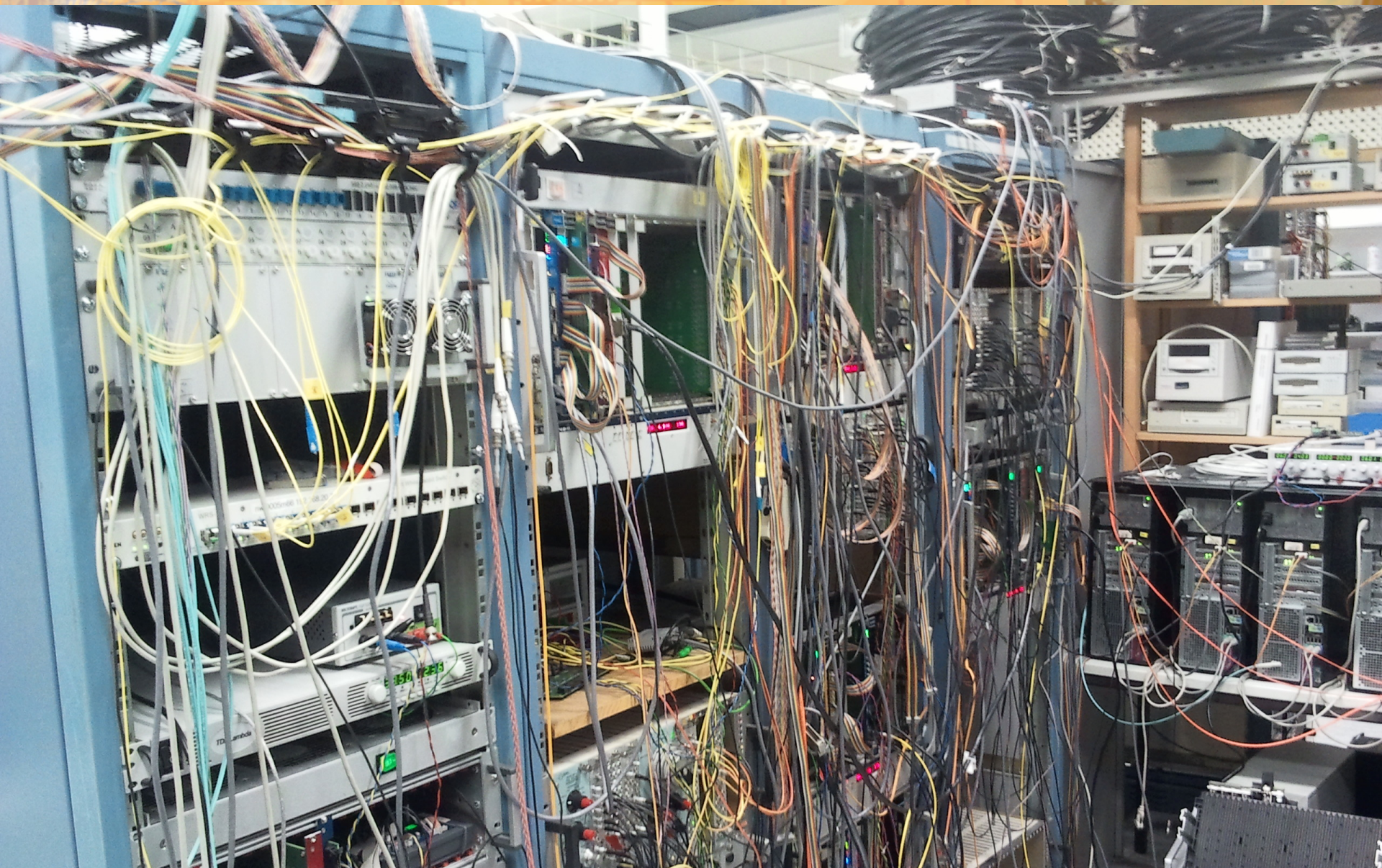
Current Testing

- Timestamped Data Acquisition for Experiments
- Front End Controller for Beam Instrumentation
- Function Generator for Power Supplies

→ We got invaluable feedback so far!

GMT and DAQ for Experiments

N. Kurz, J. Frühauf et al., EE, GSI: Our Favorite Users So Far!



Conclusions & Future Work

Conclusions and future work

- Second Data Master prototype built
- SCU integrated
- Timing Receivers for PCIe & VME developed and integrated
- Timing System ready for installation and integration with CRYRING equipment

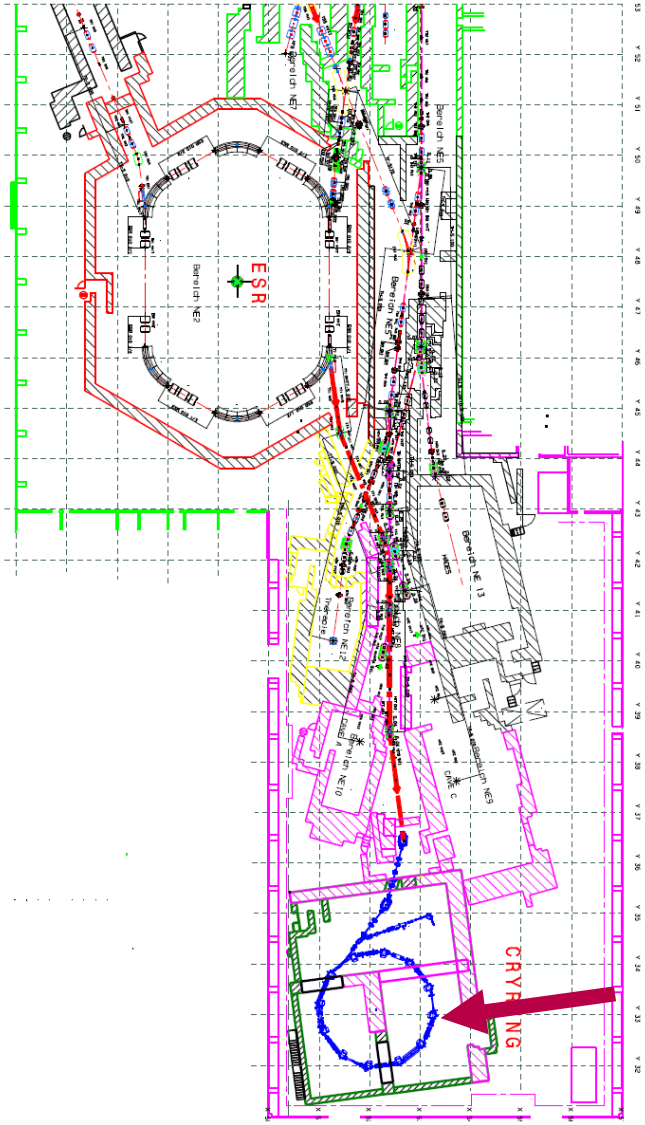
- Waiting for CRYRING infrastructure (power, racks, network and cable trays)

Facility for Antiproton and Ion Research

Photo 2014-05-25: Jan Schäfer for FAIR

CRYRING @ GSI

- CRYRING moved from Stockholm to GSI
- „a test ground for the FAIR control system“



Time for Questions