BUCKET SELECTION SYSTEM OF THE KEKB RINGS

E. Kikutani, A. Akiyama, T. Katoh, M. Suetake and M. Tobiyama
KEK, 1-1 Oho, Tsukuba-shi, Ibaraki-ken, 305, Japan

Abstract

KEKB is an asymmetric electron-positron collider, now under construction at KEK Japan. It consists of two storage rings and an injector. In order to feed the beam from the injector into arbitrarily selected rf-buckets of the rings, we are constructing a bucket selection system. It is made up from a bunch-current monitor, a delay timing controller in the injector and a message transfer system that transports the bunch-current information to the injector. The information is offered also to accelerator operators, the loging system and so forth. The bunch-current measurement is done every 20 ms and the information is transferred to the injector at this rate.

1 INTRODUCTION

KEKB[1] is an asymmetric electron-positron collider now under construction at KEK Japan. This accelerator facility consists of a 3.5 GeV positron ring, an 8 GeV electron ring and a linear-accelerator complex which can feed both electron and positron beams. In order to accomplish the target luminosity, $1 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the number of bunches stored in each ring is approximately 5000, which is almost the number of the rf-buckets in the rings, 5120. The minimum bunch spacing is, therefore, only 2 ns, corresponding the RF-wavelength.

For smooth and well-controlled operation of these accelerators, it is necesarry to prepare a timing control system[2]. The bucket selection system, which we explain in present paper, is a sub-system of the timing system. High precision wide-band system is required considering the short bunch spacing.

2 DESIGN OF THE BUCKET SELECTION SYSTEM

2.1 Why do we need a bucket selection system?

While data are taken by the physics detector, the beam-currents in both rings will be decreased due to several reasons. We must refill the beam when the current goes down to some specific value. At that time, we will not abandon the remaining beams but will top off the beam to save the filling time. Even though the same amount of electrons/positrons are injected into each of the RF bucket, the currents in the buckets will get smaller in diffrent rates from bucket to bucket. Then the required top-off currents are differnct among the buckets. Since the full current of one bucket is several times of the one pulse of the injector, we can regurate the current of in a bucket by controlling the number of injection pulses.

In order to realize such a control, we must prepare a system of measuring the bunch currents and controlling the bucket to which the beam is injected next time. The system is required to work in 50 Hz, which is the repetition rate of the injector linac.

2.2 Constituents of the system

In order to carry out the jobs explained above, we must prepare three parts, an injection-bucket selector, a bunch-current monitor and a message transfer mechanism which connects the former two parts. The bucket selector is very simple. A digital delay module in a VME package is prepared and we can easily select the bucket by setting the delay value to this module. The other two parts, the bunch-current monitor and the message transfer system is not simple and explanation of these parts is the main aim of this paper.

3 BUNCH-CURRENT MONITOR

The bunch-current monitor is a system consisting of the front-end circuit and the memory system which storing the bunch current data.

3.1 Front-end Circuit

Circuit of directly catching the bunch current is rather simple as shown in Fig. 1. This circuit inputs the signal from a button electrode and outputs a pulese whose height is proportional to the bunch current. Roughly speaking the circuit consists of a low-Q band-pass filter (two combiners/splitters and three cables) and a down-converter. We use the 2 GHz-components of the beam signal to catch the bunch current. Then each component should have sufficient bandwidth capable of this frequency.

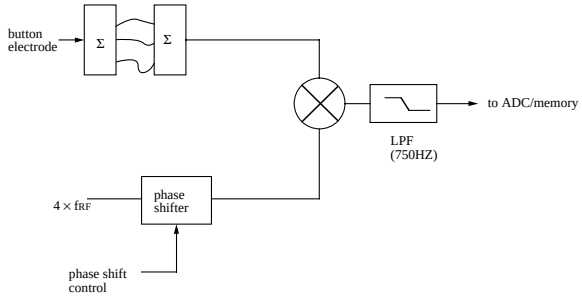

Figure 1: Front-end circuit of the bunch-current measuring system. The two combiners/splitters and three cables make a band-pass filter. The diffrencees in the lengths of the shortest cable and the other two cables are the wavelength of 2GHz and twice of it.

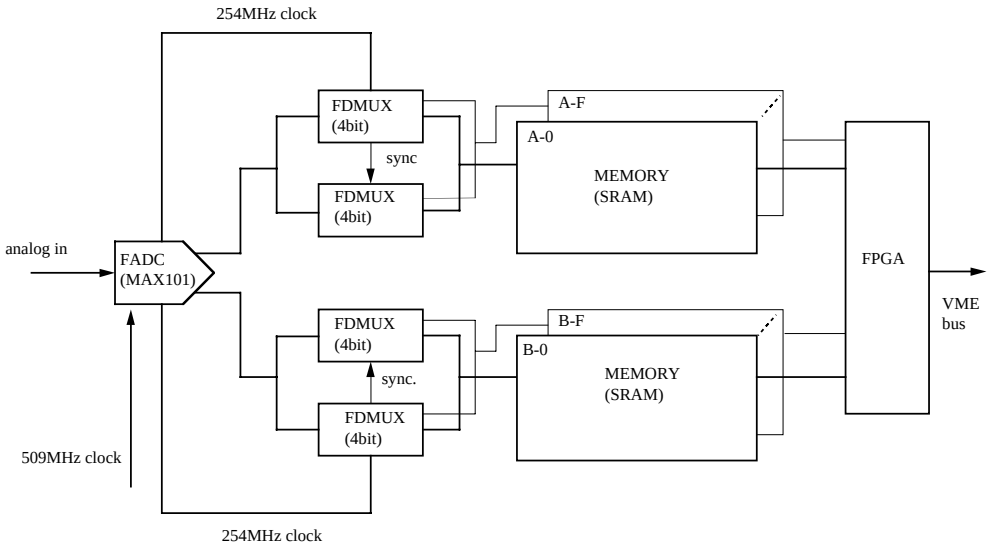

Figure 2: Block-didagram of the memory board. The signal which holds the bunch-current information is degitized with the ADC in rate of 509MSamples/s. The ADC outputs the digitized data from two output ports each of them has the 254MHz rate. These signals are de-multiplexed by the custom LSIs. One chip of the de-multiplexer can treat 4-bit data. The de-multiplxed data are stored in 16 identical memory banks.

3.2 The Memory Board

In order to store the turn-by-turn bunch-current information, we use the memory board, which is a by-product of the signal processing board for the KEKB bunch feedback systems. Since a closed describtion is given in another paper[3], we breifly explain the function of the memory board.

The board consists of a flash A-to-D converter (ADC), fast de-multiplexers (FDMUX) and banks of memory. A simplified blockdiagram is shown in Fig. 2. The ADC generate 8-bit digital data corresponding to the pulse-height of output from the front-end circuit. Since the bunch frequency is 509 MHz, the repetition rate of the conversion clock is also this frequency. The ADC outputs two 254 MHz digital signals. Each of the output is de-mulitiplexed to 16 signals with FDMUX. FDMUX is specailly fabricated for the bunch feedback sysmtes employed in the KEKB machines. The data is stored in the memory chips whose capacity is 20Mbytes in total. The board has a VME interface and the content of the memory is easily read out through the VME bus.

The bunch-current measurement is done by a series of the A-to-D conversions which is initiated by the 50 Hz trigger. This trigger is synchronizing with the injection beam from the linac. One series of the A-to-D conversion is 5120×128 of the A-D conversions. Strictly speaking, this bunch-current monitor gives us relative values of the bunch-current. The absolute values are obtained by normalizing the data with DCCT data.

3.3 Installation of the bunch current monitor

Since the detection frequency of the front-end circuit is rather high (2 GHz), it is not good idea to connect the pickup electrode and the front-end circuit with a long cable. We install the front-end circuit as well as the memory board in a local control-room near the beam line. The memory board is controlled through a VME computer, which is also installed near the beam line.

4 TRANSFER OF THE BUNCH-CURRENT INFORMATION

4.1 Transfer to the Linac Control Area

As we described above, the bunch-current monitor is installed in the local control-room. On the other hand, the delay module to control the linac pulse-timing is installed near the gun of the linac. We must transfer the bunch-current information from the local control-room to the gun control area. To ensure well synchoronized data-transfer, we do not use a general communication network of the control system but use a dedicated communication system. This system is based on the Shared Memory System, developed by Advanet Inc. Japan.

The Shared Memory System provides a method of fast communication among VME computers, which are distributed around a laboratory. The architecture is as follows. One prepares the ”VME memory boards”, the number of which is the same as that of the computers that he/she wants to connect. Each memory board is installed in a subrack of its respective computer. The memory board is equiped with memory chips and transmitter/receiver to exchange data among them through opticalcables. If one computer in one subrack writes data on the memory board, the copy of the content of the memory will be made in the other memory boards on line. Then the other computer can reads the data from their memory board as if they are sharing the common memory. The maximum length of the cable is 1km, then it

is possible to connect computers in several different buildings.

Basic specification of the system shown in below:

packaging	double-height VME
connection	optical fiber cables
max. distance	1000m
bit rete	250 Mbit/s
max. # of station	255
memory capacity	8kbytes-24Mbytes

Table 1: The main items of the specification of the shared memory system.

4.2 Transfer to the KEKB Main Control Room

The bunch current information is used by not only the bucket selection system but also used by accelerator operators and others as one of various kinds of information of the accelerator operation. To provide the bunch-current information to this genral purpose, we prepared another memory board, which is installed in a subrack located in the Central Control Room of KEKB.

4.3 Location of the computers

As easily understood from the above explanation, we use three memory boards as well as three corresponding computers, in total. Figure 3 schematically explains this communication system. The distance between the bunch current monitor and the Main Control Room is about 300m and that from the Control Room to the Linac is about 900m.

5 SOFTWARE IN THE THREE COMPUTERS

The control system of KEKB is constructed under the EPICS environment[4]. Under this system, all the devices accessed are controlled through various kinds of VME boards. The operating system running in the VME computer is VxWorks. Then, it is reasonable to use this operating system for all the three computers concerning the bunch-current information.

In the computer controlling the bunch-current monitor (refered as computer A), a process is periodically initiated by a hardware interrupt which is synchrozied with the linac injection. The process reads the content of the memory board and makes the average of 64 or 128 turns for each bucket. The averaged data are written into the Shared Memory Borad. In this computer, the EPICS database does not exists.

In the computer of the linac timing control, a process is running for determining which bucket should be filled by the next pulse consulting the data transferred from the computer A. Another important function is this process is set the appropriate delay setting on the digital delay module corresponding to the selected bucket. This process should, as the process in the computer A, be synchronized to the injection. Then it is initiated by the hardware interrupt.

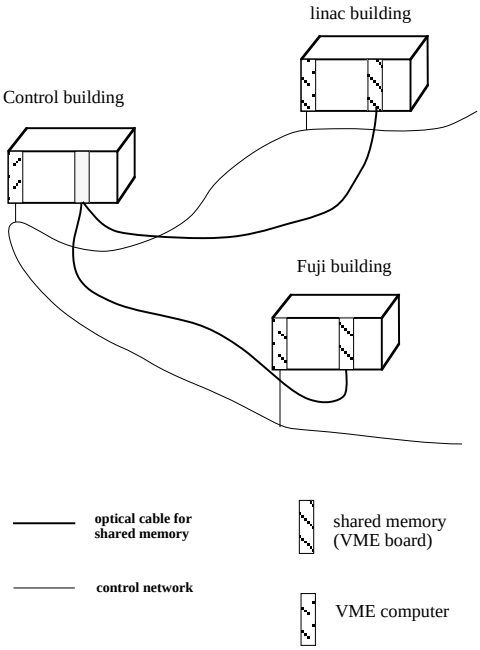

Figure 3: Distribution of the bunch-current information with the shared memory system. Besides the standard control network, the three computers are connected with the dedicated comunication system through the optical fiber cables.

In the computer installed in the Main Control room, the EPICS database of the bunch current is defined and standard EPICS processes will run. The user can freely get the bunch current information by accessing this database through the EPICS access method.

6 SUMMARY

A bunch current monitor system, a linac timing system and a message tranfer system make up a bucket selection system of KEKB. Since the real-time transfer of the bunch-current information is essential, we use the Shared Memory System for the transfer of the data. The the system provies the bunch-current information for accelerator operation or other general purposes through the standard EPICS access method.

7 REFERENCES

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