NEW TECHNOLOGIES IN THE DESIGN OF RF CONTROLS FOR ACCELERATORS

K. Fong, TRIUMF, Vancouver, Canada.

Abstract

RF cavity designs within the accelerator community have increased many fold in the last 20 years. Operating frequency now spans from a few megahertz to gigahertz, and quality factor varies from 1 to 10^{10}. The requirements for stability and reliability have also become more stringent. During this period, technological revolutions in computers, telecommunication and networking have resulted in the production and wide spread availability of fast digital electronics components. These enable RF low-level control systems to rise to the challenges presented by the demands of new accelerators. By adapting more complex control algorithms in hybrid or fully digital feedback controls, a RF low-level control system with uniform parameterization, which was once impossible to implement in a fully analogue system, can now be achieved.

INTRODUCTION

A low-level RF control system (LLRF) is required to operate under different operating modes such as conditioning, power-up sequencing and normal operation. Even under normal operation, the control system must provide a stable RF voltage under various beam currents and duty cycles. This is typically achieved using feedback control, sometimes augmented by feed-forward control. A control system must also be able to detect faults within the RF system, protect equipment and personnel, and determine the best recovery procedure from these faults.

The demands of modern accelerators are imposing challenging requirements on the stability of the RF field voltage. A phase error of 0.01^{o} translates to a phase noise of -75 dBc, while an amplitude error of 0.01% is equivalent to an amplitude noise of -80 dBc. In order for a control system to be able to deliver a field voltage that satisfies the stringent requirement of the beam dynamics, extra care must be taken to analyse the noise characteristics of the components within the control system.

Superconducting RF cavities, meanwhile, have been achieving unloaded Q's of the order of 10^{10}. Even when operating under overcoupling conditions the loaded Q's are still of the order of 10^{7}. At this high operating Q, any slight detuning of the cavity will cause a large deviation in the output phase as well as a large increase in RF power, in order to keep the cavity at the operating voltage. The detuning can arise from the fluctuation in helium pressure and microphonics. It requires advancements in tuner design and control in order to keep the RF cavity in resonance.

DIGITAL CONTROL

The development of digital hardware like Digital Signal Processors (DSPs), Field-Programmable Gate Arrays (FPGAs) and software tools such as (VHSIC hardware description language (VHDL) allows real time digital control systems to be implemented with relatively ease. As more and more processing power can be packed into these devices, complex control algorithms and higher bandwidth can be applied to achieve higher performance than that which was available using analogue system. Other advantages of digital control over analogue control include:

1. No variation of system parameters due to component value fluctuations, but system parameters can be easily changed on line.
2. No parasitic, secondary effect, or cross-talk induced degradation.

Since most devices already have diagnostics algorithms built-in, it is easy to implement diagnosis routines for device and board-level self-diagnosis. A digital system introduces quantization error due to its finite word length. Together with jitter in the sampling clock the errors are manifested as amplitude and phase noise. A digital system inevitably requires pre- and post-filtering.

To implement a digital control system, there are two categories of methods: transform and state-space methods. The transform method, also known as the auto-regressive method, follows the classical approach of applying the z-transform to analyse the open loop response of the system, analogous to the Laplace transform used in analogue controls. This method is quite satisfactory when applied to systems that have a single input and a single output, e.g. in cavity field control. The state-space method is better suited to more complex system where multiple inputs and outputs are involved.

SIGNAL PROCESSING AND FEEDBACK CONTROL

Similar theoretical approach to signal processing is also applied to the field of digital control. There are also differences between the two fields. For digital signal processing, the signal bandwidth is often in megahertz, while for feedback control system the required control bandwidth seldom exceeds 100 kHz. However, while sampling rates of slightly more than twice the signal frequency is sufficient for signal processing, the sampling rate must be many times the control bandwidth for digital control. In addition, transport lags can be very detrimental to the stability of a feedback control system, while for signal processing delays of tens of milliseconds can be tolerated and remain unnoticed. An example of this is a

FFT calculation, which is very useful in signal processing, but because of the delay involved in collecting enough samples, is never used inside a feedback control loop.

CAVITY FIELD CONTROL

In a LLRF control system, there are three major components in cavity field control: Demodulation, processing and modulation The RF from a cavity must first be demodulated and converted into digital form. A digital processor examines the digitized signal and generates the necessary correction. The correction signal is then modulated back into RF for amplification and injection into the cavity. Different accelerators have different operating frequencies, amplitude noise and the phase noise requirements. Cyclotrons typically are fixed frequency devices, while other types of accelerator may be variable frequency devices. Some may have relaxed phase noise requirements compared to other machines. These different characteristics will determine the type of modulation and demodulation scheme to be used for field control.

Demodulation Schemes

To control the RF field within a cavity, the RF voltage must be sampled at a rate many times the control bandwidth. When the RF voltage is sampled directly (Fig. 1a), or after it has been down converted into an intermediate frequency (Fig. 1b), it can then be

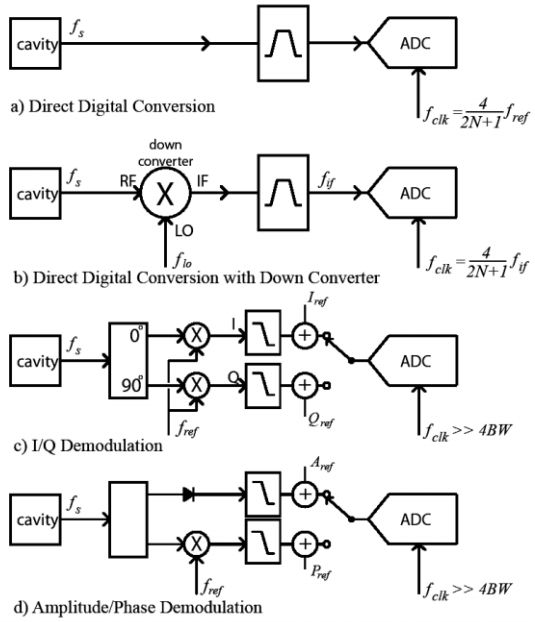

Figure 1. Difference Demodulation Schemes

considered as direct digital conversion. In both of these cases, separation into I and Q channels is performed after digitization to impose uniformity between the 2 channels. If the RF voltage is down converted to baseband (Fig. 1c and 1d), then it is a hybrid system. Once the signal is extracted to baseband, further division can be made by separating the signal to its two orthogonal representations (I/Q and Amplitude/Phase). Quantization errors that were significant problems for earlier 8-bit and 10-bit ADCs have become insignificant for the later generations of 14-bit and 16-bit ADCs.

At first glance, it may appear that direct digital conversion (Figure 1a) requires the least amount of hardware, but an external phase-locked loop (PLL) is required to generate the $f_{clk}=\frac{4}{2N+1}f_{ref}$ sampling clock. It also demands the highest performance from the ADC and is most intolerant to jitter originating from the sampling clock σ_{clk} and the ADC's internal sample-and-hold window σ_{adc}. The signal-to-noise ratio SNR_{jitter} due to jitter is [3]

$$SNR_{clk}(dB)=20\log\left[\frac{1}{2\pi f_s\sqrt{{\sigma_{clk}}^2+{\sigma_{adc}}^2}}\right] \quad (1)$$

Since SNR_{jitter} is inversely proportional to f_s, direct digital conversion with its high f_s demands a sampling clock and ADC with very little jitter. One of the state-of-the-art ADCs is the Linear Technology LT2209. This is a 16-bit, 160 Msps ADC with a quoted pre-released aperture jitter of 70 fs rms. The following table gives the SNR of this ADC at different input frequencies.

Table 1. Phase noise characteristics of LT2209 ADC

f_s	SNR (dBFS)	Phase noise (° rms)
5 MHz	77.1	0.0080
30 MHz	77	0.0081
70 MHz	76.9	0.0082
140 MHz	76.6	0.0085
250 MHz	75	0.01

A sampling clock typically has higher jitter. A typical low phase noise commercial clock IC is the Analog Device AD9510 series clock generator. These clock circuits exhibit a jitter of 250 fs rms, which is 3.6 times that of LT2209. This means that at a 250 MHz signal frequency, the total phase noise is 0.023°. In order to achieve better results, the RF signal is often down-converted into a more manageable intermediate frequency before digitization, as shown in Figure 1b. The choice of down-converter must be considered to include the phase noise due to the mixer as well as the local oscillator. Technical difficulties also arise from the generation of the sampling clock. The sampling clock as well as the local oscillator must be phase-locked to the reference frequency. Two PLLs with low-noise phase detectors and VCXO/DROs are needed to produce sufficiently low phase noise to satisfy the aperture jitter requirement. PLLs are also very sensitive to external interference and must be installed with their own electrical shields. A

good clock can be compromised by routing it through a FPGA where internal crosstalk is prevalent. Designers of FPGAs only envisage them to be used in a synchronous environment, and often maximize I/Os at the expense of ground pins, resulting in ground bounce. There should be few or no logic gates in the sampling clock path, as a single ECL gate has approximately 4ps rms timing jitter. When the sampling rate is not phase-locked to the signal frequency, I/Q demodulation schemes cannot generate phase information without a large amount of calculation. For this reason the hybrid Amplitude/Phase demodulation scheme is the only viable solution in self-excited mode operation.

In the hybrid system (Figure 1c and 1d), the signal is first demodulated into baseband in either I/Q or Amplitude/Phase components. The error signals can be extracted either before the ADC by analogue subtraction (as shown in Figure 1c and 1d) or by digital subtraction after conversion. In the first case, the full scale of the ADC can be devoted to the error signals, raising the dynamic range and the resolution of the demodulation sub-system. Since the signals are dc after conversion, the only requirement for the sampling clock is that the sampling frequency must be set to exceed four times the control bandwidth. SNR_{jitter} degradation due to jitter for baseband sampling is negligible and can be ignored. These signals are subjected to degradation due to dc offset, external interference and cross talk. Systematic errors such as dc offset and channel imbalance can be corrected after digitization.

Modulation Schemes

A major development in the area of modulators is in the area of direct digital synthesis (DDS). A comparison of traditional methods vs. DDS is shown in Figure 2. In an Amplitude-Phase modulator, the reference signal is modulated in series by an amplitude modulator and an electronic phase shifter. In an I/Q modulator, the reference signal is split into an In-phase component and a Quadrature-phase component. These components are amplitude modulated in parallel and then recombined. There is no analogue modulator inside a DDS, the output sinusoidal waveform is calculated digitally and updated with an external reference clock. With DDS, reference-clock jitter can be seen as phase noise on the fundamental signal. Phase truncation may introduce an error into the output level, depending on the code word chosen. For a frequency ratio that can be exactly expressed by a truncated binary-coded word, there is no truncation error. For ratios requiring more bits than are available, the resulting phase noise truncation error results as spurs in a spectral plot. Their magnitudes and distribution depend on the code word chosen. As good linearity at high speed is difficult to achieve, the spurs are dominated by the nonlinearity of the DAC output. Other digital logic within the DDS and the DAC quantization error will also contribute to the output phase noise. Table 2 compares the advantages and disadvantages of the three different modulation schemes as applicable to low level RF control.

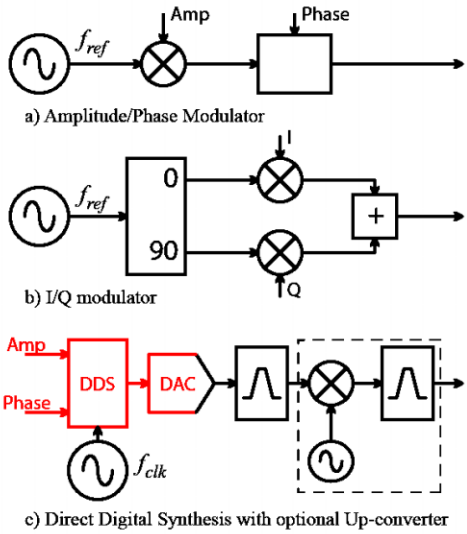

Figure 2. Different Modulation Schemes

Table 2. Comparison of Different Modulator Scheme

Amp/Phase Modulator	I/Q modulator	Direct Digital Synthesis
Large phase control range	Small phase control range	Large phase control range
Non-linear phase response	Linear phase response	Linear phase response
Large cross-talk	Small cross-talk	No cross talk
Subject to thermal drift	Subject to thermal drift	Not subject to thermal drift
Suitable for self-excited mode	Suitable for self-excited mode	Not suitable for self-excited mode
Uses external frequency reference	Uses external frequency reference	Requires external frequency that is multiples of reference frequency
Low phase noise	Low phase noise	High phase noise
Low data latency	Low data latency	High data latency
Low parts count	High parts count	High parts count

One particular point that should be emphasized is that DDS is unsuitable for self-excited mode operation because synthesizing the RF directly breaks any RF feedback path necessary for a self-sustaining oscillation. Many high power CW machines can benefit from self-

excited mode operation, whether during the testing phase, the commissioning phase or even during the operational phase. For these machines DDS cannot be used as the modulator.

There is a little known unstable mode when using an I/Q modulator together with an amplifier with high AM-PM conversion gain. Normally this unstable mode can be damped out by the action of the tuner. But in the TRIUMF booster[8] the actuation speed of the tuner is too slow to achieve any effective damping, and the movement of the tuner actually sets off limit cycle oscillation by this mode. The only method to eliminate this limit cycle oscillation is to use an Amplitude/Phase modulator instead of an I/Q modulator.

ADAPTIVE CONTROL

Most RF cavity field control system operates in regions where there is little change in process dynamics, so there is little need for a complex feedback control algorithm. Fixed-gain PID controllers will satisfy the requirements of most accelerators. In operations where there are various beam intensities, the addition of gain scheduling is all that is needed to handle heavy beam loading (Figure 3a). The beam current can be used as the scheduling variable to determine the PID parameters. Additionally, these sets of PID parameters can be determined at the

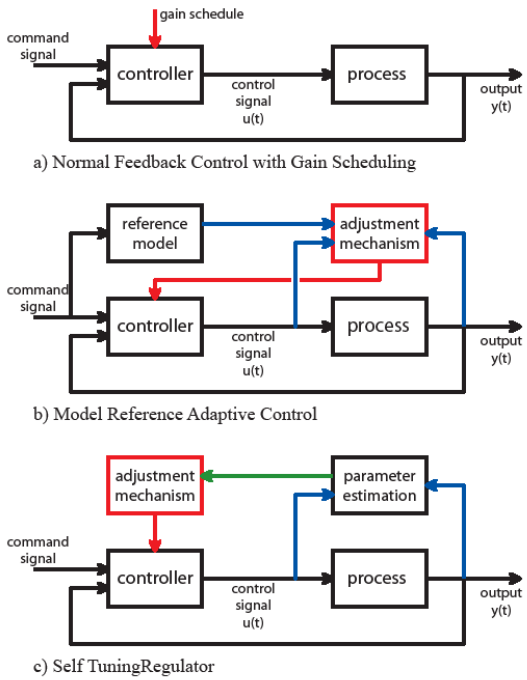

Figure 3. Block diagrams of Normal Controller and 2 types of Adaptive Controllers

time when a new control loop is commissioned, or when the operating conditions are altered. New digital controllers have a built-in Auto-tuning function which allows the PID parameters to be determined automatically using the Ziegler-Nichols method[4]. The Ziegler-Nichols method involves measurements of the step response of the system in order to estimate the best parameters. Earlier algorithm requires the system to be put into an open loop. Newer systems use the relay method that does the measurement without disabling the

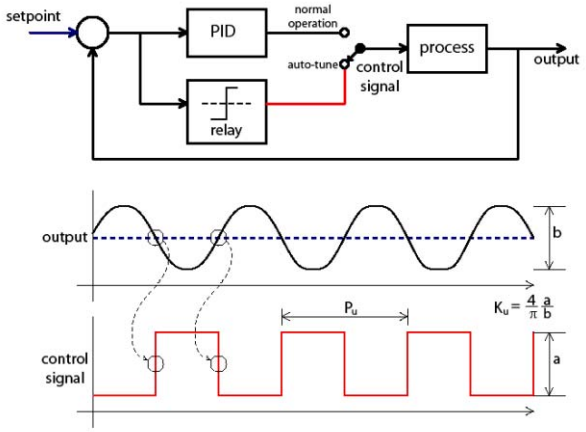

Figure 4. Auto-Tuning PID controller using Relay Method

feedback (figure 4).

Due to system limitations, such as actuator limits or safety limits, the logic of the PID controller needs to be able to prevent windup of the integrator. When the actuator desaturates it may then take a long time for the system to recover. Anti-windup schemes can be easily added using digital controller. As soon as saturation is detected at the output, the integration stops and prevents the integrator from winding up. Further improvement in pulsed-operation is easily achieved with feed-forward compensation.

Cavity resonance (tuner) control systems have quite different requirements. They require much smaller control bandwidth, but often involve nonlinear processes and are subject to higher noise contamination. The tuning signal is often derived indirectly from the phases of RF pickups in various locations, where the signals are subjected to thermal drift. The tuning signal often contains a strong signature due to both internal and external mechanical resonances. Mechanical actuators have different responses in different loading conditions. Some actuators such as piezoelectric actuators are nonlinear in their response. During a cold start, the cavity will usually have a different resonant frequency than the operating frequency. It is the tuner control system's job to determine the difference and adjust the cavity by moving the tuner to the desired frequency as quickly as possible. When the acquisition phase is completed, the tracking phase command signals are issued in response to disturbances. Conventional design practices that allow a system to remain stable in all these instances will suffer by having sub-optimal performance. The use of a variable structure control system will be able to deliver both performance and reliability. Variable structure control systems (VSCS) are characterized by a suite of feedback control laws and a decision rule. The decision rule, called the switching function, selects a particular

feedback control in accordance with the system behaviour.

Mixed in with VSCS is adaptive control strategy. Adaptive control can help to deliver both stability and optimal performance in the different structures within a VSCS. An adaptive controller monitors the process dynamics in real time continuously and modifies the control algorithm coefficients to compensate for variations in the environment and in the system itself. In the acquisition phase, Model Reference Adaptive System (MRAS in Figure 3-b) can be used. In a MRAS, the control parameters are continually changed such that the output obeys a pre-defined model. In the tracking phase, Stochastic Self-tuning Regulator (STR, in Figure 3-c) is used. The purpose of the stochastic STR is to minimize the variance of the output. With a time-invariant linear system described by the Autoregressive moving with an average auxiliary input (ARMAX) model [5],

$$A(z^{-1})y(t) = z^{-d}B(z^{-1})u(t) + C(z^{-1})e(t) \qquad (2)$$

where *u(t)* and *y(t)* are the input and output of the system, *e(t)* is a zero mean white noise process of variance σ^2, z^{-1} is the unit time delay, and *d* is the delay of the system. The general controller for regulation is

$$B\left(z^{-1}\right)F\left(z^{-1}\right)u(t) + G\left(z^{-1}\right)y(t) = 0 \qquad (3)$$

This gives the closed loop equation

$$\begin{bmatrix} A & -z^{-d}B \\ G & BF \end{bmatrix}\begin{bmatrix} y(t) \\ u(t) \end{bmatrix} = \begin{bmatrix} C \\ 0 \end{bmatrix} e(t) \qquad (4)$$

The performance criterion for such a system is

$$J = \lim_{N\to\infty} \frac{1}{N}\sum_{k=1}^{N} E\left[y(t)^2 + \rho u(t)^2\right]. \qquad (5)$$

where ρ is a constant parameter used to weigh the relative importance of the output and input variance. An STR tries to minimize the 'loss function' *J* by recursively predicting

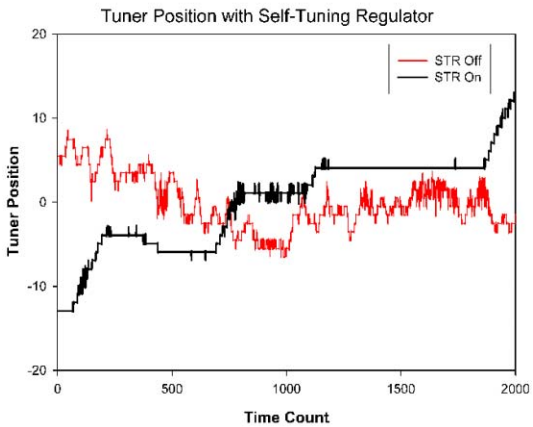

Figure 5. Performance of ISAC 2 Tuner with Self-Tuning Regulator

and correcting *y(t)* using the Riccati equation. *F* and *G* obtained from the recursive iterations are applied to calculate the next control signal *u(t)*. Such an approach, when expressed in state space, is similar to that used to calculate the steady-state Kalman filter.[6]

Both VSCS and STR have been deployed in the resonance control of the TRIUMF ISAC 2 LLRF control system. In this system the tuning signal is obtained by comparing the RF phase at the input and output of the cavity. The controller is a PI controller, which drives a servo linear motor. Through a cam and lever system the motor pushes the bottom plate of the quarter-wave cavity, and changes the geometry and the resonant frequency. Figure 5 shows that after STR is applied, the variance of the tuner position is reduced.

Adaptive control is a very rich field. Here we have only described one implementation of STRs. In more complex cavity resonance control systems, adaptive controllers have even greater potential that are yet to be exploited by system designers.

SELF-DIAGNOSTICS

With the rapid rise in system performance and growth in system complexity, analysing the health of system components around the feedback loop becomes more demanding. As circuitry becomes more complex, it becomes more difficult not only to probe the inside of devices such as FPGAs and DSPs, but also to monitor device-to-device and board-to-board communications. To solve these growing problems, electronics component and board manufacturers formed the Joint Test Action Group (JTAG) to develop methods that can simplify and standardized in-circuit and on-line testing of components. The solution is to build test functions and test points into the ICs, and to ensure compatibility between all compliant devices. This is published in the IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture.

Boundary scan is the application of a scan path that occurs at the boundary (I/O) of ICs to provide controllability and observability access via scan operations. It requires a register to be added at every I/O pin on a device. This allows standardized software known as Boundary Scan Description Language (BSDL) to perform control-and-response tests on every pin and all logic within the device, as well as interconnecting devices. Most FPGAs and DSPs devices manufactured after 1990 have JTAG architecture incorporated in them. Some microcontrollers and memories also have JTAG ports.

The JTAG architecture not only allows device-level, board-level, interconnect, and system diagnostics, but it also enables on-line modification of firmware for FPGA's, CPLD's and Flash Prom's for DSP's. With the addition of VME-to-JTAG interface, all these functions can even be done remotely.

SUPERVISORY CONTROL

Supervisory control is the control of the low level RF system outside the feedback control loops. Its functions include exception handling and recovery, power-up

sequencing, high level diagnostics, data acquisition and communication with a remote host. With the emergence of pre-emptive multitasking operating systems, the supervisory tasks can be performed concurrently with multi-tasking and multi-threading programs. Multithreading brings numerous benefits, especially in data acquisition, instrument I/O and exception handling applications. The Exception handler can now reside in an interrupt-driven, time-critical thread, for a much faster response time. Synchronous calls to instruments can be performed using individual threads, and while these threads are waiting for responses from their instrument interface, other activities can run concurrently. On multiprocessor systems, multithreading takes advantage of the additional hardware and, through simultaneous execution of tasks, can result in greatly improved overall performance.

Creating multithreaded applications can be difficult even for very experienced programmers. Multithreading involves a new way of programming the parallel execution of tasks and how they interact with each other. As more threads are added to an application, the complexity of managing those threads jumps exponentially. Unexpected behaviours in multithreading can occur when multiple threads issues conflicting requests, when multiple threads request shared resources simultaneously, when priorities prevent threads from gaining appropriate execution time, or when threads sharing data space do not include mutual exclusion code to preserve data integrity. Testing a multithreaded application is more difficult than testing a single-threaded application because defects are often timing-related making them more difficult to reproduce. Regardless of these difficulties, multithreading presents many important advantages, when incorporated into supervisory control.

CONCLUSION

The rapid advances in LLRF controls are in part due to advances in digital, mixed-signal electronics and software tools. Faster digital electronics means that more complex algorithms can be applied to feedback loops, and enabling the incorporation of adaptive controller into LLRF control system should the need arise. The development of highly complex digital hardware requires accompanying software tools to enable a designer to program these devices efficiently. As a result of recent technological advancements in both hardware and software development, one is now able to build control systems that are capable of far greater speed and accuracy.

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