

A FET BASED MASS SEPARATOR KICKER FOR TRIUMF ISAC PROJECT

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Abstract

The ISAC facility at TRIUMF is an isotope separator coupled to an accelerator. Short-lived nuclear species are produced in a thick target that is bombarded with protons from the 500 MeV TRIUMF cyclotron. A beam of short-lived isotopes (<60 keV) is mass analysed and transported to either low energy experiments or into an accelerator. The voltage of a mass separator kicker is chosen to select the momentum of the ions and generates variable pulse widths with duration comparable to the half-life of the nuclei selected. The mass separator kicker system includes a pair of deflector plates. One plate is charged up to +10 kV by a FET based modulator, while the other plate is driven up to -10 kV by another modulator. Each modulator consists of two stacks of FETs operating in push pull with both variable output voltage and repetition rate from virtually DC to 10 Hz. The specifications for the mass separator kicker demand that a stack of FETs must be held in the on-state for between 20 ms and 10 s. The relatively long duration requires special consideration of component leakage currents and a novel drive technique. This paper describes the design of the kicker system and shows the results of measurements.

1 DESIGN CONCEPT

A total potential difference of up to 20 kV is required between two deflector plates. One plate is driven to +10 kV by a solid-state modulator. Another modulator drives the other plate to -10 kV. The design of these modulators is based on previous designs at TRIUMF [1,2,3,4]. However the design has been modified[9] for operation at very low repetition rates (almost DC to 10 Hz). The specified rise and fall times are 1 ms. The modulators have been designed to give a rise and fall time of 100 μ s (see Table 1). The rise and fall time could be significantly less than 100 μ s, however 100 μ s allows substantial current limiting to be employed, therefore resulting in a very conservative and reliable design.

The basic building block of the circuit consists of 1 kV APT1004[6] FET modules[1,2,3,4]. PSpice[7] was used to verify and optimise the circuit for this application. The drive signals to modules are transformer coupled using single turn pulse transformers. The 10 kV solid-state switches consist of two stacks of 14 FET modules, operating in "push-pull" mode; when one stack is on the other stack is off. One stack is referred to as the "pull-down" stack and the other is referred to as the "pull-up" stack. In the +10 kV (-10 kV) modulator, when the "pull down" stack is on the deflector voltage is pulled down to ground (-10 kV), and when the "pull-up" stack is on the

deflector plate is pulled up to +10 kV (ground).

Table 1: Measured values for TRIUMF Pulser Designs

Pulse voltage	Rise and Fall time	Repetition rate (continuous)	References
6 kV	30 ns	10 Hz to 20 kHz	[1,2]
10 kV	40 ns	10 Hz to 1 MHz	[3,4]
± 10 kV	100 μ s	<10 mHz to >10 Hz	Present paper

Analytical equations have been derived to calculate the variation in voltage per module as a function of the capacitance ratio $k=C_{\text{gnd}}/C_{\text{m}(n)}$ [2]. Where C_{gnd} is the parasitic capacitance to ground of one module and $C_{\text{m}(n)}$ is the total linearized drain to source capacitance of a 1 kV FET in module #n, including parallel grading capacitance.

$$\text{If } k \text{ is small then; } V_{m(n)} \cong V_{m(1)} \left(1 + \sum_{i=1}^{n-1} ik \right)$$

Each modulator is housed in a metal cabinet. The parasitic capacitance, measured between the pulsed output of a modulator and ground, with both stacks in the off-state, corresponds to a capacitance to ground for each module of 2.1 pF. Since the rise and fall times and maximum repetition rates are low, the grading capacitance per module (9.4 nF) was chosen so that k in the above equation is small (2×10^{-4}). Hence, from the above equation, transiently $V_{m(14)}$ is 2% greater than $V_{m(1)}$. The current for charging the 9.4 nF capacitance is limited by four resistors (each of 470 Ω) in series with both the FETs and fast-grading capacitors on each 1 kV module. This time-constant is approximately 17.6 μ s. In addition the DC grading resistors (3 x 820 k Ω) are 1% resistors. The measured off-state drain-source resistance of an APT1004 FET is > 10 G Ω , with 900 V drain-source and 0 V gate-source. Hence the DC voltage grading is good to 1%.

The low repetition rate results in very low power dissipation in the FET stacks and thus no heat sinks, or forced cooling are required. The current limiting resistors are low power, and are mounted on the PCB card of a module, rather than on the back plane of the stack. This permits a compact layout compared with previous designs. The very low repetition rates require a new design for the drive circuits; the gate-source voltage of the FETs cannot otherwise be held on (or off) reliably for periods of more than 0.5 s. In addition, the gate-source zener diodes, used to protect the gate of the APT1004 FETs, are chosen to be low leakage current devices.

The rate of decay of gate-source voltage cannot be measured directly without affecting the decay: hence a two-step process was used. Firstly the peak positive gate-source voltage was measured; the voltage probe was then removed. Secondly a 900 V, 32 mA supply was connected between drain and source; and the APT1004 driven on.

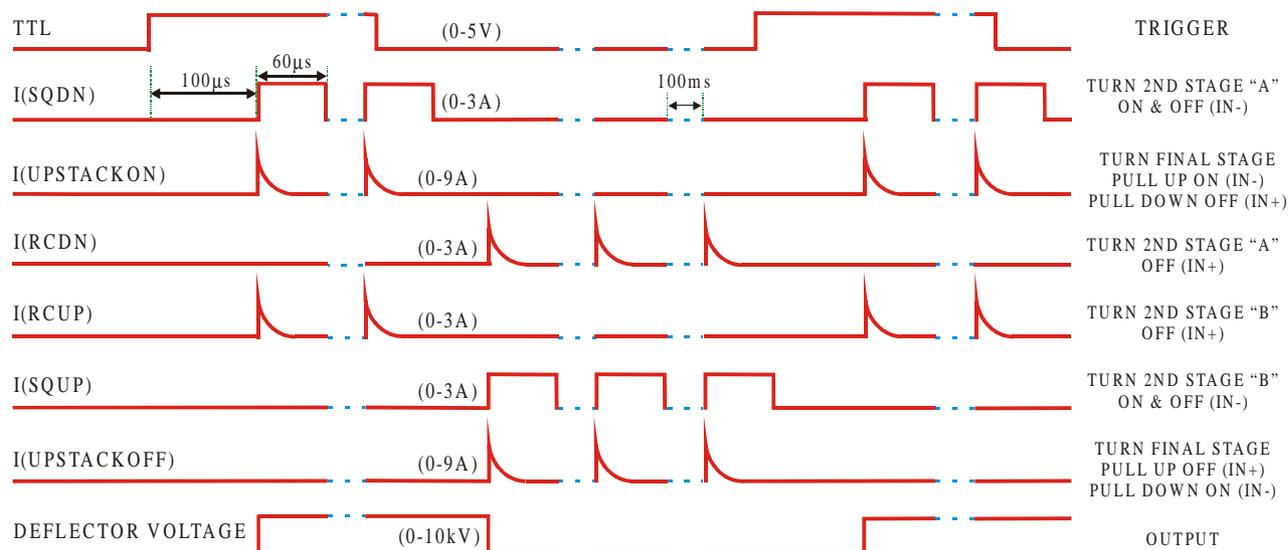


Figure 1. Typical pulse sequences for 1st, 2nd and final stages

The APT1004 starts turning-off (i.e. drain-source voltage increases) when the gate-source voltage decays to the threshold level (~ 4 V). An effective time-constant for the decay of gate-source voltage is calculated from these measurements.

A gate to source resistor of $200\text{ M}\Omega$ is included on each module to ensure that the gate-source voltage is 0 V , if there is a fault and no drive reaches the gate. The equivalent linearized gate-source capacitance of the APT1004 FET is approximately 2 nF . A discrete capacitance of 3 nF is also added to increase the effective gate-source capacitance to 5 nF . This increases the measured time constant of the decay of the gate-source voltage to approximately 1 s . However the effective time constant also depends on the gate-source voltage, drain to source current, and drain-source voltage. It is not feasible to add further gate-source capacitance to extend the effective time-constant of the gate-source voltage to 10 s ; this would require a total capacitance of approximately 50 nF . A gate-source capacitance of 50 nF would require a very substantial drive current to charge and discharge the gate to approximately $\pm 15\text{ V}$. Thus a novel drive technique was developed where a continuous train of pulses is used to keep the APT1004 in the desired state. The pulse train has a conservative period of 100 ms ; the pulse has a fast rise time and a slow decay. An exponential decay with an RC time-constant of $12\text{ }\mu\text{s}$ was chosen for these pulses, such that the voltage that is coupled onto the secondary of the pulse transformer is less than a diode voltage drop (0.7 V), and is not coupled through to the gate-source of the APT1004.

Two pulse systems were built and tested. One operates at voltages of up to $+10\text{ kV}$ and the other at voltages of up to -10 kV . We describe the $+10\text{ kV}$ system in the following. The beam kicker consists of three stages to convert a TTL master trigger pulse pattern to a 10 kV pulse pattern. The three stages are referred to as the *First Stage*, *Second Stage* and *Final Stage*. The dashed lines in

Fig. 1 indicate the 100 ms time period. The square current pulses $I(\text{SQDN})$ and $I(\text{SQUP})$ have a duration of $60\text{ }\mu\text{s}$.

To avoid a conflict between the timing of the continuous pulse train and that of the switching of states from the master trigger pulse there is a $100\text{ }\mu\text{s}$ delay between the master trigger pulse and the gate pulses; thus the $\pm 10\text{ kV}$ output is also delayed by $100\text{ }\mu\text{s}$ (Fig. 1).

1.1 First Stage

A master TTL signal with the desired output pulse pattern is fed to controls. The controls generate the required pulse train, which is fed to the first stage through a fibre optic link. The first stage consists of 4 drive circuits, per deflector plate, arranged functionally in two pairs of two. One of the drive circuits per pair provides a square current pulse from a 600 V source (e.g. $I(\text{SQUP})$, 3 A , and $60\text{ }\mu\text{s}$ duration). The other drive circuit of the pair provides a pulse (e.g. $I(\text{RCUP})$, 3 A peak) with a fast rise-time and RC decay of about $12\text{ }\mu\text{s}$. Fig. 1 shows one pair of first stage pulses to drive second stage “A”, and a second pair of first stage pulses to drive second stage “B”.

1.2 Second Stage

The second stage consists of two stacks (“A” and “B”) of 2 modules each. Each second stage stack has two independent single turn primary windings. One single turn primary is used to turn one stack on and $60\text{ }\mu\text{s}$ later off (e.g. $I(\text{SQDN})$), and the other single turn primary (e.g. $I(\text{RCUP})$) is used to keep the stack in the off state.

The second stage modules are the same as the final stage modules except for the following:

- Output resistor values are lower in the second stage ($33\text{ }\Omega$ total per module), compared with a total of $940\text{ }\Omega$ per module in the final stage, to allow for increased current (9 A) for the drive to the final stage;
- Grading capacitors values are lower in the second stage (2 nF per module total) compared with 9.4 nF total per module in the final stage.

A 650 V, 50 mA, capacitor charging power supply from F.u.G.[5] provides energy for the 600 V rails of both the +10 kV and -10 kV systems. Voltage and current set points limit the output of the F.u.G. to 600 V and 25 mA.

The F.u.G. provides the energy for the drive pulse train (I(RCDN) & I(RCUP) in Fig. 1) for recharging the gate-source of the second stage modules to -15V. The F.u.G. charges a 56 nF capacitor to 600 V though a resistance of 50 k Ω , i.e. with a time constant of 2.2 ms. This time-constant is substantially less than required for producing a drive train with a period of 100 ms. The 56 nF is discharged through 204 Ω (3 A peak). About 60 μ s (i.e. 5 discharge time-constants) later this FET is turned off to allow the 56 nF to recharge.

Both stacks of a final stage share two primary windings; the primaries of the pull-up stack and the pull-down stack are in series but pass through the transformers cores in opposite directions, so that one stack is turned on by the drive and the other stack is turned off by the same drive. The two primary windings carry current in opposite directions so that a single F.u.G. can be used for the modulators. These primary windings carry current pulses, generated by the second stage, (I(UPSTACKON) & I(UPSTACKOFF) in Fig. 1). The current pulses are for switching the final stage or keeping it in the desired on or off state. The energy for these pulses is provided by the F.u.G. power supply, which charges 4 parallel 56 nF capacitors to 600 V though a resistance of 5 k Ω , i.e. with a time constant of 1.1 ms. These capacitors are discharged through 66 Ω (9 A). The second stage, used to discharge the parallel capacitors, is on for 60 μ s (i.e. 4 discharge time-constants), and then turned off to allow the parallel capacitors to recharge. Thus the input drive for the second stage modules, which generate the final stage drive, is square pulses (I(SQDN)& I(SQUP) in Fig. 1).

1.3 Final Stage

There are a total of 28 final stage modules for each 10 kV system. The output of each Glassman[8] (10 kV, 500 μ A) power supply is connected to a 60 nF filter capacitor, via a 500 k Ω resistor. The 60 nF is required to store energy because of the limited output current of the Glassman power supply. The 500 k Ω resistor limits the average current from a 10 kV supply to 20 mA and therefore protects the final stage modules from excessive dissipation if a higher power 10 kV supply is used.

2 MEASUREMENTS

Figure 2 shows the output of both the +10 kV stack and -10 kV modulators. The output of each modulator is loaded by 670 pF (i.e. 9.4 nF per module for 14 series modules) capacitance of the off-state stack plus 365 pF capacitance of a 4 m coax cable used to connect to the deflector plates. The deflector plate capacitance is approximately 40 pF.

At frequencies higher than 10 Hz, the 10 kV power supplies cannot supply enough current to cause damage.

The 10 kV output voltage starts to droop at 10 Hz. At 20 Hz the output droops to 5 kV. In addition the 600 V power supply current limits to 25 mA at 15 Hz.

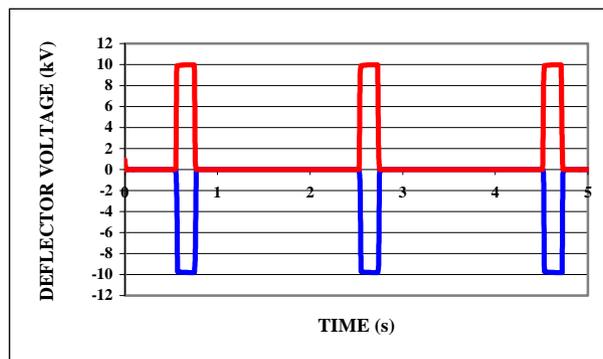


Figure 2: Measured 10kV pulses

3 CONCLUSIONS

The +10 kV and the -10 kV systems were operated together for a test. The TTL trigger signal was varied from <10 mHz to >10 Hz. The output \pm 10 kV pulse patterns duplicated the TTL pulse patterns with a 100 μ s delay. The systems work at very low repetition rates, essentially to DC operation. The kicker systems exceed the ISAC requirements as shown in table 2.

Table 2: FET pulse parameters

Parameter	Specification	Measured
Output voltage	9 kV	9.8 kV
Min pulse width	20 ms	150 μ s
Max pulse width	10 s	infinite
Rise/fall time	1 ms	100 μ s
Max. Rep rate	2 Hz	10 Hz

The system is designed for low frequencies and thus is protected from operating at higher frequencies, which could overheat components. The system was installed in the ISAC facility on June 6, 2000.

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