BROADBAND BUNCH BY BUNCH FEEDBACK FOR THE ESRF USING A SINGLE HIGH RESOLUTION AND FAST SAMPLING FPGA DSP

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Abstract

In order to increase the current in the ESRF storage ring we have developed a set of multi bunch feedback systems aimed at fighting longitudinal and transverse coupled bunch instabilities. The longitudinal feedback (LFB) has been the first system installed and tested. It was designed using the scheme developed at SLAC, ALS and INFN Frascati: bunch by bunch processing of a beam phase error signal and correction using a low Q kicker driven by a QPSK modulator. However, we took advantage for this development of the latest available technology for the signal processing electronics with high resolution, high sampling rate ADC and DAC, and FPGA DSP, as well as for the FPGA programming environment. It allowed us to substantially reduce the complexity of the project: the algorithm runs on a single processor, the kicker requires only 200W of RF power to control a 6GeV beam, and the implementation took only about one year. We will describe the main features of our LFB and present the results already achieved in the damping of instabilities driven by HOM of our RF cavity. We will also report on the status of the transverse feedback, which is built using the same FPGA system as the longitudinal one.

INTRODUCTION

The first motivation of this project was to allow the storage of 300mA with a uniform filling of the buckets of the ESRF ring, instead of the 200mA that we are presently able to store. The present limitation is due to the excitation of longitudinal coupled bunch instabilities by higher order modes (HOM) of our RF cavities. To overcome this problem, we decided to implement a longitudinal feedback.

We also started in parallel the implementation of a transverse feedback; the additional work to design and implement transverse feedback was moderate; it would allow us to test new machine tunings while studying new modes of operation (16 bunch filling with topping up for instance) or to cope with the 300mA current stored with the help of the longitudinal feedback. It would also be a very powerful diagnostic for transverse studies.

LONGITUDINAL FEEDBACK DESIGN

We chose the now classical approach of detecting every turn the variation of the phase of each bunch with respect to its equilibrium phase, to derive from this phase deviation an energy correction to apply to the beam, and to produce this correction using a longitudinal kicker. We paid a lot of attention to achieve the best possible resolution in the phase measurement in order to reduce the required kicker maximum strength.

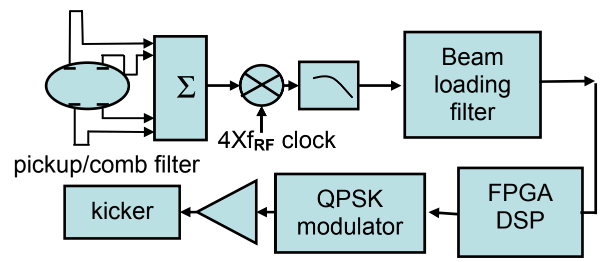

Figure 1: Layout of the ESRF longitudinal feedback.

Phase Detection

We detect the beam signal using a set of 4 capacitive pickups. We combine the pickups signals with cables of different lengths to obtain a comb filter selecting a bandwidth of 352MHz around 1.4GHz (four time our RF frequency of 352.2MHz). We use a RF mixer as a phase detector (see figure 1); the output of the mixer is amplified to match the input range of the 14bit ADC of the FPGA DSP board resulting in the resolution detailed in the table 1.

Table 1: Phase detection resolution

Phase detector sensitivity (RF mixer)	≈ 6mV /°
Noise (Z_0 =50Ω, BW =176 MHz, N=6dB)	12μV rms
Phase detector turn by turn resolution δϕ	2 10^{-3}°=4fs
usable range (14 bit ADC, LSB = δϕ)	+/- 32ps

In our storage ring, the ratio between the energy and time amplitude of a longitudinal oscillation is .4KeV/fs; so our time resolution of 4fs is equivalent to an energy resolution of 1.6KeV.

Kicker Strength Requirement

Our synchrotron frequency f_s is 2KHz and our synchrotron damping time is 3ms. We aimed at reducing this damping time down to ≈1ms (2 synchrotron periods). The kicks producing this damping will add up over a large number of turns: our revolution period is 2.8µs, ie 160turns/ms. It means that given the 4fs time resolution achievable with the scheme described above, a relatively modest kicker strength will be sufficient to control oscillations of initial amplitudes very large compared to the resolution of our phase detector. For instance a synchrotron oscillation driven by a kicker with a 1KV maximum strength will grow up to an amplitude of .25ps in 1ms.

Kicker Design

Our kicker is a low Q pill box cavity following the scheme imagined at INFN Frascati[1]. We duplicated the design of the cavity used for the SLS longitudinal feedback with a slight change in dimensions due to our different center frequency. The shunt impedance obtained is 1700Ω. With such a cavity we are able to produce a 600V kick using a 200W RF amplifier. To drive this cavity we are using the QPSK modulator scheme developed for the PEP longitudinal feedback [2]

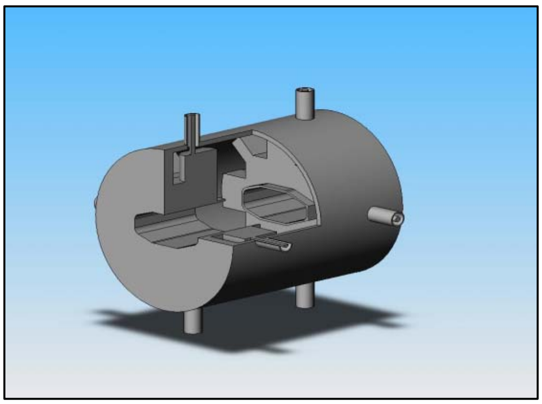

Figure 2: longitudinal kicker shape.

DIGITAL SIGNAL PROCESSING

Principle of the Correction Signal Computation

For the longitudinal feedback, we measure for each bunch a phase deviation, and we must apply an energy correction; so the correction signal should be ideally the derivative of the error signal, with some gain. Such a derivation is difficult to calculate without generating noise, so we approximate it with a $\pi/2$ phase shift; this approximation is valid as long as both error and correction signal are quasi sine signals. This is true since a bunch signal for an oscillation of moderate rise and damping time ($<2/f_s$), is a sine signal at the synchrotron frequency. We obtain the desired band pass filtering and phase shift with a digital finite impulse response (FIR) filter. For the longitudinal feedback we use a use a decimation by 11 followed by a 16taps FIR;

Spurious Phase Signal Due to the Beam Loading

A part of the bunch to bunch phase variation is due to the variation of the cavity voltage during one revolution period when the filling pattern is not perfectly uniform (beam loading effect); this leads to each bunch having a constant phase offset different from other bunches. The amplitude of the beam loading driven signal can be larger than the optimum +/-32ps dynamic range given in the table 1 for the input of the 14bits ADC. To avoid increasing this dynamic range which would spoil the resolution of the phase signal analog to digital conversion, we have implemented a periodic notch filter (beam loading filter of figure 1) between the phase comparator and the input of the 14 bits ADC to remove as much as possible the harmonics of the revolution frequency. This notch filter is implemented on an auxilary FPGA board; The ADC of this board takes 124 samples of the beam phase per turn and computes for each sample the value of the beam phase averaged over one synchrotron period. This value is used to generate an analog average beam phase signal which is removed from the raw output signal of the beam phase detector by an analog substraction performed with a wide band signal combiner. Any residual beam loading signal is eventually completely removed by the FIR filter used for the main feedback algorithm, since the sum of the coefficients of the filter is zero, which allow applying a large gain to the error signal.

DSP Plateform

The phase measurement resolution and the kicker strength requirement assumed above will require a phase data acquisition rate and correction calculation for each bunch of one sample per turn without any under sampling. Such a processing rate is only achievable if we use a FPGA processor. After considering the different platforms and programming environment potentially adequate for our project, we went for the following solution: we use a special development of the *Libera* bunch signal processor developed by *I-Ttech* for the error signal acquisition, signal processing and correction signal generation. The main feature of this product are: up to 500 Msps ADC and DAC sampling rate with 14bits resolution, *Virtex II* pro FPGA with 64 Mbits of DDRAM for data logging.

Programming Environment

We wanted to be able to reprogram flexibly by our self the details of the feedback algorithm and we could not rely on a dedicated expert in FPGA programming for this project, therefore we specified that the *System Generator* programming environment should be available for the *Libera* platform. *System Generator* is a graphical programming environment developed by *Xilinx* and the *MathWorks* which allow defining and validating a processing algorithm at the bit and sample level using a library of *Matlab/Simulink* models provided by *Xilinx*., The availability of this kind of programming environment is one of the reasons to the relatively short time that was needed for the coding and testing of the feedback algorithms on the FPGA during this project.

LONGITUDINAL FEEDBACK TESTS

Test Set Up

In order to assess the effect of the longitudinal feedback we added to the components of the feedback loop a signal generator able to add test signals at the frequencies of the modes of oscillation of the beam at the kicker input. We used a gated Agilent 4395 spectrum analyser to record the amplitude of beam phase oscillation with and without feedback.

Tests Results

The most significant result of these tests is shown in the figure 3. We have plotted the display of the phase signals measured with the spectrum analyser in the so called zero span mode; in this mode the analyser displays the variation in the time domain of the amplitude of the input signal oscillation filtered by a 30KHz bandwidth band pass filter around the frequency of the coupled bunch mode under study. The left plot is obtained with a stable beam at 200mA when the oscillation of the mode 407 (144.503MHz) is forced by a continuous signal of the test generator, and the feedback is turned on and off every 15ms. On the second plot the current is 250mA; above 200mA our the beam is unstable on this mode without feedback; when the feedback is turned off we see the oscillation initially grow exponentially with a 1ms rise time, and as soon as we turn the feedback on again, we observe the damping of the oscillation in a bit more than 1ms.

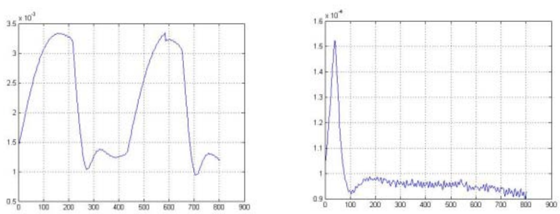

Figure 3: effect of the feedback on a bunch coupled longitudinal oscillation (mode 407).
left: forced oscillation of a stable beam
right: unstable oscillation driven by a RF cavity HOM
horizontal scale: 4ms/div, vertical scale: a.u.

TRANSERSE FEEDBACK DESIGN

Feedback Layout

There are 2 separate systems for the vertical and horizontal plane. The layout of the transverse feedback is shown on figure 4.

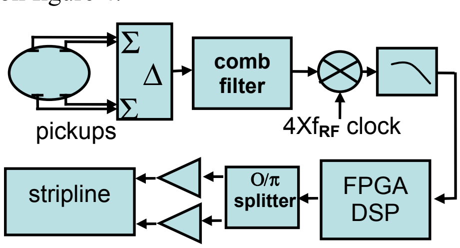

Figure 4: Layout of a transverse feedback system.

The beam signal pickups are 11 mm diameter capacitive electrodes located in high beta H and V locations (36m for both plane). The RF front end detects the position by a synchronous detection of the difference signal of the BPM pick up signals. We perform the detection on the 4th harmonic of the RF frequency in order to increase the sensitivity and to ease the filtering of the 0 to 176 MHz base band signal from the RF clock spurious signal. We are using strip line kickers to apply the correction kicks. Each blade of the strip line is fed by a 100W/200MHz BW solid state power amplifier.

Signal Processing

For the transverse feedback we make the same derivative/phase shift approximation as for the longitudinal feedback, but the phase shift between the error and correction signals will also be function of the betatron phase shift between the BPM and the transverse kicker; we use an 8 taps FIR in the vertical plane and a 7 taps FIR in the horizontal plane, without decimation.

Feedback parameters	*vertical*	*horizontal*
Measurement range	+/-.4mm	+/-1.5mm
Resolution at 200mA	7μm	7μm
Kick strength per turn	.3 10^{-6} rd	.6 10^{-6} rd
Min. damping time	100μs	200μs
Added noise	.5μm	.25μm

Status of the Transverse Feedback

The components of both horizontal and vertical systems are now installed and tested. The FIR filter algorithm has been tested on the beam vertical position signal and the resolution of the position measurement checked.

CONCLUSION

The implementation of a bunch by bunch feedback used to be a very challenging task. It is now a well proven technique thanks to the experience gained on feedback systems implemented on many machines during the last 10 years. In addition, thanks to the availability of fast and accurate ADC and DAC, powerful DSP using an FPGA, and user friendly programming environment, it showed to be a relatively straightforward piece of equipment to design and implement.

ACKNOWLEDGMENT

Michael Dehler from SLS helped us a lot by allowing us to use his design of the longitudinal and horizontal kickers.

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