ISAC II RF CONTROLS - STATUS AND COMMISSIONING*

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Abstract

The rf control system for the 20 ISAC II superconducting cavities is a hybrid analogue/digital design which has undergone several iterations in the course of its development. In the current design, the cavity operates in a self-excited feedback loop, while phase locked loops are used to achieve frequency and phase stability. One digital signal processor provides amplitude and phase regulation, while a second is used for mechanical cavity tuning control. The most recent version has been updated to incorporate newer hardware and software technology, as well as to allow for improved manufacturability and diagnostics. Operating firmware and software can be updated remotely, if the need arises and system security permits. This paper describes the RF control system, outlines the status of the system, and details the commissioning experience gained in operating this system with five four-cavity cryomodules.

INTRODUCTION

This paper briefly reviews the development and outlines the design of the TRIUMF superconducting rf control system. It then details some of the test results obtained over the course of about two years of testing – initially with single cavities, progressing to four cavity cryomodules, and finally with commissioning of the full 5 cryomodule accelerator. A number of design changes proved necessary and/or desirable during this time, and some of these are described. Finally, a few conclusions are offered.

RF CONTROL SYSTEM

Figure 1 shows a block diagram of the current superconducting controls design implementation. While many elements of this system have been documented elsewhere [1], they are reviewed briefly here. A commercial crystal-referenced synthesizer provides the reference to the frequency distribution system via phase-stable coaxial cable. A custom designed synthesizer had been used previously but was found to have sidebands which were contributing to the system phase noise.

There are two phase detectors in the system. One is used for phase regulation, while the second controls the tuner. Both of these are implemented in a single programmable gate array and have been described in an earlier poster [2]. Also shown on the block diagram and incorporated in the PLA design are two frequency counters and a subtracter. The counters have a resolution of 1 Hz and are used to measure and compare the reference and cavity frequencies. The counters are used to perform initial tuning of the cavity to within the desired phase lock range (about 10% of the cavity bandwidth). In future they may be used to force the phase detector output high or low to speed convergence of the PLL to the reference frequency.

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As mentioned, a single DSP is used to control both the amplitude and phase loops. Originally a single multiplexed A/D convertor was used to digitize both of these input signals. It was found that even with all possible steps taken to minimize crosstalk, there was still some noticeable interference, possibly due to residual charge storage in the shared sample and hold circuit. To eliminate this problem, separate A/Ds are used in the current design. These have a resolution of eighteen bits, which places digitizing errors well below the noise floor of the system.

The tuning loop is implemented in a second DSP, and provides conventional PI control to the tuner servomotor. A second low bandwidth loop has been added to the tuner system via the system software. When all the loops are closed, this loop looks at the phase drive signal and adds/subtracts from the tuner drive to minimize the phase drive. The principal tuner loop has a bandwidth of about 40 Hz. This may be enough to provide some damping of the lower frequency microphonics, but not enough to damp the cavity fundamental resonance of about 75 Hz. These lower frequency mechanical resonances are filtered by a first order Kalman filter. The filtered signal is combined with a similarly filtered signal from the Q-loop to minimize the drive power required by the frequency/ phase loop.

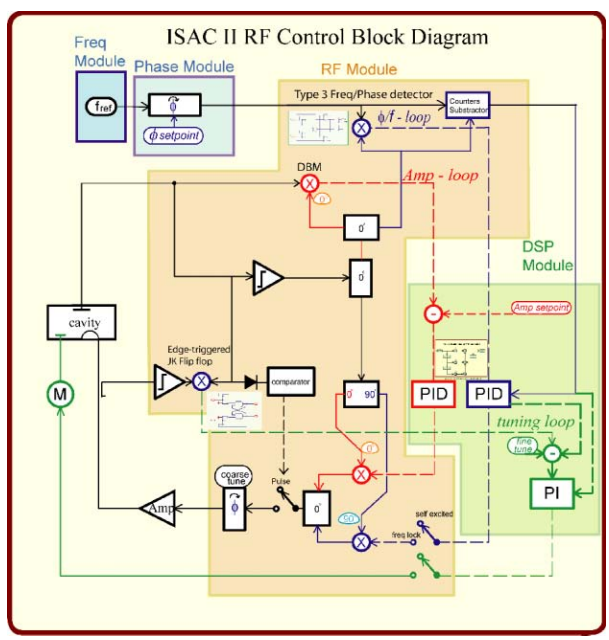

Figure 1: Superconducting Control System

Frequency/ Phase Detector

For the benefit of those who may not have seen the aforementioned poster, some of the features of this design are outlined here. It is implemented in a Xilinx FPGA (XC3S50). The operating frequency is 106 MHz. The phase loop detector is a type 3 detector with a linear range of +/-

180 degrees. An output waveform from this detector is shown in figure 2. It displays good linearity and the necessary DC offset to enable phase locking. In operation, the tuner is used to bring the cavity within about 1 Hz of the reference before the phase and tuner loops are enabled. The software employs a sliding mode control algorithm to facilitate rapid convergence to the desired frequency. Basically, this reduces the gain as the frequency converges. A deadband is also employed to minimize overshoot when the target is reached.

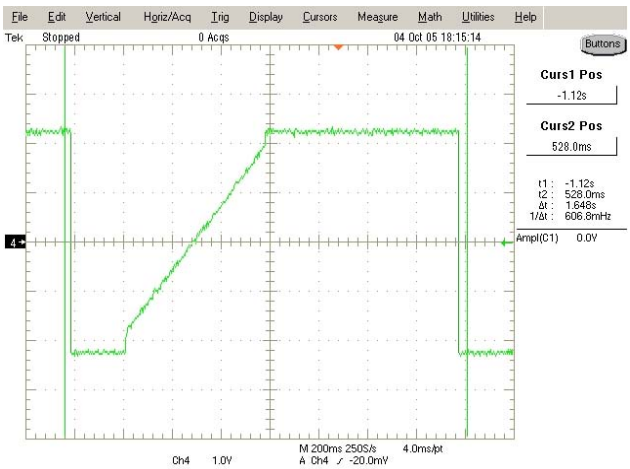

Figure 2: Frequency /Phase Detector 1

The second phase detector included in the gate array is used to control the tuning loop. This is a somewhat simpler design. It also has a linear range of +/- 180 degrees, but the output does not require memory. The output waveform of this detector is shown in Figure 3. It is the characteristic sawtooth waveform of this type of detector. Also evident is some crossover distortion around the middle of the linear range. This is not particularly critical in this application (minimizing reflected power), and may even be an advantage (slight reduction in gain around operating point). It is one of the problems with this type of detector.

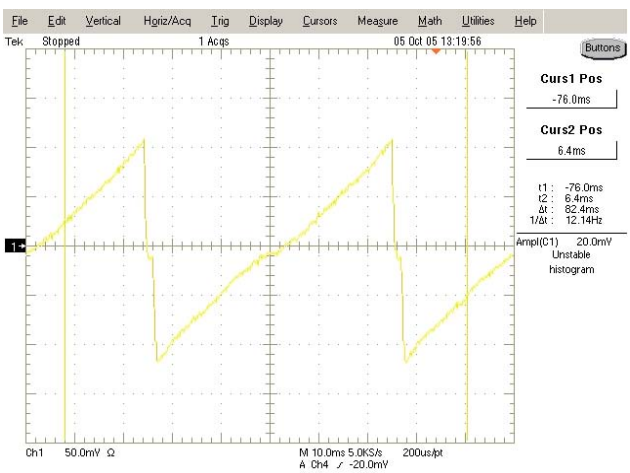

Figure 3: Phase Detector 2

Control Software

The rf control software is EPICS-based. It incorporates a number of safety interlocks, and has been updated to provide improved tuning control. This is indicated in Figure 4. Each PC can control up to 4 cavities, and each cavity is controlled independently by a separate task with its own EPICS virtual IOC. This is indicated as the upper left node in the figure.

All control parameters and status readback values can be access remotely by EPICS. Not shown in the figure is that up to 4 of these nodes can be running simultaneously.

The upper right node is used to control common shared resources such as the tuning motor controller and GPIB controller. This node communicates with the cavity controller tasks with shared memory inside a dynamic linking library, as indicated by the package labeled “shared memory DLL”. Since the regulation bandwidth of the tuning loop depends on the communication throughput between the controller node and the common resource node, with this configuration the data update rate to the tuning controller is only limited by the maximum write speed of the hardware. Finally, external safety parameters are read via EPICS with another task, located in the bottom of the UML diagram. The safety parameters are distributed to all the controller tasks with the shared memory DLL. At the present time while we are still at the developmental stage, all the tasks have built-in graphical user interfaces. A replica of the graphic user interface with full control/status display can be employed remotely via EPICS. We may remove the local graphical user interfaces when we have completed the commissioning stage.

Commissioning

Commissioning of the ISAC II accelerator controls consisted of a number of steps. Cavities and controls were first tested individually in a test stand. They were then integrated into four cavity cryomodules which were again tested in the test stand. Finally, the cryomodules were installed one at a time into the accelerator vault, the refrigeration system connected and tested, and the final commissioning work begun. Further information on the cavities and their test results can be found in [3]. The latter task was complicated by an interlock system which mandated that no one be present in the vault while rf power was applied to a superconducting cavity, due to possible x-ray emissions.

While integration, testing and commissioning involved dealing with the usual bugs one might expect in a system of this size, there were still a number of surprises. The cavities are driven by 1 kW tube amplifiers. A bad case of microphonics in one of the cavities was traced to a faulty tube which was picking up mechanical noise from the cooling fans. Due to over-etching to meet Q specifications, two of the cavities had to be modified to raise their operating frequency to within range of the tuning system. The method elected was to add a disk-shaped appendage to the tuning plate. This changed the frequency, but had the undesired side effect of increasing the tuner gain by a factor of three. The net result was that these two cavities pose a much more difficult control problem than their neighbours. Other difficulties included loss of performance possibly due

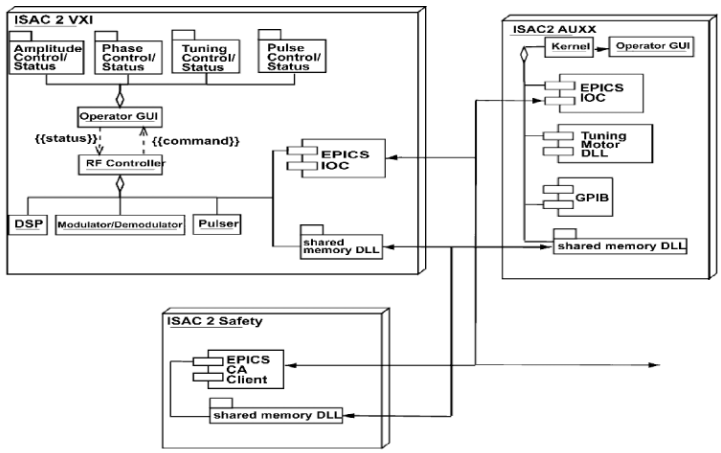

Figure 4: Control System Deployment Diagram

to contamination during the process of transporting cryomodules from clean room to accelerator vault. Conditioning managed to improve the performance of all cavities to the point where they provide useful field strength. Some still have some residual multipactoring making it difficult to bring up the cavity without some manual intervention such as adjusting the coupling loop. Finally, differences in residual phase noise between cavities by factors of up to 3 to 1 have yet to be satisfactorily explained. A typical phase noise spectrum obtained from one of the control systems is shown in figure 5. Some peaks at the 60 Hz powerline frequency and harmonics at 120 Hz and 180 Hz might be expected. The somewhat broader peak at about 75 Hz is the cavity mechanical resonance. Yet to be explained are the apparent subharmonics of the line frequency. These show distinct peaks at 30, 15, and even 7.5 Hz. The power supplies of the commercial tube amplifier used to drive the cavity are the prime suspect at the moment. When this plot is integrated and normalized to

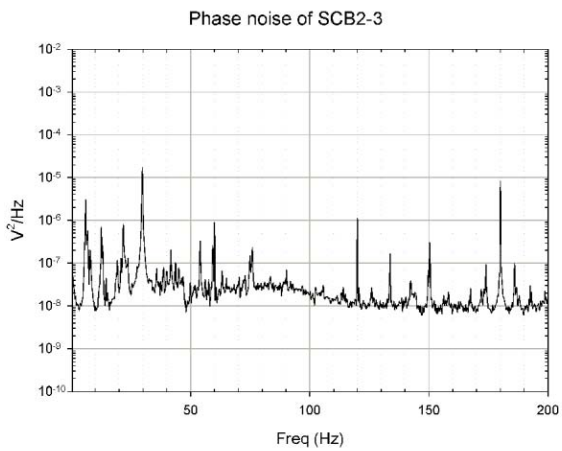

Figure 5: Typical Residual Phase Noise Spectrum

the phase detector gain, the rms phase error equates to less than 0.3%, well within the accelerator requirements. A background scan with the reference signal applied to both phase detector inputs yielded a base noise level of 0.03 degrees rms over the same 200 Hz bandwidth.

For a detailed account of the accelerator commissioning, see [4].

CONCLUSION

The control system has met the accelerator requirements for amplitude and phase error. Amplitude control to within 0.2% and phase control to within 0.3 to 0.8 of a degree has been demonstrated. The design was successfully updated to include newer DSPs (56303) and A/Ds. Gains of the respective control loops have been optimized for the system. Some further improvements, particularly in the area of phase noise, may be realized with further analysis of the noise sources in the system. For the next stage of the accelerator, up to 8 cavities per cryomodule are required. To accommodate their control requirements within a single 13-slot VXI mainframe, a new control module incorporating both the rf modem and DSP functions would be required. This option is currently being investigated.

REFERENCES

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[4] R. Laxdal, K. Fong, M. Marchetto, W. Rawnsley, I. Sekachev, G. Stanford, V. Verzilov, V. Zviagintsev, “Commissioning the ISAC-II Heavy Ion Superconducting Linac at TRIUMF,” TUPLS031, this proceeding.