DIGITAL MASTER OSCILLATOR FOR THE ISIS SYNCHROTRON

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Abstract

Rutherford Appleton Laboratories in Oxfordshire is home to an 800MeV synchrotron particle accelerator called ISIS. Its main function is to direct a beam of protons into a heavy metal target to produce neutrons for scientists to analyse condensed matter. A second harmonic system is being developed to upgrade the beam current from 200μA to 300μA in order to drive a second target station. This is being achieved by the inclusion of four second harmonic cavities to increase the width of the RF bucket. In the past the six fundamental cavities were driven by an analogue Master Oscillator but the extra cavities will bring more difficultly in the phasing of the system. This could be more easily and precisely controlled by using a Direct Digital Synthesis system (DDS) as the heart of a new digital Master Oscillator.

This paper describes the initial research and feasibility of such a system for the setting up, phasing and synchronisation of the ten cavities in the ring. It also describes how more of the controls to the oscillator can be encompassed by digital means.

INTRODUCTION

The Fundamental system is relatively easy to phase as the cavities are arranged in geometrically opposing pairs in the ring and so only require three pairs of drive signals. With the introduction of four 2nd Harmonic cavities (2RF) in close proximity in superperiods 4, 5, 6 and 8, the phasing becomes extremely difficult. Theta phase has to be introduced which is a dynamic phase shift between the Fundamental and the 2RF cavities, along with the static phase between each 2RF cavity due to their position in the ring. Therefore if a digital system could be used this would lead to precise control of the ring and be more easily implemented using digital techniques.

EXISTING SYSTEM

The existing system consists of a Voltage to Frequency Converter (VFC) producing a variable frequency pulse which is then converted using a pulse to sine converter. This single output is passed to a phase splitter to provide the three RF signals to the three pairs of fundamental RF cavities. The fundamental cavities are swept in frequency from 1.3MHz to 3.1MHz. The input to the VFC is a differential analogue voltage which is generated by the RF Frequency Law Generator before the other RF loops (radial loop, beam phase loop, bunch-length loop and trim function) are added. The scaling on this analogue voltage is: 1V = 500kHz.

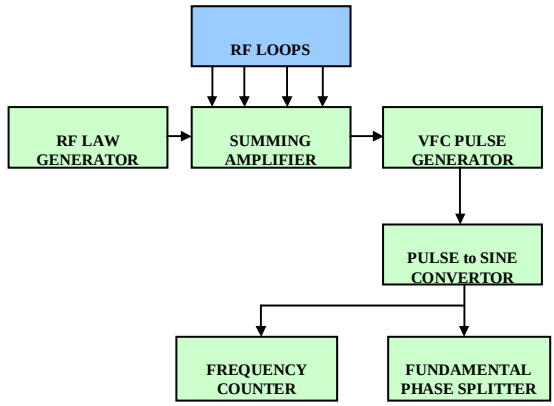

Figure 1: Existing RF frequency generation.

DDS INVESTIGATION

DDS Operation

The basic system comprises of a large Look Up Table (LUT) containing sine values. When it is addressed from start to finish, the digital values are put through a DAC to produce an analogue sine wave. Each value is produced on every system clock cycle (fclk). If a step (or skip) value is added to the address then the table completes the cycle in a shorter time so producing a higher frequency. This can be precisely controlled using digital means and is locked to the stability of a crystal oscillator.
If two systems are used then adding an offset to the step value can give a precise phase shift between channels.

Initial Research

DDS chips were first evaluated but it was shown that the required frequency change rate couldn't be achieved due to the way the tuning words are serially loaded into the devices. The parallel chips require loading the tuning word with six serial blocks, and the serial chip tuning word was limited by a 25MHz serial clock. What was needed was a parallel scheme.

Therefore embedding a DDS system in a Field Programmable Gate Array was investigated to see if the frequency could be changed every system clock cycle. Also the added advantage using this device would be to use the remaining logic gates to control the whole system.

FPGA

An evaluation board containing the Lattice® Semiconductor LFECP20 FPGA was used to investigate if a DDS system could be instantiated. Evaluation boards for the DAC and ADC were connected to this.

A Field Programmable Gate Array (FPGA) is a re-configurable logic device that can be programmed in the field using a hardware description language (called VHDL in our case) so is application specific. It is made up of Configurable Logic Blocks which comprise of a Look Up Table which is programmed with the truth table of combinational logic and can either be synchronously clocked out or be concurrently set. An FPGA is a truly parallel device.

This one was chosen because it contains:

- 4 Phase Locked Loops (PLLs)
- 28 18x18 multipliers
- 7 DSP blocks
- 424Kbits Embedded Block Ram
- 19700 LUTs (≡ 1.5M logic gates) [1]

It is hoped that the output low pass filters could also be built inside the FPGA using the embedded DSP cores at a later stage.

Simulation

Simulation of digital circuits is easily achieved using software packages. A VHDL program is tested by running a test bench (also written in VHDL) to drive the code and show the resultant waveforms that would come from the FPGA. This enables the programmer to see the results and affect changes. This simulation package is called ModelSim® by Mentor Graphics® and is included in the ispLEVER® programming environment [2] that was purchased from Lattice. It was used at all stages of code development and proved to be an invaluable asset.

FIRST TRIALS

Creating a single channel DDS system in the FPGA was first tried but found to have problems due to the Embedded Block Ram (EBR) in the FPGA being only 53kB. Therefore ¼ sine tables were used to emulate a larger sine wave table for the system but lacked resolution. Cordic Algorithms were then experimented with in order to calculate the sine values 'on the fly', but even when employing the embedded math modules it was found to take seven to eight system clocks cycles to change the frequency. This slow rate of change would therefore not 'mimic' an analogue system, or follow the rate of change from the Frequency Law Generator.

The system proved most efficient when it was reconfigured to have a 2^{21} counter with the result divided by 8192 to index a 255 address EBR 8-bit sine table so simulating a 2MB RAM. This provided a good spread of data to the 8-bit DAC producing a sine wave that changed frequency within a clock cycle; see Figure 2 below.

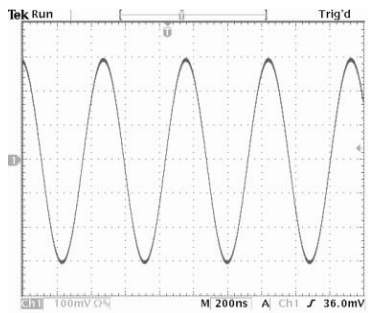

Figure 2: Output from DAC passed through the 'scope's 20MHz low-pass filter.

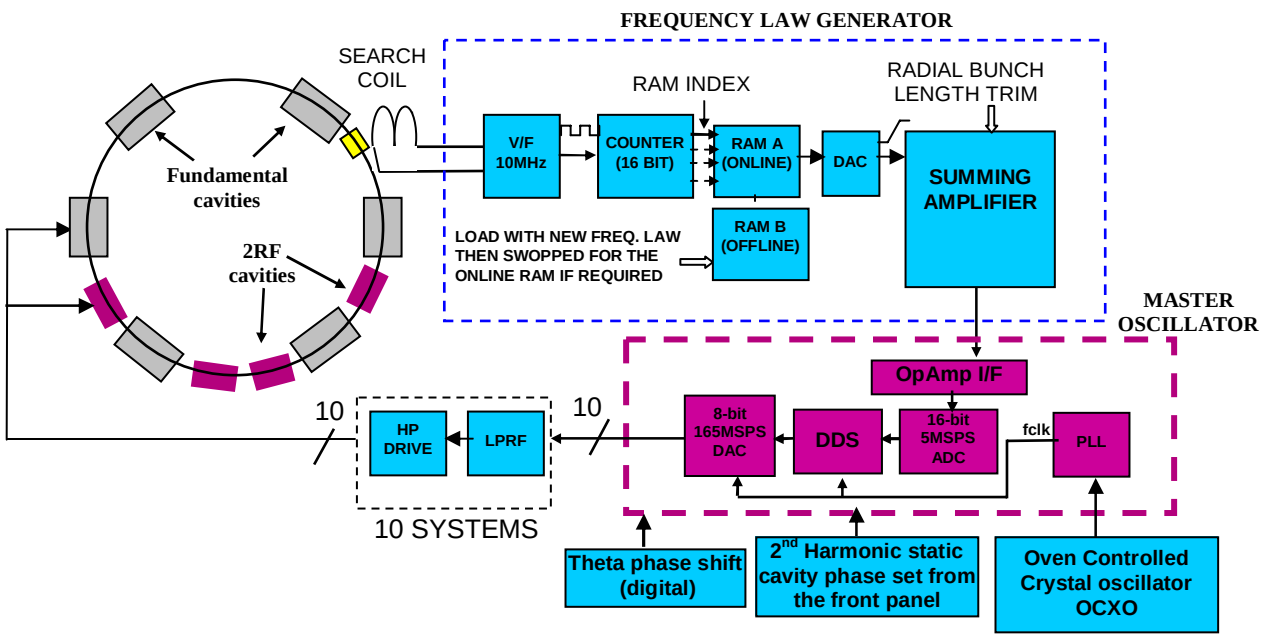

Figure 3: Cavity drive system incorporating the Master Oscillator.

Possibilities Arising

The successful creation of the DDS system in the FPGA led to the realisation that more control functions in the Master Oscillator could be encompassed and therefore reducing some of the existing instrumentation. For example:

- All the Fundamental cavities could be driven directly without a phase splitter.
- If connected to the machine's ΔP signal and the RF loop signals digitised, the RF law can be stored in the FPGAs thus eliminating the summing amplifier and Frequency Law Generator (FLG).
- The analogue drives that determine the phase relationship between the Fundamental and 2RF cavities could be replaced for digital units so being able to connect directly with the FPGA rather than through ADCs.
- Front panel digital potentiometers could be used to set static phase shifts between the 2RF cavities and also provide a facility to change parameters for setup and test purposes.

Proposed First System

Figure 3 shows the intended first prototype system setup to test the Master Oscillator. This will involve all ten cavities being driven and a digital input to the instrument to set the phase between the Fundamental and 2RF cavities. Front panel digital potentiometers will be included so tests such as modulating the fundamental frequency only (for example) will be possible. An embedded PLL in the FPGA will be used to multiply up the lower standard frequency of a crystal oscillator to provide a system clock as this proved to work well on the prototype. An oven controlled crystal oscillator will now be used here.

If this proves successful then the next stage will be to include the FLG system.

RESULTS

Testing

Testing of the VHDL software was straight forward as the simulation package aided development allowing test benches to be written which showed all the waveforms running. Code was downloaded to the FPGA with the ispLEVER® programming environment and the resulting sine wave was created as shown in Figure 2. The requested frequency is derived from the equation:

$$\text{Frequency} = \frac{Step\ value * fclk}{counter\ size}$$

$$\text{Hence the resolution} = \frac{fclk}{counter\ size}$$

The interface OpAmp circuits were designed to provide a correlation between the frequency equation and the ADC in order to provide a voltage to frequency ratio of 1V = 500kHz output. A voltage sweep from an HP signal generator was set up to simulate the input from the summing amplifier to demand frequencies from 1.3MHz to 3.1MHz. A slow rate of 5 seconds was applied to initially prove the system, and the required frequencies were seen on a Tektronix oscilloscope. Then a 50Hz sweep was applied and continuously changing sine waves were observed. Dummy values for 1.3MHz and 3.1MHz were created in software so bypassing the ADC in order to check the rate of change in frequency and this proved to be within 10ns as viewed on the oscilloscope.

Achieved DDS Specifications

• System clock rate	132MHz
• Frequency change time	<10ns (one fclk)
• Resolution	63Hz
• Simulated sine wave table	2MB
• Frequency range	1.3MHz to 3.1MHz (X2 for the 2RF)

CONCLUSIONS

The readings from the oscilloscope have shown that a digitally generated sinewave can certainly be produced from an FPGA, and that the frequency can be accurately controlled by a simple equation. With two or more channels it is entirely feasible to create phase shifting by digital means as well, therefore making it worth while now to move away from the evaluation boards and build a ten channel PCB with the capacity to read digital potentiometers. This is currently halfway through design and will facilitate development of phase shift tests.

The next report will be regarding trials in the synchrotron. If the preliminary resolution (63Hz) is not sufficient then the system might need to be reconfigured to improve this. All this can be done in software.

ACKNOWLEDGEMENTS

Thanks are due to Andy Seville for his support relating to the current Master Oscillator system and suggestions for this new development. Also thanks are due to Derek Bayley for his support on the analogue interface part of this project.

REFERENCES

[1] Lattice ECP/CE Family Data Sheet Information.
[2] http://www.latticesemi.com/products/designsoftware/isplever/advancedimplementationtoo.cfm