MACHINE PROTECTION BY ACTIVE CURRENT-TRANSMISSION CONTROL AT GSI-UNILAC

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Abstract

Numerous beam current transformers (BCT) are installed at dedicated locations along the UNILAC accelerator. Each one provides an output signal for transmission loss control purposes. Dedicated pairs of these signals from consecutive BCTs feed differential integrator stations. If preset thresholds are exceeded due to local particle transmission losses or thermal overload of profile harps, interlock signals are instantly generated during the present macro pulse by the corresponding stations. The actual beam pulse is then immediately truncated by a fast beam chopper, thus any thermal damage or activation of machine components is prevented.
An upgraded BCT macropulse selector/display (MAPS) is presently under construction, which will provide time structure observation of multiple UNILAC macropulses from the BCTs, as well as long-term measurement data logging. The hardware is set up with PXI components from NI®, running a multi-client/server controller software under LabViewRT®. An offline-analysis of accumulated BCT data will further improve the protection system's operation and operational reliability.

INTRODUCTION

Since the intensity upgrade of GSIs UNILAC accelerator ion beam currents have been increased well above 10 mA of e. g. $^{238}U^{28+}$. Calculations of stopping power loads [1,2] on insertion devices exposed to the beam indicated, that machine protection would become a mandatory task. Based on the existing BCTs, a safeguard for the machine and its instrumentation devices was designed and installed. During the last years it was constantly expanded and improved.

BEAM CURRENT TRANSFORMERS

Each BCT along the UNILAC and the is equipped with a local head amplifier [3], which provides a calibrated output voltage with switchable gain factor. An additional differential output with a fixed transimpedance forms the input signal of its associated loss integrator, interconnected by a twisted pair line. Both outputs provide adequate rise-time and pulse droop error values allowing a true representation of the macro-pulse shape [4].

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Table 1: BCT specs

max. beam current	100mA
typ. resolution	~ 500nA, full BW, 1ms pulse
rise-time	< 2 µs
droop error	< .1% for 1ms pulse length

LOSS INTEGRATORS

The loss integrator stage contains two clock-synchronous V/f-converters with a maximum frequency of 8 MHz, which are driven by the BCT signals from two consecutive machine locations, respectively. These converter pulses, with their frequency being proportional to the instantaneous beam current, clock an UP/DOWN-counter. A half-period shift between the XCO master clocks of both channels avoids any overlap, so beam charge will be reliably summed up. Each pulse represents a fixed amount of beam charge. Feeding the UP-input with the pulses from the first BCT and the DOWN-input with the second signal, the counter value represents the instantaneous charge difference, which is eqivalent to the ion transmission loss along the measurement section. The counter, two threshold comparators and additional digital logic have been implemented into a CPLD (ALTERA® 7000 series).

Table 2: loss integrator specs

max. differential beam charge	18000 nC
typ. charge resolution	2.2 nC
offset error	± 5 nC
temp. coefficient of gain	~ 200 ppm/K

Up to 8 integrator boards can be installed into a common 19"-crate. In the standard configuration scheme, every unit's DOWN-input is internally routed to the next UP-input. Connection to the control system is done via MIL-Bus interface and a VME-based controller. All crates are located in a common rack.

For three different safety tasks dedicated versions of the loss integrator have been designed.

Charge loss monitoring

This type comprises the UP/DOWN-inputs, a single programmable loss threshold and an interlock output for wired-OR connection on the crate's backplane. Each crate drives its single interlock line to the chopper control station (CCS).

Presently 12 units are portioned to the 19"-chassis, partitioning the UNILAC into associated safety segnents. They are always active during machine beam times, acting as the main safety guards in the background..

Profile harp protection

These are used to protect the wires of the profile harps against thermal damage. Only the UP-input signal is used, and routed to the next unit, while the DOWN-input is unused. Thus the absolute beam charge passing the assigned BCT is monitored, and the beam power load on the harp wires is dynamically reduced if necessary. The interlock signal is routed via a front panel socket to a different input at the CCS.

For harp protection the UNILAC is partitioned into four segments. The associated protection units in that case evaluate the second threshold, which had been calculated and set prior to any movement of the harp actuators.

Operation is activated by an operator's push-button, which also enables the harp actuators.

Emittance harp protection

These modules a priori work like the standard unit, evaluating the first threshold, and controlling the transmission loss. If an emittance measurement (slit-harp method) has to be performed, the participating harp's wires must be protected. For this purpose, the unit's active threshold is changed by the CCS, and the unit is then switched into the absolute (harp-protection) operation mode. In the assigned machine section, the arrangement of the elements is: 1st BCT – high power slit – 2nd BCT - profile harp. Due to the massive, but unavoidable beam loss on the slit, the loss control function must be disabled, and the 2nd BCT now has to be used. The DOWN-signal is connected to the UP-input, while the DOWN-counter idles.

GATE PULSES AND INTERLOCK

The CCS collects the various interlock signals, checks their relevancy with respect to the present state of the accelerator, and sends the control signals to the beam chopper. The dynamic truncation action starts at 100 µs beam pulse length, and is limited to 10 µs, which is the shortest usefull value for beam diagnostic instruments like harps, BCTs or Faraday-cups.

4 OPERATIONAL RESULTS

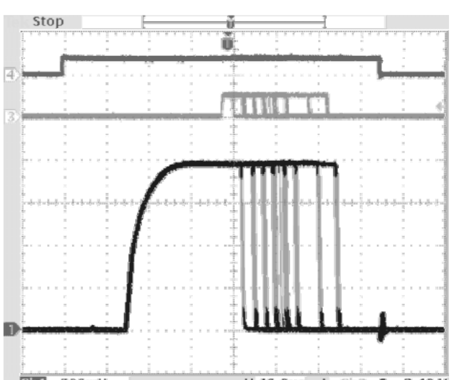

Fig. 1 Beam pulse truncation due to varying transmission loss

The counting pulses are gated by appropriate timing signals in order to exclude erroneous counts from electromagnetic disturbances during the pulse gaps. The CCS provides these pulses, while keeping the macro-pulse always enclosed by the gate. Fig. 1 shows the count-enable signal (ch4), the BCT gate pulse (ch3), and the BCT analogue signal (ch1). Transmission loss was manually induced by a beam steering magnet.

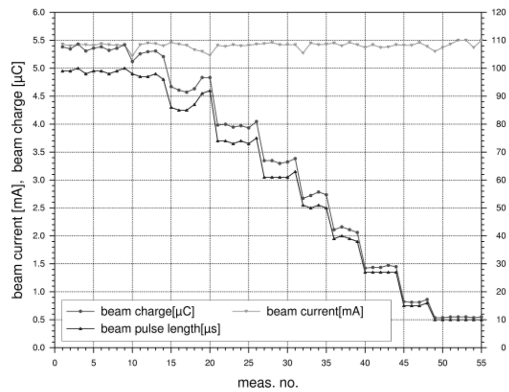

Fig. 2 Beam-pulse charge and length (see Fig.1)

Fig. 2 depicts the corresponding values of beam charge and macro-pulse length during the described manipulation. The average beam current is also shown for reference.

NEW MACRO PULSE SELECTOR

Old MAPS System

The UNILAC accelerator produces heavy ion beam pulses, at most with 50 Hz repetition rate. The beam parameters (ion, energy, intensity etc.) can be switched from pulse to pulse. From BCTs in 40 positions along the beam line the pulse current waveforms are digitized synchronously at 2 Ms/s with 8 bit resolution. A user-selectable subset of these current waveforms can be displayed together with their corresponding digital gate pulses from the UNILAC timing control unit, as well as the integrated current and pulse length from the transformer digitizer stations.

In the old MAPS only two waveforms could be acquired and visualized at the same time, by using analog-multiplexers. The data acquisition and visualization was performed by a monolithic program on a stand-alone PC under MS-DOS. Since several hardware components are not available any more and, with respect to the challenging FAIR project, the requirements for a distributed and more flexible system became more important, and work was started for a replacement.

Upgraded System – Architecture and Hardware

A new system, based on National Instruments Hardware and Software, was developed [5, 6]. The overall architecture of the upgraded system is shown in Fig. 3. A client-server approach was chosen to create a distributed system. The communication protocol is based on TCP/IP-socket connections. The server manages the client requests with a lower priority than the data acquisition which is running in a time critical thread. A FPGA board is used to read the pulse ID, integrated current and pulse length from the transformer electronics and to detect gates and triggers from the timing control unit.

The client can be started on any computer with installed LabView runtime engine and a network connection. The server is running on an embedded NI-PXI-8186 controller (2.2 GHz Pentium 4-M, 1GB RAM, 100 Mbit Ethernet). Up to 112 analogue waveforms will be measured with 8-channel simultaneously sampling ADC cards NI-PXI-6133 (2.5 MS/s, 14 bit, 16/32 MB onboard memory). A NI-RIO-7811R FPGA board is used for digital I/O.

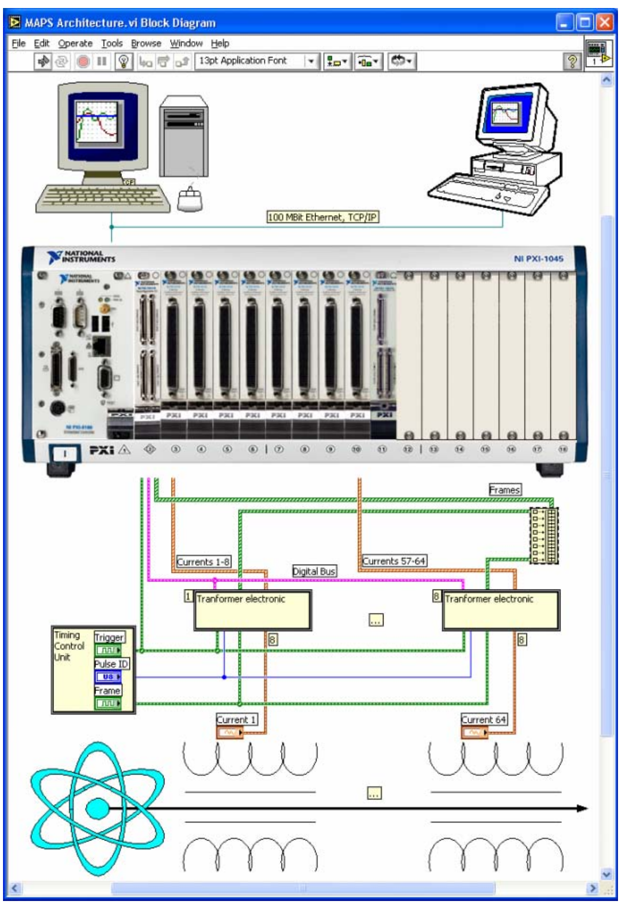

Fig. 3 Architecture of the upgraded system [4]

Software Application

A dedicated LabView Real-Time OS is used to implement the server and data acquisition loops. The FPGA module is programmed to configure the NI-RIO board. The consumer-producer pattern is applied to implement the client-server association. The client registers itself at the server for a subset of available data. If new data become available they are sent automatically to all registered clients.

The time critical DAQ loop is implemented as a state machine with well defined transitions for configuration, data acquisition and error handling. Commands and measured data are exchanged with the server loop by event driven communication. The DAQ system is externally triggered by the timing control unit at 50 Hz. The onboard-memory of the DAQ cards is sufficient to buffer 10 ms pulses completely so that the CPU is decoupled from the DAQ. The FPGA board is used to implement the transformer bus protocol and to measure the relative timestamps of the timing pulse edges.

Status & Outlook

A first functional test was performed successfully by simulating the not yet finished transformer bus interface and analog signal distribution with an additional NI-RIO-7831 FPGA board and a NI-PXI-6070 MIO card. However, the system is not yet in the final stage, and needs further improvement.

The new interface boards which manage the data transfer between the NI-RIO-7831 and the BCT device bus inside the transformer electronics are presently developped at Brunel-IMG GmbH, Nordhausen, Germany.

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