COMMISSIONING OF A NEW DIGITAL BPM SYSTEM FOR THE PSI PROTON ACCELERATORS

B. Keil, P.-A. Duperrex, U. Mueller, PSI, Villigen, Switzerland.

Abstract

A new digital beam position monitor (DBPM) system has been developed and successfully tested at the PSI proton accelerators. The DBPM hardware consists of an analogue RF front-end (RFFE), a VMEbus backplane module (VBM), and the PSI VME PMC Carrier board (VPC). The RFFE combines the 2nd RF harmonic (101.26 MHz) beam signals of pickup coils with a 101.31 MHz pilot signal. The RFFE output signals are undersampled and down-converted to base-band (no analogue mixer) by ADCs and DDCs (Direct Digital Downconverters) on the VBM. The DDCs send the digitised beam and pilot signal amplitudes to a Virtex2Pro FPGA on the VPC board. The FPGA calculates the beam positions at different averaging rates, checks interlock limits, and provides triggered storage of beam position waveforms. Furthermore, the FPGA performs automatic gain control of voltage-controlled amplifiers (VCAs) of RFFE and VBM. By continuous normalisation of beam to pilot signal, nonlinearities and temperature drifts of the electronics are eliminated. Compared to the old analogue BPM electronics, the new DBPMs offer an increased dynamic range (0.2 µA to 2 mA instead of 5 µA to 2 mA) and larger bandwidth (10 kHz instead of 10 Hz).

INTRODUCTION

The PSI high intensity proton accelerator chain consists of a 870 keV Cockcroft-Walton accelerator, a 72 MeV injector cyclotron, and the 590 MeV ring cyclotron that delivers its beam to two rotating-wheel targets for pion/muon production and to the neutron spallation source SINQ. Typical beam currents between 1.6 and 1.9 mA result in a CW beam power of >100 kW in the 72 MeV transfer line between injector and ring cyclotron and >1 MW in the 590 MeV transfer lines from ring cyclotron to targets and SINQ.

In contrast to the Swiss Light Source (SLS) that requires sub-micron orbit stability of its thin and flat electron beam, the beam of the proton accelerators has a much larger size and just needs to be kept well centred in the beam pipe in order to minimise beam losses, to avoid activation and damage of accelerator components due to the high beam power, and to achieve reproducible machine operating conditions and high availability. The required beam stability and thus BPM resolution is in the order of 1 mm which is about 1% of the beam pipe diameter. The beam position in the different transfer lines is usually automatically corrected at a rate of up to 10 Hz by high-level software using RF BPMs, with the correction rate being limited at about 10 Hz due to eddy current effects of the magnets. Therefore a BPM bandwidth of some 10 Hz is sufficient for normal machine operation.

The analogue CAMAC-based RF BPM electronics that was used so far fulfils these basic requirements, but has the drawback that beam currents can only be measured for currents from the nominal operation current of about 1.8 mA down to a lower limit of 5-10 µA. However, the beam positions have to be measured and corrected at lower currents in order to avoid high beam losses and activation of components during tuning or when the current is ramped from 0 to 1.8 mA after it was switched off due to an interlock condition. So far the orbit measurement and correction at currents below 5 µA were performed using time-consuming wire-scanner measurements and feed-forward lookup tables for magnet currents. The new DBPMs allow orbit measurement and fast automatic correction for currents down to 200 nA. Other reasons for the BPM upgrade were the request for a programmable bandwidth up to 10 kHz for machine studies, and the desired upgrade from CAMAC-based BPM electronics to the PSI standard VME64x that allows faster readout of large amounts of BPM data.

DBPM SYSTEM ARCHITECTURE

DBPM Hardware Architecture

Fig. 1 shows the hardware layout and Fig. 2 a photograph of the newly developed DBPM hardware that was designed in-house at PSI.

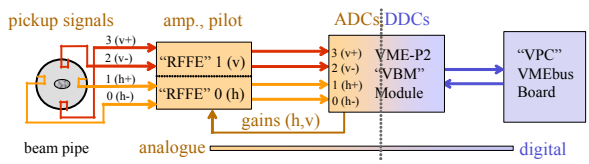

Figure 1: Schematic diagram of the DBPM hardware.

The DBPM consists of two RF front-end modules (RFFEs) [1] located close to the beam, a digital downconverter VMEbus backplane module (VBM) [1] that is plugged onto the VMEbus P2 backplane, and the PSI VME PMC Carrier board (VPC) [2,3] as a digital processing back-end.

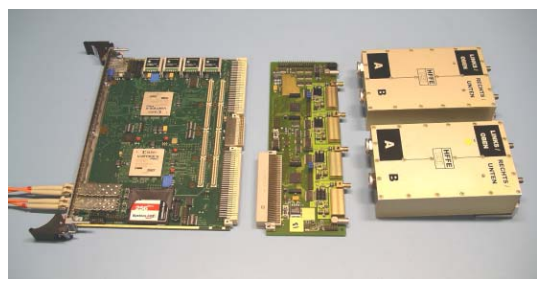

Figure 2: DBPM hardware. Left to right: VPC, VBM, RFFEs.

The two RFFEs of each BPM filter and amplify the 101.26 MHz signal (2nd RF harmonic) of four pickup coils in the beam pipe. Each RFFE also generates a 101.31 MHz pilot signal that is combined with each beam signal and sent via two triaxial cables per RFFE with some 10 m length to the VBM that filters and amplifies the four signals, samples them with four ADCs (23-46 MSa/s), and delivers them to two ISL5216 digital downconverter ICs (DDCs) on the VBM. Since each DDC has four independent channels, beam and pilot signals can be processed simultaneously. The two DDCs deliver the resulting four beam and four pilot signal amplitudes to the VPC across the VME-P2 connector via serial links, at a programmable rate of currently 50 kSa/s.

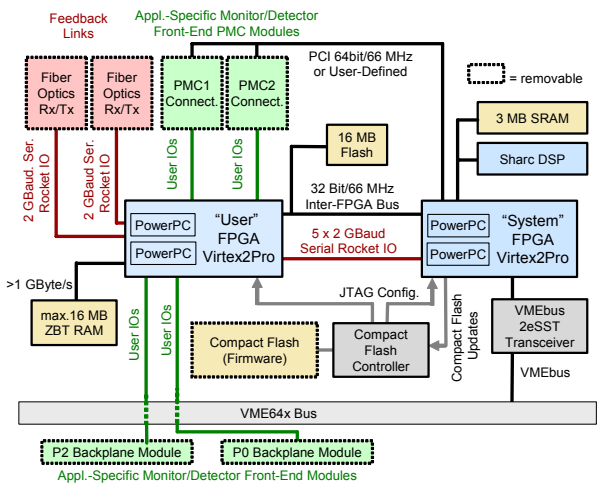

Figure 3: Block diagram of the VPC board hardware.

Fig. 3 shows the hardware layout of the VPC board. The DDCs of the VBM are connected to a Xilinx Virtex2Pro FPGA on the VPC board via the VME-P2 backplane connector. This so-called "User" FPGA contains DBPM-specific firmware and software. The Virtex2Pro contains two PowerPC processors, eight multi-gigabit serial links (two of which are connected to fibre optic transceivers), RAM, and clock synthesis logic on the silicon die. This allows the implementation of the complete digital section of a beam instrumentation system on a single chip (System-On-a-Chip, SOC). The second FPGA of the VPC board is called "System" FPGA and contains generic firmware which is common to all VPC board applications at PSI. Internal registers and RAM in the User FPGA as well as components connected to the User FPGA (e.g. DDCs or RAM) can be accessed via the VMEbus interface of the System FPGA using an Inter-FPGA bus that connects the two FPGAs.

DBPM Firmware and Software Architecture

Fig. 4 shows the layout of the User FPGA firmware for the DBPM. The green boxes of the diagram are application-specific VHDL modules (VBM interface), while the other boxes are generic modules that are also used for other VPC board applications. The first PowerPC (PPC1) initialises the internal registers and filters of the DDCs on the VBM using their parallel bus interface. The DDCs deliver beam and pilot signal amplitudes to the serial interface module of the firmware that stores the data in a cyclic dual-ported internal RAM. This RAM can also be accessed by PPC1 via on-chip peripheral bus (OPB) bridged to the processor local bus (PLB). PPC1 reads and calibrates the BPM data at 50 kSa/s, normalises the beam to the pilot signal either statically using fixed or dynamically using "live" pilot signal values, calculates beam positions, performs additional averaging, checks interlock levels, and provides oscilloscope-like trigger features with simultaneous storage of waveforms at four different averaging rates (50 kSa/s, 1 kSa/s, 50 Sa/s, 1 Sa/s) in the external ZBT RAM for VMEbus readout.

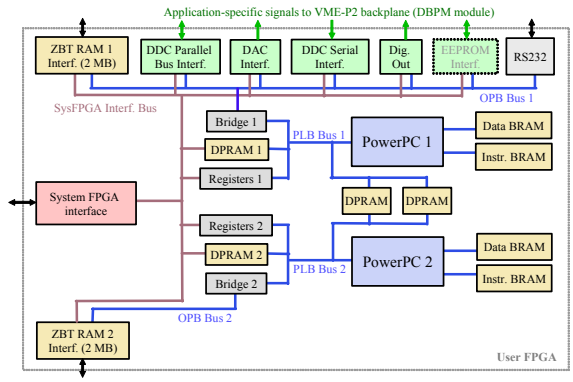

Figure 4: Schematic diagram of the VPC User FPGA firmware for the DBPM.

While PPC1 has a fixed software package that provides all features that are vital for the operation of the accelerator, PPC2 is available for any kind of data analysis, and its software may be changed often without risk for the operation of the accelerator.
Data transfer between each PPC and the System FPGA (and thus the VME-based control system) is done by internal dual-ported RAMs ("DPRAM1", "DPRAM2" in Fig. 4), by registers, and by the external ZBT RAMs. Dual-ported VHDL interface modules for ZBT RAMs and VBM allow full access to RAMs and VBM (e.g. of the DDCs) both by PPC1/PPC2 and VMEbus.

DBPM CHARACTERISTICS AND FIRST OPERATIONAL EXPERIENCE

PPC1 also performs automatic gain control (AGC): it reads the DDC input level detectors periodically and sets the gains of VBM and RFFE every 160 µs so that the ADC signals are kept at a user-defined level. The amplifier gains of RFFE and VBM (45 dB range each) are controlled by voltages generated by a 4-channel DAC on the VBM. Each RFFE also has an 18 dB attenuator that can be switched by PPC1, resulting in 108 dB overall gain. Fig. 5 shows the gain changes for increasing current. For decreasing current, the plot would look slightly different, since the 18 dB attenuator of the RFFE would switch at a lower signal level. This hysteresis avoids frequent on-off switching and related switching noise.

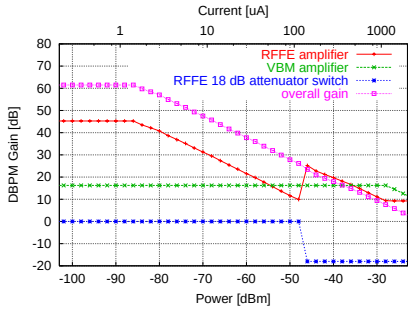

Figure 5: RFFE and VBM amplifier and RFFE attenuator gains as set by the AGC loop of the User FPGA.

After successful tests of the DBPM electronics in the lab and at the accelerator in autumn 2005, twelve of the old BPM electronics for the 72 MeV transfer line between injector and ring cyclotron were replaced in March 2006 by the new DBPMs which are since then in use during normal machine operation.

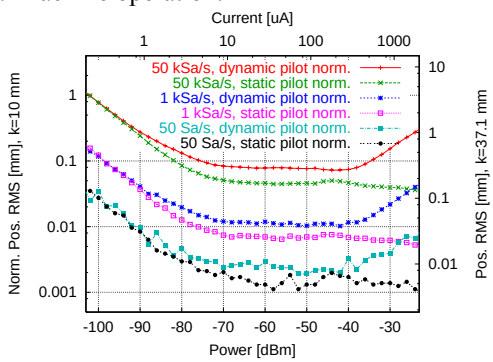

Figure 6: DBPM resolution for three different bandwidths, for continuous ("dynamic") normalisation of beam to pilot signal and for normalisation to constant ("static") pilot signal values.

Fig. 6 shows the resolution of the DBPM as a function of the beam current. The left axis is the position resolution for the usual scaling factor of k=10 mm (position=k*Δ/∑), the right axis is the resolution for the real scaling factor of the proton accelerator beam pipe (k=37.1 mm). There are two curves for each bandwidth: in "dynamic normalisation mode" the beam signals are continuously normalised to the "live" pilot signals, while in "static normalisation mode" the beam signals are normalised to fixed values, usually to pilot signal values taken once at a certain beam current. Since the pilot signal generator level can only be changed by 45 dB, the pilot signal level at the ADC decreases when the RF power is increased above -40 dBm, therefore its relative noise and thus the beam position noise for the dynamic normalisation mode also grows at high beam currents. However, in both normalisation modes the BPM resolution is still better than required for machine operation. As shown in Fig. 7, the beam current dependence is smaller in dynamic normalisation mode: except for a systematic drift at very low currents due to asymmetric pilot signal crosstalk in the RFFE, nonlinearities and asymmetries of the analogue signal chains are well compensated. Therefore this mode is presently the standard mode during machine operation. If necessary, a future firmware upgrade could eliminate the increased noise and systematic drift in the dynamic mode, e.g. by using lookup tables combined with a sufficiently averaged pilot signal instead of the full-bandwidth signal for normalisation. The DBPM position readings have also been verified by comparison with wire scanner measurements for different beam currents and positions.

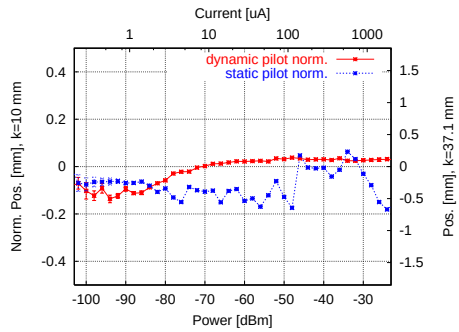

Figure 7: Beam current dependence of the position offset of one DBPM electronics, for dynamic and static normalisation of beam to pilot signals.

CONCLUSIONS AND OUTLOOK

A newly developed DBPM system for the PSI proton accelerator has been developed and successfully commissioned. A first set of 12 DBPMs has been installed and is now in use during normal machine operation. The remaining old analogue BPM systems will be replaced by DBPMs in the near future. The higher dynamic range allows automatic orbit correction and machine tuning at a beam current 30 dB lower than before, resulting in reduced radiation levels as well as safer and more comfortable machine operation. The increase of BPM bandwidth by three orders of magnitude allows machine studies that were not possible with the previous BPM system. The use of the VPC board as a standard digital back-end for PSI beam instrumentation and the resulting synergy effects significantly reduced the time for development and commissioning of the system.

REFERENCES

[1] P.A. Duperrex et al., "Latest Diagnostic Electronics Development for the PROSCAN Proton Accelerator", BIW'04, Knoxville, Tennessee, May 2004, AIP Conf. Proc. Vol. 732, p. 268.

[2] B. Keil et al., "The Generic VME PMC Carrier Board: A Common Digital Hardware Platform for Beam Diagnostics and Feedbacks at PSI", EPAC'04, Lucerne, Switzerland, July 2004, p. 2517.

[3] B. Keil et al., "The PSI VPC Board - First Applications of a Common Digital Back-End for Electron and Proton Beam Instrumentation at PSI", DIPAC'05, Lyon, France, June 2005, p. 14.