LOW LEVEL RF SYSTEM DEVELOPMENT FOR THE SUPERCONDUCTING RF CAVITY IN NSRRC

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Abstract

The present low level system in NSRRC is based on analogy feedback control scheme. It provides feedback regulation on amplitude, phase, and resonant frequency of the superconducting RF cavity. In order to address the required flexibility and improve diagnostic of the RF control system, a new digital low-level RF system based on Field Programmable Gate Array (FPGA) is proposed to be developed in house. The status of current analogy low level RF system and the specifications of the new digital FPGA based low level RF system are reported herein.

UPGRADE OF PRESENT LLRF SYSTEM

The low-level RF control system for the CESR-B type superconducting RF cavity in NSRRC is based on analogy feedback loops. It consists of 4 independent feedback control loops: gap voltage control, cavity phase control, klystron phase control and cavity frequency (tuner) control. These control loops ensure the required stability conditions for the SRF cavity operation. Figure 1 shows the simplified block diagram of this system.

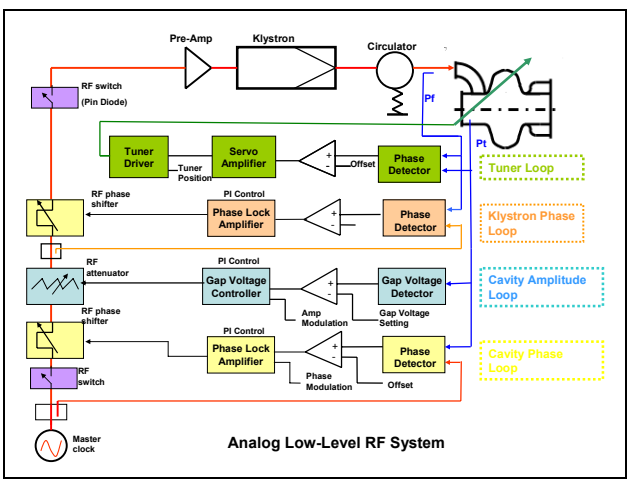

Figure 1: Functional block diagram of the analog low level RF control system.

The gap voltage control loop keeps the gap voltage inside the cavity constant. The cavity phase compensation loop keeps the phase of the cavity field constant in respect to the referred input phase of the master clock. The cavity frequency tuning loop measures the phase difference between the forward RF power and the cavity filed to determine and promise the resonant condition of the SRF cavity. The phase error signal is processed by a servo amplifier and then applied through the tuner driver to the stepping motor of the tuner.

Recently an additional klystron phase feedback loop was installed in the RF low level system, which effectively reduces the klystron RF phase variation.

A new phase detector module, which incorporates with the Analog Devices AD8302, has been assembled. And all three sample type phase detector modules in analog LLRF system has been replaced by the new module. The phase detector using AD8302 has superior amplitude rejection, 60dB dynamic range, better temperature stability and faster response time than the original phase detector. The block diagram and designed performance of the new phase detector NIM module are shown in Figure 2.

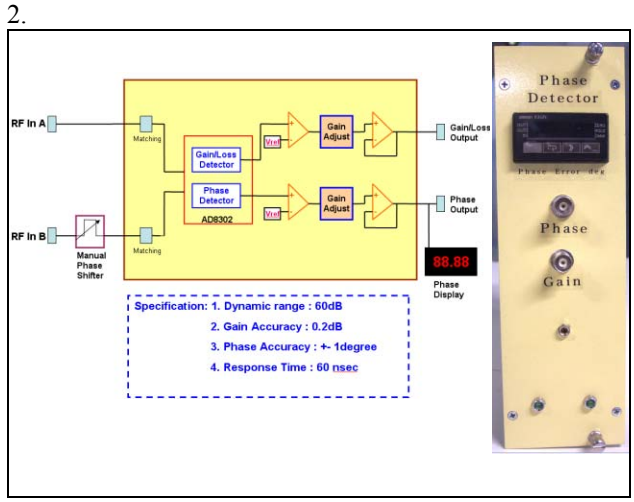

Figure 2: Phase Detector NIM module

The achieved amplitude and phase error of LLRF system are around $\pm$ 1% and $\pm 2^{\circ}$ respectively, mainly perturbed by microphonics.

DIGITAL LOW LEVEL SYSTEM

The advance of FPGA, digital signal processor and high performance digital data acquisition in the last few years make it possible to build a digital low level RF control system design. The advantages of the digital system over analog one include flexibility and powerful computation ability provided by FPGA device [1-6]. A new FPGA based digital low level RF system is proposed to serve for the future Taiwan Photon Source.

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Besides, accelerating electric field stability of ± 1% in amplitude and ±1° in phase is required for the future SRF system. The digital RF feedback control system with FPGA and DSP embedded processor is adopted in order to achieve these requirements and flexibility of the feedback control algorithm implementation.

Shown in Figure 3 is the scheme of the proposed of digital RF control system. Mainly this digital LLRF system controls in-phase(I) and quadrature(Q) components of the cavity filed. The front detectors for the cavity field, forward wave, and reflected wave are implemented as digital I/Q detector. The RF signals are converted to an IF frequency of 15 MHz by mixer and analog-to-digital converter (ADC) sampled at a rate of 60MHz. The output of the ADC is fed into an FPGA, which separates I/Q components of the data string and applies adequate sign swap by digital I/Q demodulator, i.e., two subsequent data points describe I and Q of the cavity field. The primary function of digital demodulator is to down convert the digital IF signal to the baseband and to filter the out-of-band spectrum.

The I and Q components describe the cavity filed vector and are multiplied by a 2x2 rotation matrices to correct the phase offsets and to calibrate the gradients of the cavity probe signals. Then the vector streams are filtered by FIR low pass filters. Finally the implemented feedback algorithms applied the proportional gain and integration gain to the regulating error.

The outputs of FPGA are sent to two independent D/A converters, and the outputs of the D/A converters are directed to the vector modulator. The vector modulator modifies the phase and the amplitude of the master reference clock carrier frequency to generate the desired RF signal for the klystron based on I/Q vector inputs from the digital LLRF.

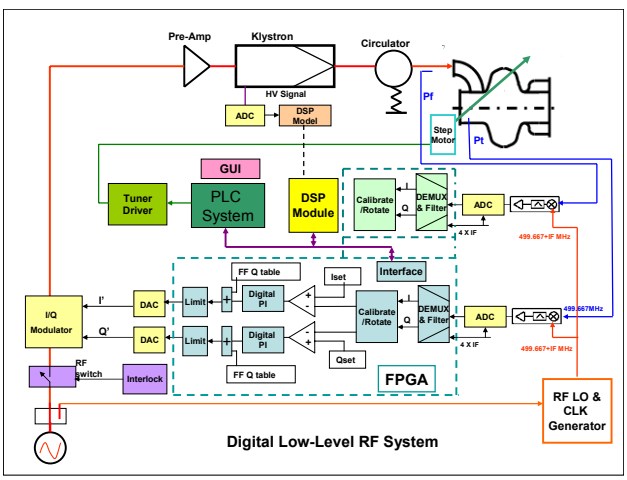

Figure 3: Function blocks of digital low level RF system.

Local Oscillator and CLK generate module

Residual phase noise from local oscillator and converter clock can degrade the LLRF system performance. Then low phase noise, good frequency stability over operation temperature ranges of both local oscillator source and clock are essential for digital low level system. The local oscillator and clock distribution module has two phase lock loops to generate low level signals. Thus the loop can lock on the master reference clock of low level system. Figure 4 shows the schematic of the LO and clock generator module.

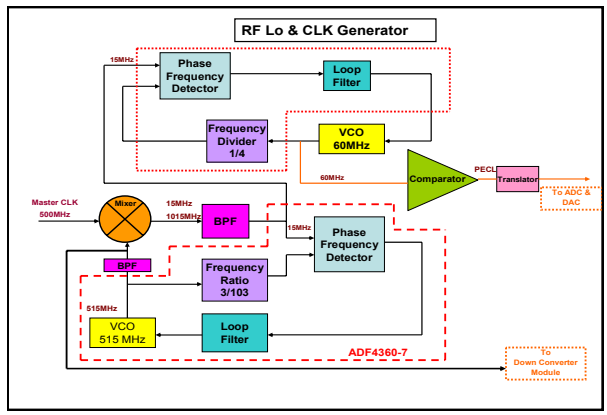

Figure 4: Block diagram of RF LO & Clock generator.

Data Converter and FPGA Board

To realize the vector sum control functions, main RF control functions will be developed and implemented into the FPGA on the Xilinx XtremeDSP Development board [7]. The XtremeDSP board is a commercial product and show in Figure 5. It consist of two independent ADC channels in the analog signal processing, large one FPGA chip in the fast digital signal processing, two independent DAC channels in the reconstruction analog waveform and large static RAM for the acquisition data.

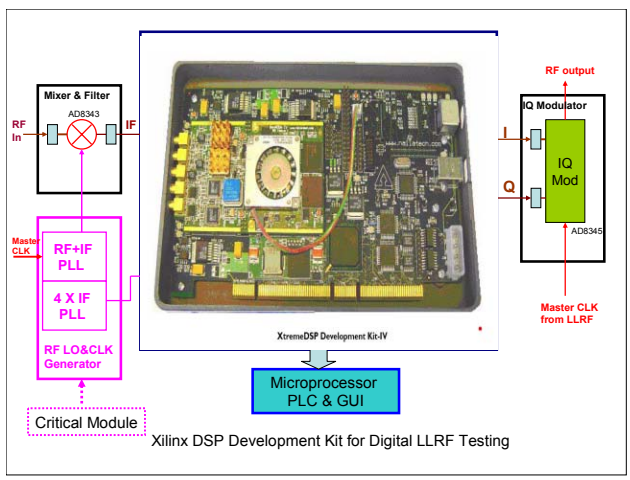

Figure 5: Xilinx DSP development Kit for Digital LLRF System testing.

The ADC is based on AD6645, a high speed, high performance, monolithic 14-bit analogy-to-digital converter. All necessary functions, including track and hold and reference, are integrated on this chip to provide a complete conversion solution. The DAC is based on AD9772, a 14-bit over-sampling digital-to-analog

converter and optimized for the baseband or IF waveform reconstruction application.

The vector controller of FPGA device will be implemented by VHDL description language in Xilinx ISE development environment. Figure 6 shows the simplified function blocks of vector controller in FPGA. There are several issues to be considered in the real implementation in FPGA to achieve the goal of a real time. One is to reduce the hardware latency. Hardware latency is an important key to successful implementation of a digital feedback control. In order to reduce hardware latency, a well planned pipeline VHDL design will enable the signal go through the vector control path in minimum clock cycles. Another issue is the finite word length effects. Practically FPGA designs are limited by finite precision signal processing using fixed-point arithmetic, to avoid the complexity of floating point hardware. In mapping the vector control function onto FPGA, the dynamic range and desired precision of input, intermediate and output signals, must be determined in advance.

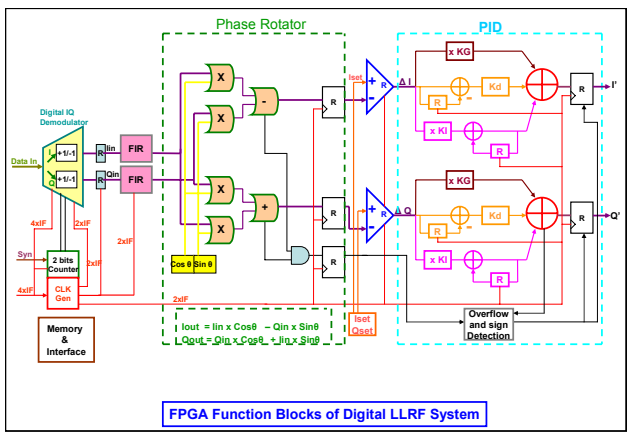

Figure 6: FPGA function blocks of digital LLRF system

DSP Module

The Digital Signal Processor (DSP) has three primary functions. 1) It calculates the tuning phase error of the cavity use the CORDIC arithmetic. The IQ data transfer between DSP module and FPGA module via high speed digital interface. 2) DSP regulates the cavity resonance frequency use proportional-integral-derivative (PID) control.

Programmable Logic Controller

Programmable Logic Controller provides system diagnosis, interlock protection and state machine operation control logic. We will adopt Siemens S7-300 type controller and associated hardware to measure analog and digital interlock inputs, and to process input logic.

CONCLUSIONS

The overall functions of proposed digital low level system are introduced in this article. The construction of digital LLRF system is proceeding. First integration testing with the front end, LO&CLK module, the FPGA board, and IQ modulator module for the vector sum control are expected to launch in middle of 2007. More efforts on phase lock loop and hardware design are foreseen.

ACKNOWLEDGEMENT

Dr. D. Teytelman in SLAC and Dr. S. Belomestnykh in Cornell University are deeply appreciated for their valuable recommendation on RF feedback systems.

REFERENCES

[1] M. Liepe, S. Belomestnykh, et al, “New Digital Control system for CESR-c and the Cornell ERL”, Proceedings of the 2003 Particle Accelerator Conferences, Portland.

[2] S.N. Simrock, et al., “Digital Low-level RF Controls for Future Superconducting Linear Colliders”, Proceedings of PAC 2005, Knoxville, Tennessee

[3] S.N. Simrock. “State of The Art in RF Control”, Proceedings of Linac 2004, Lubeck, Germany.

[4] S. Michizono et al., “Digital RF control system for 400-MeV Proton Linac of JAERI/KEK Joint Project”, Proceedings of LINAC2002, Gyeogju, Korea.

[5] S. Michizono et al., “Digital Feedback System for J-PARC Linac RF Source”, Proceedings of LINAC2004, Lubeck, Germany.

[6] Hengjie Ma, Mark Champion et al., “Low-level RF Control of Spallation Neutron Source: System and characterization”, Physical Review Special Topics-Accelerators and Beams 9,032001 (2006)

[7] Xilinx Homepage, http://www.xilinx.com