DIAMOND BOOSTER MAGNET POWER CONVERTERS

J. A. Dobbing, C. A. Abraham, R. J. Rushton (Diamond Light Source, Oxfordshire, U.K),
F. Cagnolati, G. Facchini, M. Pretelli (OCEM SpA, Bologna, Italy),
C. Rossi (University of Bologna, Italy)

Abstract

The design, performance and early operation of the Diamond Booster Power Converters are described. The design performance has generally been achieved and early operation of the Booster is encouraging.

INTRODUCTION

The Diamond Booster power converters, PC's consist of a single dipole supply, two quadrupole supplies, two sextupole supplies and 44 steerer supplies. The Booster itself operates at 5 Hz to accelerate the electron beam from 100 MeV to 3 GeV. To achieve this acceleration the PC's are required to produce an off-set sine wave current with high repeatability at the 5 Hz operating frequency.

To avoid disturbance on the ac distribution network the dipole and quadrupole power converters were designed to present a constant load despite having high circulating energy: 2 MVA in the case of the dipole.

As with all the Diamond power converters, redundancy was introduced wherever this was economically feasible. Plug-in modules are used to simplify and speed up repairs. Component standardisation and de-rating across all power converters was an additional design goal. In particular, all the Diamond power converters are controlled by the same ADC cards and digital controllers, manufactured under licence from the Paul Scherrer Institute, PSI.

BOOSTER DIPOLE POWER CONVERTER

The Booster dipole PC is rated at a peak current and voltage of 1000A and 2000V respectively. The power circuit consists of four series connected units as shown in Fig. 1. Three units are sufficient to produce the required output. The fourth provides redundancy. Any unit can be taken out of circuit by means of a bypass switch.

Each unit is made up of a boost circuit and a two quadrant output regulator that produces the required off-set sine wave current. The boost circuit regulates the voltage on the main energy storage capacitor and is controlled to draw constant power from the ac network. The output regulators are equipped with output filters. These both reduce the output ripple and limit surge currents through the stray capacitance of modules floating at high voltage.

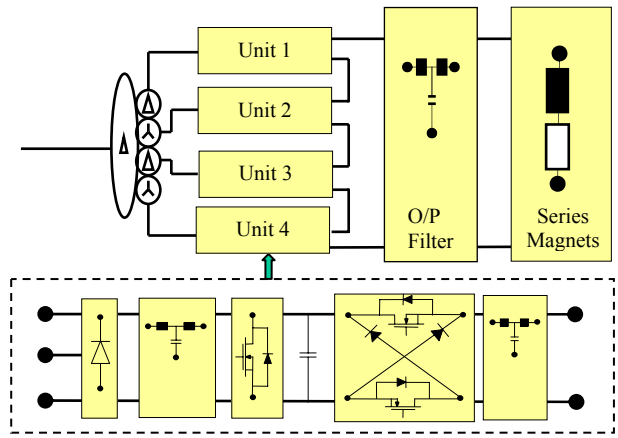

Figure 1: Booster dipole power circuit.

The units operate at 4 kHz switching frequency. They are phase displaced to give an effective operating frequency of 16 kHz. There is a final output filter to further reduce ripple currents. This is centre earthed so that the power supply operates symmetrically around ground potential.

The PC is air cooled from a dedicated air handling unit. This supplies temperature controlled air at 16 ^{o}C by means of an air/chilled water heat exchanger.

Power semi-conductors are mounted in "plug-in" modules. These weigh 100 kg due to the large heatsinks and require special handling gear.

Control Architecture

Each of the four units is controlled by a digital controller and ADC card. A further controller and ADC card regulates the output current and controls the input soft start circuit. The five controllers are fitted in a standard 3U sub-rack. Optical outputs and analogue signal processing is performed in another 3U sub-rack. These are linked by a 6U backplane. This also provides communication between controllers through a data bus.

The unit controllers control the boost circuits and provide interlocks and protection for the units. The master controller houses the control loop for the output current. It distributes the modulation index for the unit output regulators over the data bus to the unit controllers. These generate the Pulse Width Modulation, PWM, signals for the unit output regulators.

Control Algorithms

The third order state space equations for the output current controller are:-

$$x(t_n) = A.[B.u(t_n) + x(t_{n-1})]$$
$$y(t_n) = C.x(t_n) + D.u(t_n)$$

u(t) = control error (difference between I_{ref} and I_{actual})
y(t) = modulation index (-0.98 < y(t) < 0.98).

This has the Bode plot shown in Fig. 2. As can be seen this is highly resonant at the operating frequency of 5 Hz.

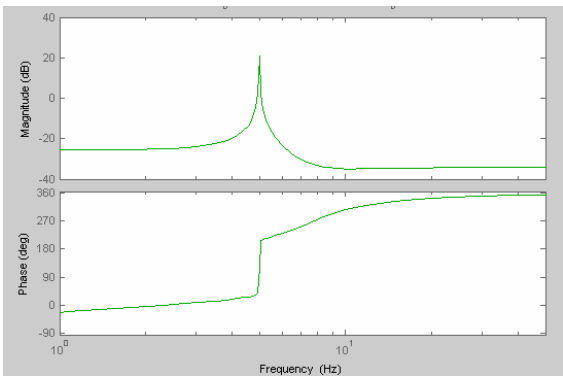

Figure 2: Bode plot of the output regulator controller.

The unit boost controllers consist of an inner current control loop and an outer loop that controls the peak voltage on the main energy storage capacitor bank, as shown in Fig. 3.

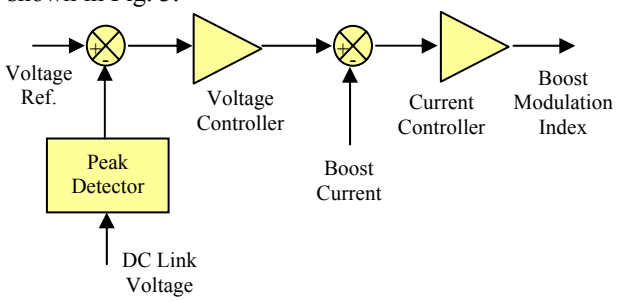

Figure 3: Boost controller block diagram.

Performance

As can be seen in Fig. 4, the output current tracks the reference after the first few cycles. The DC link voltage reaches steady state condition after about 16 cycles. The rectifier current is also constant after the initial transient.

The pulse to pulse variation is within the 50 ppm specified, when operating at 5 Hz. The control error during the accelerating part of the cycle is less than ±600 ppm, as shown in Fig. 5. This is greater than the 50 ppm specified and the ±100 ppm predicted by the model. The increased error is attributed to non-linear effects not captured by the model. Since the error is repeatable it can be compensated for by adjusting the reference waveform, if necessary. The tracking between dipole and quadrupole PC's is within the generally accepted limit of 1 in 10^3, even without such compensation.

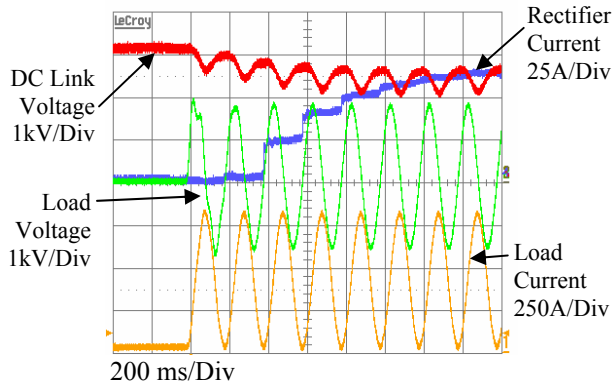

Figure 4: First few cycles after turn on.

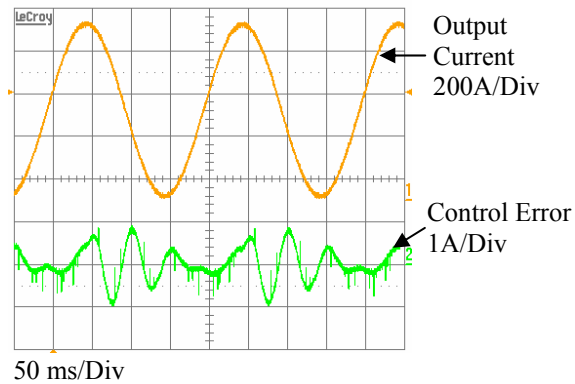

Figure 5: Output current and control error.

BOOSTER QUADRUPOLE POWER CONVERTERS

The quadrupole PC's consists of three parallel modules, one of which is redundant and can be isolated. Each module is fed from its own unregulated ac/dc converter and boost circuit to control the voltage on the associated energy storage capacitor. The output regulators are two quadrant H bridges, with IGBT's switching at 7 kHz.

Like the dipole PC the quadrupole PC is air cooled, with temperature controlled air provided from an under floor supply. Power semi-conductors are also mounted in "plug-in" modules.

As with the dipole, the quadrupole PC require five controllers and five ADC cards: one for each of the three modules and two to control the outputs. The control algorithms have the added requirement of maintaining the current sharing between the parallel modules.

The performance of the quadruple PC's is similar to that of the dipole.

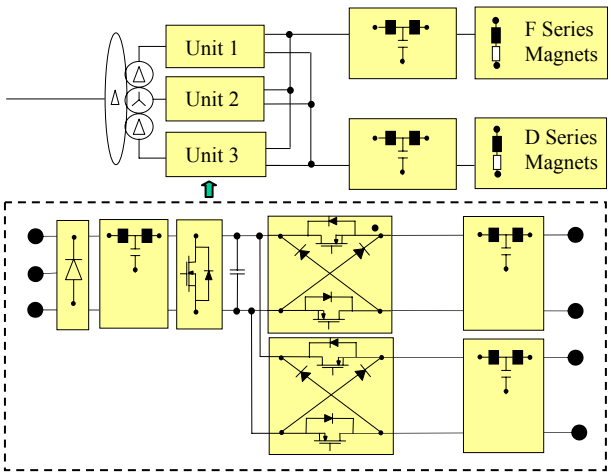

Figure 6: Booster quadrupole power circuit.

BOOSTER SEXTUPOLE POWER CONVERTERS

The two Sextupole PC's are based on standard four quadrant H bridges, with MOSFETS switching at 100 kHz. The output is filtered with a two pole filter. Ac/dc conversion is provided by commercial PULS 24V supplies in a redundant configuration. The voltage on the main energy storage capacitor is controlled to 72 volts by a boost circuit. The PC outputs are each rated at 55V 20 A peak. The controller uses the standard PSI control algorithms [1].

BOOSTER STEERER POWER CONVERTERS

The steerer PC's are of the same design as those on the Storage Ring. These are described in another paper at this conference [2]. In the Booster they are used at a fixed value, whereas in the Storage Ring they are used with a preset off-set and as part of a beam position feedback system.

INITIAL BOOSTER OPERATING EXPERIENCE

Initial operation of the Booster was hampered by the lack of a water cooling system to cool the magnets. This resulted in the maximum energy of the beam being limited to 700MeV. After five months operation the efficiency at this energy reached 60-80%. Efficiency is defined as the charge extracted divided by the charge injected into the Booster. Currents of up to 2 mA are routinely accelerated.

First turn was achieved without the steerer magnets being powered, indicating that the ring is well aligned.

In early June a temporary water cooling system was installed for the magnets. The power converters were then rapidly run up to the level required for 3GeV operation, which was achieved after a few days operation.

Operation at 3GeV is not as stable as at 700MeV. The problem has been traced to the fact that the 5 Hz operating frequency is derived from the mains and varies by up to 1%. This is a significant amount for the highly tuned dipole PC controller.

The locking of the 5 Hz to the mains is done for the benefit of the Linac. To achieve the required reproducibility in the Booster the Dipole PC PWM will be phase locked to the mains. This is relatively easy as the modules are already phase locked to one another.

CONCLUSIONS

The Diamond Booster has operated routinely at 700MeV for five months. Stable operation at 3GeV has yet to be achieved due to variations in the mains frequency to which the 5 Hz Booster cycle is locked.

The power supplies were commissioned very rapidly thanks to the extensive factory testing and modelling. It was not necessary to adjust the control loops significantly from their factory settings.

ACKNOWLEDGEMENTS

The authors would like to thank the staff of the Paul Scherrer Institute for their help in developing the controller software.

REFERENCES

[1] F. Jenni, L. Tanner, "Digital Control for Highest Precision Accelerator Power Supplies", PAC'01, Chicago, June 2001, p. 3681.

[2] R. Rushton, et al. "Diamond Storage Ring Magnet Power Converters", EPAC'06, Edinburgh, June 2006.