A HIGH ACCURACY PROGRAMMABLE TIMING SYSTEM FOR THE LINAC OF THE CLIO FREE ELECTRON LASER.

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In order to allow a very good repeatability of the operation of the linac of CLIO, a low jitter triggering electronic has been built. This electronic is based on the use of programmable preset counters synchronised by a clock derived from the pilot of the RF. The circuits are implemented on Europe boards and programmed with a G 64 bus. A basic circuit synchronised with a 31.25 MHz clock allows the programmation of triggering signals in a 2 ms range by steps of 32 ns with less than 50 ps jitter. For more stringent applications an additional circuit synchronized on a 500 MHz clock is used. This circuit is built using a 500 MHz varicap phase shifter, a HP HDMP 2001 retiming circuit and an Analog Device AD 9500 programmable delay generator. It allows the generation of 500 ps risetime pulses with less than 10 ps jitter and 10 ps repeatability with respect with the linac's beam, inside the same 2 ms range.

Introduction.

CLIO is a free electron laser driven by a 60 MeV linac.The linacs RF frequency is 2998.55 MHz ; the electron bunches will be produced in an injector composed of a thermionic gun followed by two bunching RF structures with 499.76 and 2998.55 MHz RF frequencies. The linac will be operated in 12 µs long RF pulses with a repetition rate of 50, 25, 12.5, 6.25 Hz. Inside this 12 µs pulse length the spacing between the electron bunches will be n x 2 ηs (n = 1 to 16) and the bunches length about 15 ps : the thermionic gun will provide 1 ηs bunches and the subharmonic buncher will compress this length to less than 180° of phase of the 2998.55 MHz bunchers RF frequency : this length will be reduced down to 15 ps in the S band buncher. The operation of the laser will demand a very good stability of the operating parameters of the RF. In order to contribute to this stability the timing system of the pulsed element of the machine and their associated measurement electronics has been designed in order to avoid any variation of the operating parameters due to jitter or long time drift. The timing system has also been designed in order to be flexibly controlled by the G 64 bus used for the control CLIO.

32 ηs steps G 64 programmable pulse generators.

Most of the timing requirements of CLIO components can be met with a resolution of about 50 ns for the delay and width of the pulses. These requirements are due the risetime of the pulsed RF generators, filling time of the RF structures, bandwidth of the electronics etc. The most used approach to build a programmable timing pulse generator with low jitter and good accuracy is to use programmable synchronous preset counters circuits with high stability clock and reset signals. We wanted to implement this circuits on a G 64 format board using G 64 standard power supplies.The fastest preset counters IC compatible with this approach are the 74 AS serie 74 ALS 867 8 bits counters with a maximum clock frequency of 50 MHz. The subharmonic frequency of the 499.76 MHz immediatly inferior is 31.235 MHz (32 ηs period). With a 16 bits programmation of the delay and width of the pulses and this clock frequency we cover a 2.097 ms range in 32 ηs steps for both settings which is more than enough for our applications.
In addition to the programmation of the delay and length of the pulses it is also possible to choose the rate of the generation of the pulse (50, 25, 12.5, 6.25 Hz) and single shot and to use an internal 31.235 MHz clock for stand alone operation of the module. One connector of the bus can be used to program one or two pulse generators. These G 64 modules will be implemented in the different G 64 crates controlling the CLIO components and will be synchronized by the same reset and clock signals.

Generation and distribution of the reset and clock signal

The 31.235 MHz clock signal is generated with ECL D flip flops dividing the frequency of the 499.76 MHz subharmonic bunchers RF pilot frequency. The 499.76 MHz pilot is a state of the art transistor cavity oscillator phase locked on an oven temperature stabilized quartz reference at 99.951 MHz. The stability of the reference is better than 5.10^{-9} per day. Both the phase locked source and the quartz reference are commercially available components.The repetition rate of the operation of CLIO is the 50 Hz AC frequency and its subharmonics. The timing reset pulse is generated a quarter of period after the positive zero crossing of the AC main voltage. The amplitude of the next positive half period of the 31.235 MHz following this reset signal is doubled according to the following time diagram.

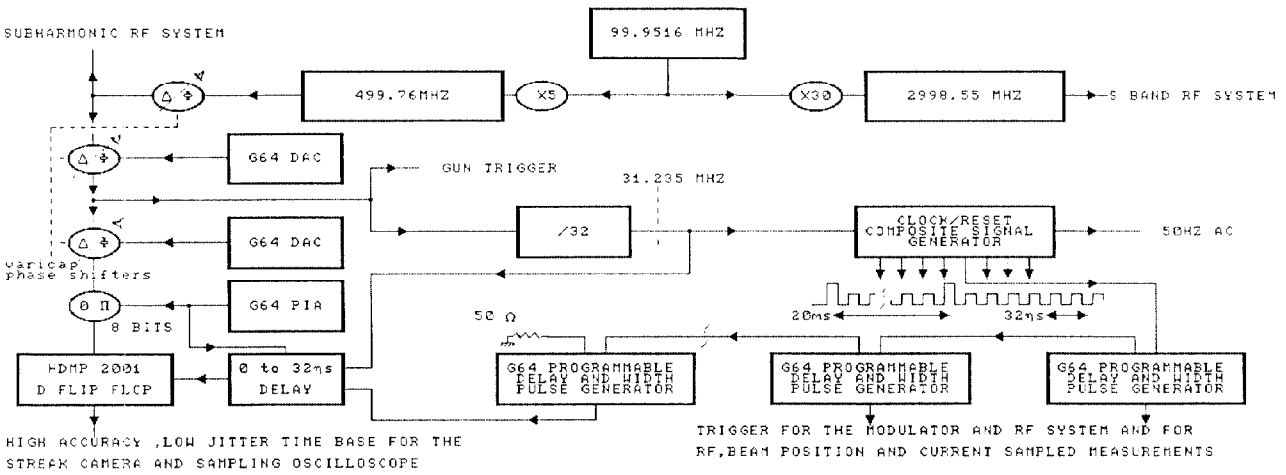

Figure 1 : Schematic diagram of the timing system of CLIO

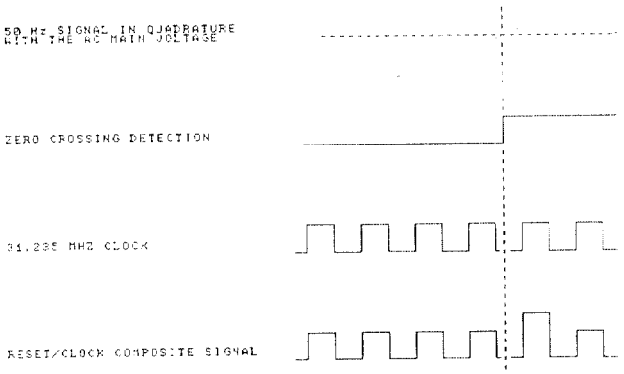

Figure 2 : timing diagram of the clock/reset composite signal generation

This signal is amplified and multiplexed in order to be available at eight outputs with an amplitude of 1 volt on 50 Ω (2 volts for the reset pulse). In this way the preset and the clock signals for the G 64 modules are available on the same cable. Up to five G 64 modules can be daisy chained along a cable delivering the signal on a distance much longer than the CLIO dimensions.

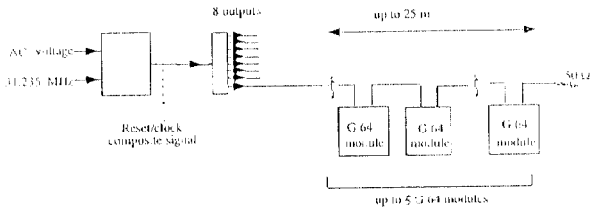

Figure 3: Interconnection of the 32 ns steps timing system components

High accuracy timing circuit.

For some application we need a time base with a more precise setting and a lower jitter. We will use a streak camera, a fast digitizer and a sampling oscilloscope for measurements of the bunched beams micropulses parameters (length, parasite satellites bunches, etc) A convenient and flexible approach to trigger these instruments would be to use a time base synchronized on the RF signal and programmable with a good resetability. The most stringent application is the triggering of the streak camera which demands a jitter inferior to 10 ps (our streak camera trigger input signal must be a 4 volts 1 ηs rise time, 30 ηs long signal).

Principle of the circuit.

This high resolution programmable delay signal is generated with a D flip flop circuit using the 499.76 MHz signal as a clock. To set precisely the delay of the output pulse we change the phase of the clock signal using electronic phase shifters and we select the right period of the clock using the D input for the long range delay setting according to the figure 4. The varicap phase shifter does not introduce any additional jitter (providing the control voltage is not noisy) and is easy to control with a DAC. Using the classical circuit given below we get a 0 to 200° range of phase shift. An additional phase inverter made of another 3 dB hybrid terminated by an ASGA switch increases the phase shift range of 180° (figure 5 photograph) giving a 2 ηs range for the fine setting of the delay.

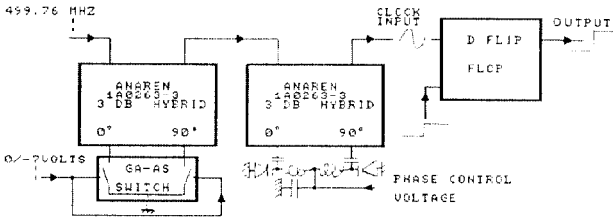

Figure 4 : D flip flop and phase shifters arrangement

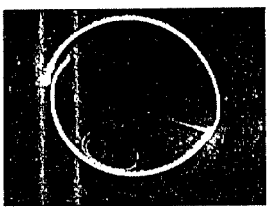

Figure 5 : Phase shifters range measurement (amplitude/phase polar display)

Choice and evaluation of the D flip flop.

In order to have a reliable operation at 499.76 MHz and a low rise time of the output we have decided to use a circuit able to operate with a clock frequency of 1.5 GHz. Our two main concerns were the stability of the propagation delay between the clock input and the output and the insensitivity of this delay to the position (and jitter)of the D input signal leading edge. The circuit that we have tested is an HDMP 2001 developed for the synchronisation of high rate digital communication data links.

Clock input to output delay measurement.

The delay jitter was measured using a jitter free 31.235 MHz signal, subharmonic of the 499.76 MHz clock as the D input signal. The 31.235 MHz signal generated at the output was used as an external trigger for a sampling oscilloscope and the 2998.55 MHz 6th harmonic of the clock signal (for better sensitivity) visualised on the oscilloscope as shown on figure 6.

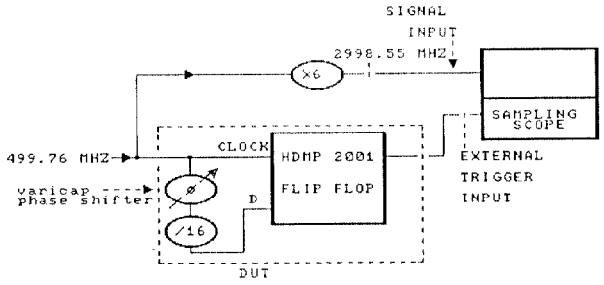

Figure 6 : Delay and jitter measurement

With the right D input phase shifter setting no measurable jitter was observed. The drift of the output signal for temperature variation, measured on the same set up was found to be less than 10ps for a 50° variation of temperature.

We have also measured the variation of the clock input to output delay with respect to the D input signal position (by varying the setting of the phase shifter). The result of the measurements are given on the curve below.

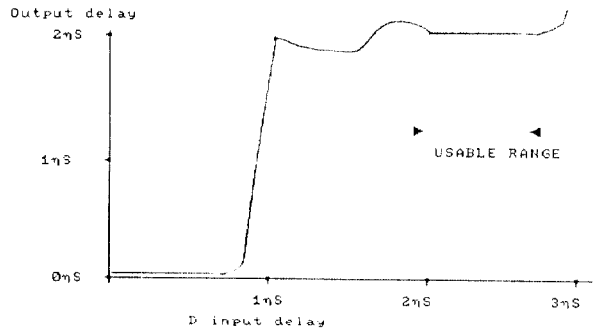

Figure 7 : HDMP 2001 clock rising edge to output delay versus D input to clock rising edge delay

The important point for our application is that there is a 700 ps range where the output pulse is insensitive to small jitters at the D input.

Generation of th D input signal.

To fill the gap between this 2 ηs range and the 32 ηs steps width of the G 64 pulse generator described above we use an AD 9500 integrated circuit made by Analog Device [2] This circuit allow the programmation with 8 bits accuracy of its output pulse with respect to a trigger pulse. The range of the delay programmation is given by the choice of the values of a set of external resistor and capacitor for our application this range is of course 32 ηs . The jitter of the output pulse for this delay range is about 100 ps. The input and output levels are ECL and the output rise time is 2 ηs For our application the circuit is triggered by one of our G 64 pulse generator and the output signal is used to validate the D input of the D flip flop clocked by the 499.76 MHz.

Operation of our circuit.

The complete schematic diagram of our circuit is given below.

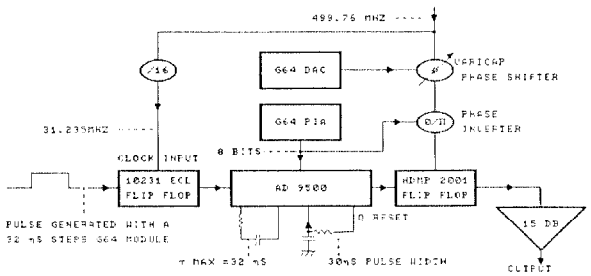

Figure : 8 Schematic diagram of the high accuracy time base circuit

The 31.235 MHz subharmonic of the 499.76 MHz is used to resynchronize the leading edge of the pulse generated by the G 64 module. This frequency is used instead of the 499.76 MHz because of the relatively high 20 ηs rise time of the output of the G 64 module. The output signal of the 10131 ECL flip flop has a 5 ηs rise time with a constant position with respect to the 499.76 MHz clock of the HDMP 2001. This signal triggers the AD 9500. The five most significant bits of the AD 9500 programmation inputs are set in order to select the proper 2 ηs period inside the 32 ηs step of the G 64 pulse generator. The fine setting of the delay is then obtained by the programmation of the varicap phase shifter and 0/π phase inverter. In order to generate an output pulse with the lowest jitter we program the three least significant bits of the AD 9500 programmation inputs to have the proper delay between the signals leading edges at the clock and D inputs of the HDMP 2001.
The value of the programmation bits of the G 64 module. of the AD 9500 circuit and of the DAC driving the varicap phase shifter for a given delay are calculated by a program writen in C and running on the local controller of the G 64 bus.

Test results.

The delay of the signal generated by our circuit can be continuously varied in a 2 ηs range with respect to a time reference. The accuracy of the setting is function of the circuit and of the reference signal : we have measured the contribution of our circuit to the jitter of the CLIO time base using again the set up of the figure 6. Figures 9a and 9b show the 6th harmonic of the 499.76 clock measured on a Tektronix 11800 sampling scope externaly triggered on figure 9a by a jitter free signal and on figure 9b by the output of our time base : the additional jitter due to our circuit on figure 9b is less than 10ps

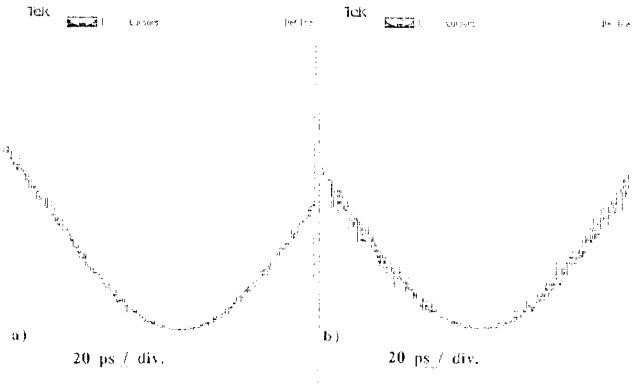

Figure 9 : 6th harmonic of the 499.76 MHz clock visualised with a sampling scope triggered by a jitter free signal (a) and by our high accuracy timing circuit (b).

Aknowledgements :

The authors thank M. BERNARD for his contribution to the writing of the control code for G 64 modules and to the improvement of the fast electronic circuit and J.C. JUMEL for his help in the development of the clock generator.

References :

[1] First beam of the CLIO linac, J.C. BOURDON, LAL, this conference.

[2] Hewlett Packard : Decision circuit, HDMP 2001, technical data, september 1988.

[3] Analog Devices : AD 9500, digitally programmable generator, Analog products data book, 1989.