

# BINARY RF PULSE COMPRESSION EXPERIMENT AT SLAC\*

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Using rf pulse compression it will be possible to boost the 50- to 100-MW output expected from high-power microwave tubes operating in the 10- to 20-GHz frequency range, to the 300- to 1000-MW level required by the next generation of high-gradient linacs for linear colliders. A high-power X-band three-stage binary rf pulse compressor has been implemented and operated at the Stanford Linear Accelerator Center (SLAC). In each of three successive stages, the rf pulse-length is compressed by half, and the peak power is approximately doubled. The experimental results presented here have been obtained at low-power (1-kW) and high-power (15-MW) input levels in initial testing with a TWT and a klystron. Rf pulses initially 770 nsec long have been compressed to 60 nsec. Peak power gains of 1.8 per stage, and 5.5 for three stages, have been measured. This corresponds to a peak power compression efficiency of about 90% per stage, or about 70% for three stages, consistent with the individual component losses.

The principle of operation of a binary pulse compressor (BPC) is described in detail elsewhere.<sup>1</sup> A schematic of a two-stage BPC is shown in Figure 1. It works as follows: Two rf inputs are phase-coded into four time-bins with phases 0 or  $\pi$ , denoted by "+" or "-", respectively. A 3-dB coupler or "hybrid," H1 in Figure 1, combines the pulse trains to produce two outputs, each at twice the peak power and half the pulse-length, properly phase-coded for the next stage. The compressed pulses are sequential, not coincident. They are made coincident at hybrid H2 by delay D1. In the second stage, H2 again doubles the peak power and halves the pulse-length. The two compressed pulses again are made coincident by delay D2 (half as long as D1), so they may be used to energize two accelerator sections of a linac. A three-stage system requires another hybrid and delay line, and more complex phase-coding.

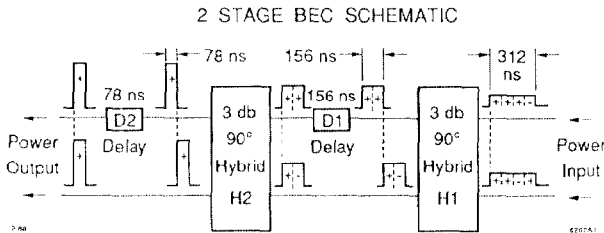


Figure 1. Pulse schematic of a two-stage binary pulse compressor. (Note that the pulses travel from right to left.)

Experiments with a low-power (non-vacuum) two-stage X-band BPC at SLAC were reported one year ago.<sup>2</sup> We recently have implemented and operated at SLAC a high-power (high-vacuum) three-stage X-band BPC. First results from the high-power three-stage BPC experiment are reported here.

In reality, the BPC peak power gain per stage is less than two because of losses in the delay-lines, the hybrids, and other components. For practical application to linac rf systems, the losses must be sufficiently small to produce reasonable efficiencies. Therefore, we have chosen to work with overmoded 2.81-inch-

Therefore, we have chosen to work with overmoded 2.81-inch-diameter circular waveguide (WC281) for the delay-lines, and standard rectangular X-band waveguide (WR90) for the non-delayed connections. Our hybrids are designed to couple the TE<sub>01</sub> circular mode in 1.84-inch-diameter waveguide (WC184) to the fundamental mode in WR90. Trombone bends of 180° are necessary to place the start and end of each delay-line in close physical proximity. All our delay-line bends are fabricated from corrugated 1.84-inch-diameter circular guide. Linear tapers are used for transitions between WC281 and WC184. We use mode transducers to convert from the fundamental (TE<sub>10</sub>) mode in rectangular guide to the circular TE<sub>01</sub> mode in circular guide.

The insertion losses of the individual components have been measured separately, except for the circular waveguide loss which was calculated. The hybrid losses differed depending on whether power was combined into the circular or rectangular output ports, and were not the same for all four hybrids, indicating that better design could reduce the losses. The component losses are given in Table 1, and can be used to predict the power loss distribution, and therefore the power gain expected, in a BPC system.

Component	Insertion Loss	
WC281 (2.81-inch-diameter)	1.1 dB/ $\mu$ sec	22%/μsec
WC184 (1.84-inch-diameter)	3.6 dB/ $\mu$ sec	56%/μsec
WR90 (0.9 × 0.4-inch <sup>2</sup> )	0.1 dB/in	2%/in
H1 circular output port	0.12 dB	2.8%
H2 circular output port	0.11 dB	2.6%
H3 circular output port	0.10 dB	2.2%
H4 circular output port	0.08 dB	1.9%
H1 rectangular output port	0.35 dB	7.7%
H2 rectangular output port	0.35 dB	7.8%
H3 rectangular output port	0.32 dB	7.1%
H4 rectangular output port	0.33 dB	7.4%
Mode transducer	0.07 dB	2%
Bend, phase-shifter, and tapers	0.1 dB	2%
Linear taper (2.81" 1.84" dia.)	0.01 dB	0.2%

Table 1. Insertion losses of individual components. The circular waveguide losses are calculated. All other losses are measured.

An electrical schematic of the three-stage high-power X-band BPC is shown in Figure 2. Differences between the low-power and high-power experimental set-ups, are indicated in the figure. The corresponding physical assembly is shown schematically in Figure 3. Since only a single X-band klystron currently is available at SLAC, we have configured the BPC phase-reversal keying and delay-line lengths for two identically phase-modulated inputs, as discussed by Latham.<sup>3</sup> (The klystron has two output ports, both phase-modulated identically.)

Variable phase-shifting in the delay-lines is necessary to obtain proper relative phasing of the inputs to each hybrid. This high-power phase-shifting is accomplished using motor-controlled translation tables to move the delay-line trombone bends in and out by up to 720° of rf phase in steps of 3°.

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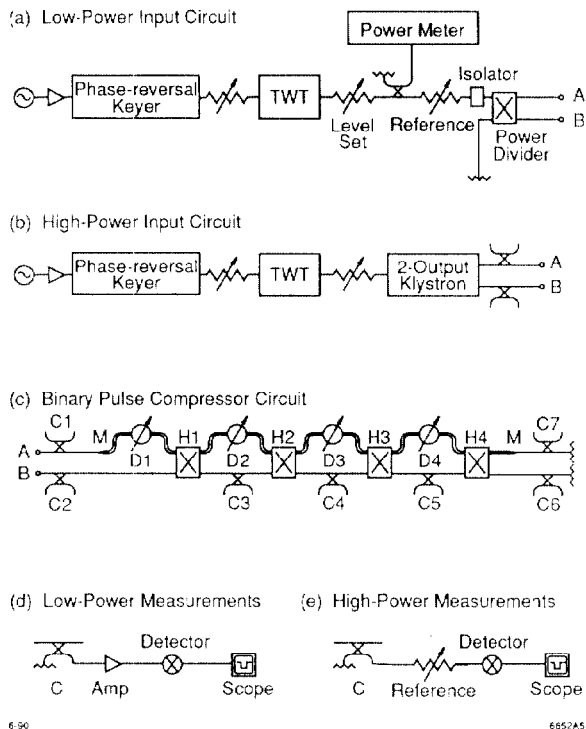


Figure 2. Electrical schematics of the input circuits (a) and (b), the binary pulse compressor (c), and the circuits for measuring rf power (d) and (e). Symbols "H" indicate 3-dB couplers (hybrids). Symbols "D" indicate delay-lines with phase-shifters. Symbols "C" indicate 55-dB directional couplers. Symbols "M" indicate rectangular-to-circular mode transducers.

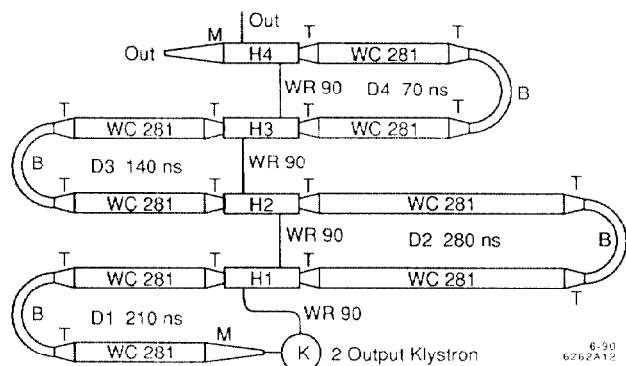


Figure 3. Physical layout of the BPC components. "WR90" is rectangular waveguide. "WC281" is 2.81-inch-diameter circular waveguide. Symbols "H" indicate 3-dB couplers (hybrids) that couple WR90 to WC281. Symbols "B" indicate WC184 bends with phase-shifters. Symbols "T" indicate linear tapers from 1.84-inch to 2.81-inch-diameter. Symbols "M" indicate rectangular-to-circular mode transducers.

Each of the two outputs of Stage-3 normally would be used to power an accelerator section. However, the three-stage BPC we have implemented has a fourth hybrid which permits the two Stage-3 outputs all be combined into a single output (by adjusting the high-power phase-shifter in delay-line D4). While some power is lost in the hybrid combiner H4, this highest-power

single output is expected to be useful for rf-breakdown studies of accelerator structures.

The three-stage BPC is brought into operation by phase-modulating the low-level input rf in 70-nsec time-bins, using the phase-reversal keyer in Figure 2(a) and (b). Then, stage-by-stage, the high-power phase-shifters in the delay-lines (D1, ..., D4) in Figure 2(c) are adjusted to obtain the relative phasing of inputs to each hybrid (H1, ..., H4) appropriate for power multiplication.

The compression process, stage-by-stage, is documented by the scope photos in Figure 4, taken with 1-kW total input from a TWT. The final compressed pulse length is 10 nsec shorter than the 70 nsec expected. Presumably, this is because the input waveguides differ in length by 10 nsec, so the phase-shift that controls the pulse compression does not occur at both inputs until 10 nsec into each 70-nsec time-bin. The rise-time of the compressed pulses appears to be dominated by the rise-time of the TWT, which reverses phase more slowly than the phase-reversal keyer. We are about to study carefully the phase-reversal rise-time of the klystron.

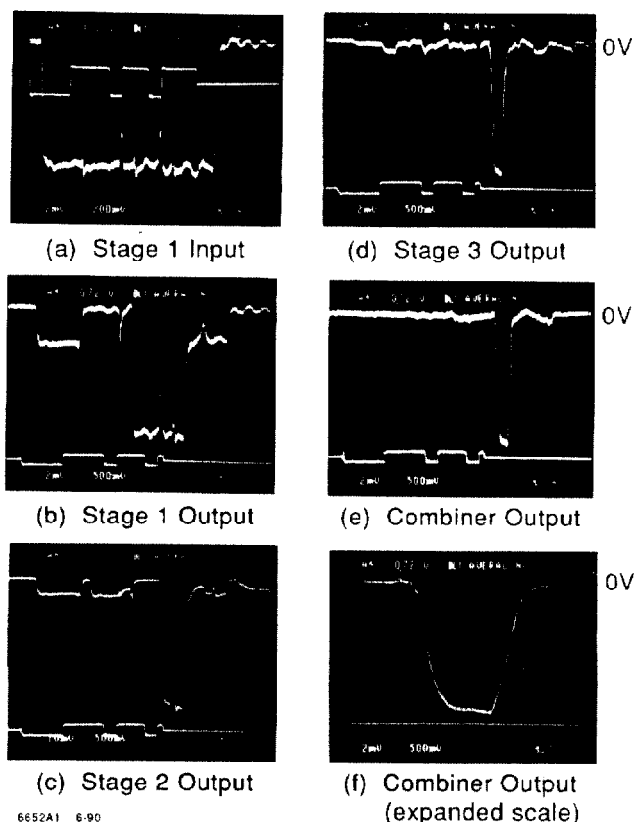


Figure 4. Microwave pulses measured with 1-kW total input power. The "digital" trace also visible on each photo is the output of a phase detector (+ or -). Pulse compression is evident in photos (a)-(d). The combiner output, in photos (e) and (f), is the sum of both Stage 3 outputs.

All rf power measurements were made at the 55-dB directional couplers (C1, ..., C7) in Figure 2(c), using tunnel diode detectors and a fast oscilloscope. Measurements were corrected by the precisely measured coupling ratio of each directional coupler. Absolute power levels were determined from a calibration of the detector performed using a long pulse and a power meter. Power gains were determined by making relative power measurements using a precision variable attenuator to produce the same

Stage(s)	Power Gain (and Compression Efficiency)		
	Ideal	Expected	Measured
1	2	1.77 (88%)	$1.75 \pm 0.10$ (88 $\pm$ 5%)
2	2	1.81 (90%)	$1.79 \pm 0.10$ (90 $\pm$ 5%)
3	2	1.85 (93%)	$1.75 \pm 0.12$ (88 $\pm$ 6%)
1-3	8	5.91 (74%)	$5.47 \pm 0.27$ (68 $\pm$ 14%)
Combine to rect.	1	0.91 (91%)	$0.90 \pm 0.04$ (90 $\pm$ 4%)
Combine to circ.	1	0.94 (94%)	$0.87 \pm 0.03$ (87 $\pm$ 3%)
1-Combine to rect.	8	5.35 (67%)	$4.92 \pm 0.36$ (62 $\pm$ 4%)
1-Combine to circ.	8	5.58 (70%)	$4.76 \pm 0.19$ (60 $\pm$ 2%)

Table 2. Power gains (and compression efficiencies). Measured values are averages of three sets of measurements performed with 1-kW TWT input.

diode detector voltage at each directional coupler. For the relative low-power measurements, the BPC input (TWT output) was attenuated using the "reference" attenuator in Fig. 2(a). For relative high-power (klystron) measurements, the directional coupler outputs were attenuated using the "reference" attenuator in Fig. 2(e).

The peak power gain of the three-stage BPC was determined from relative power measurements with 1-kW total input from the TWT, divided equally into the two BPC input ports as in Figure 2(a), (c), and (d). Power gain for stages 1-3 is defined as the sum of both outputs divided by the sum of both inputs. Gain for the combiner stage is defined as the single combined output divided by the sum of both inputs. The combiner hybrid H4 has two possible outputs, circular and rectangular, each with different losses, as in Table 1. The gain of the combiner stage always is less than one, since the combined pulse, while greater than either of the uncombined pulses, is smaller than their sum due to the losses. The measured stage-by-stage power gains are given in Table 2. The power compression efficiency, also included in Table 2, is defined as the ratio of real power gain to "ideal" power gain in the absence of losses.

In short, Stages 1-3 each multiply peak power by about 1.8, corresponding to a power compression efficiency of about 90%/stage. The gain and efficiency of the first three stages, taken together, are about 5.5 and about 70%, respectively. The combiner output is about 1.8 times higher-power than either of the Stage-3 outputs. The reflected power monitored at each stage is less than 4% of the forward power.

The measured losses of individual components (Table 1) have been used to predict the distributed losses in each stage of the three-stage BPC, and to predict the power gain expected to be measured at the 55-dB directional coupler following each stage. The expected gains are shown in Table 2, and agree well with the measured gains.

The SLAC prototype X-band klystron has two output ports. Pulses of up to 10 MW per port have been produced at the 770-nsec pulse-length required by the three-stage BPC. (Higher power is expected from the next prototype klystron.) The first attempt at compressing relatively high-power klystron pulses produced the photos shown in Figure 5. Compression is evident, but the experiment was plagued with problems. The output mode transducer and load had not yet been installed, so the circular waveguide output was simply shorted, and no power measurements were possible at coupler C7. The two input lines were poorly matched, causing frequency dependent reflections and unequal power levels at the two BPC inputs. It was later determined that the two vacuum windows in one of the input waveguides had broken at some time during the high-power experiment. Under these circumstances, the power gains observed did not meet expectations. Nevertheless, with 10-MW measured at C1, and 5 MW measured at C2, a 37-MW output was observed at C6.

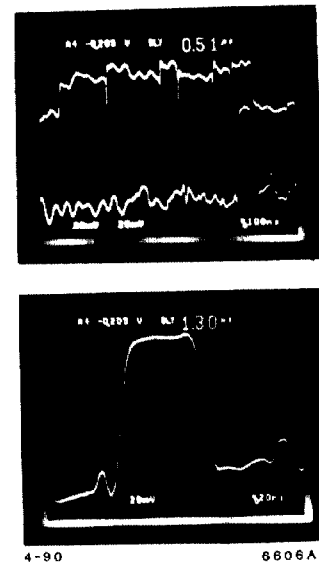


Figure 5. Microwave pulses measured in the initial high-power experiment (15-MW total input). Top picture: the upper trace is the modulated klystron output, the lower trace is the compressed pulse. Bottom picture: the compressed pulse expanded in time. The combiner output, (e) and (f), is the sum of both Stage 3 outputs.

Further high-power experiments are commencing as of this writing. Assuming the gains measured at low-power (Table 4), for 20-MW of klystron power (10 MW per input) we expect 55-MW compressed pulses at each Stage-3 output, and 98-MW compressed pulses after combining to a single output.

When two X-Band klystrons become available, the binary pulse compressor will be reconfigured to utilize both of these high-power sources. If each klystron produces 100-MW, we expect 550-MW compressed pulses at each Stage-3 output, and 980-MW compressed pulses after combining to a single output. For 550 MW, peak surface fields in the hybrid slots and in the WR90 guides are estimated to be only 80 MV/m, well below the expected threshold for breakdown.

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## References

1. Z. D. Farkas, "Binary Peak Power Multiplier and Its Application to Linear Accelerator Design," *IEEE Trans. MTT-34*, p. 1036 (1986); "Binary Power Multiplier for Electromagnetic Energy," United States Patent 4,749,950 (June 7, 1988).
2. Z. D. Farkas, G. Spalek, and P. B. Wilson, "RF Pulse Compression Experiment at SLAC", SLAC-PUB-4890 (June 1989), published in Proceedings of the 1989 IEEE Particle Accelerator Conference (Chicago, Illinois), edited by F. Bennett and L. Taylor, IEEE Catalog No. 89CH2669-0, pp. 983-986.
3. P. E. Latham, "The Use of a Single Source to Drive a Binary Peak Power Multiplier," 1988 Linear Accelerator Conference (Williamsburg, Virginia), CEBAF-R-89-001, pp. 623-624.