Digital Beam Controls for Synchrotrons and Storage Rings in the CERN PS Complex

F. Blas, J. Boucheron, B.J. Evans, R. Garoby, G.C. Schneider, J.P. Terrier, J.L. Vallet
CERN-PS
CH - 1211 Geneva 23

Abstract

New beam control systems have been designed for the acceleration of lead ions in the PS complex. The standard selected satisfies the medium term needs of all six synchrotrons and storage rings in the PS division, for the minimum cost. Special care has been taken to preserve the beam gymnastics capability that characterises the PS machine. Digital technology is used where it is considered to bring decisive advantages over more traditional analogue techniques. Full scale tests of these beam control systems have been done with protons during the LHC injectors test run in December 1993. Concept, design and practical experience are reported.

1. INTRODUCTION

As part of the lead ion acceleration project at CERN [1], a major development is required to equip the 4-ring PS Booster with adequate beam controls. These needs add to the requirements for filling the LHC [2] and for maximum compatibility with the already installed equipment in the six synchrotrons of the PS complex.

Direct digital synthesis is the obvious choice for the RF source, based upon the experience gathered on its use in our machines since 1980, and on its ease of use with modern integrated circuits. Consequently, only digital technology is used in the cascade of modules generating the open loop RF sine wave from real-time measurement of the B field. Standard RF techniques are applied for the processing of beam and cavity return signals. A high speed ADC (12 bits @ 10 Ms/s) makes the link between the phase loop analogue correction signal and the digital frequency modulation input.

Built-in facilities provide easy means to correct the frequency programme and to change the harmonic number. Special care is taken to ensure and to verify error-free data transmission between modules.

2. SYSTEM

2.1. Description

A generic beam control system was first designed including all the capabilities needed in the PS synchrotrons complex. (Figure 1). A construction standard was selected based on NIM mechanics and front panel coaxial connectors of Lemo OO type. No radial loop is represented as the digitally generated frequency is sufficiently accurate to centre the beam in the vacuum chamber. Correction signals can be entered into the summing node of the beam phase loop, to implement other functions, e.g. synchronization to an external source.

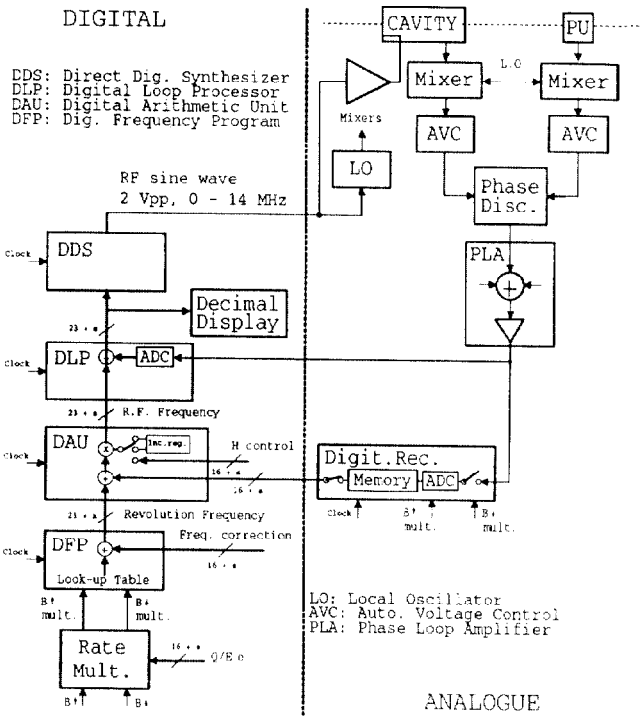

Figure 1. Generic beam control system.

2.2 Analogue functions

The beam and cavity return signals are translated to a fixed intermediate frequency of 10.7 MHz using standard super-heterodyne techniques. Commercially available FM receiver components are used when possible. A phase-locked loop generates the local oscillator signal at f_{RF} + 10.7 MHz. Global electrical characteristics of the processing chain are given in Table 1.

Table 1
Characteristics of RF analogue processing

Frequency	0.4 to 10 MHz
Input level	0.1 mV to 1 V pp
IF band-width	200 kHz
Signal/Noise at 0.1 mV pp input level (2 kHz bw)	23 dB
Overall delay for phase demodulation	< 5 µs

2.3 Digital functions

All modules in the digital part use a common 10 MHz clock, broadcast to all accelerators in the PS complex. Strobed data transfers are used, and differential transmission is applied for distances larger than ~1 m. Extensive monitoring capabilities are implemented, in the form of digital test outputs which allow connection to the decimal display device, or of analogue signals from DACs.

The Digital Frequency Programme (DFP) delivers the revolution frequency word. The B Rate Multiplier provides easy control for particles with different charge/mass ratio. In the Digital Arithmetic Unit (DAU) the revolution frequency word is multiplied by the selected RF harmonic number. Correction of the frequency programme is achieved with the Digitizing Recorder (DR) which reproduces the correction memorised during a reference acceleration where the beam was accurately centred in the vacuum chamber. Table 2 lists the basic performance of the digital set-up.

Table 2
Characteristics of the digital system

Output Frequency	10 Hz to 14 MHz
Output level	2 V pp / 50 Ω
Resolution	2.4 Hz
Maximum spurious component	- 55 dBc
Analogue modulation band-width	0 to > 2 MHz
Delay from the analogue modulation input	~ 500 ns

3. MODULES

The following description concentrates on the new digital functions.

3.1 Digital Frequency Programme (DFP)

The DFP (Figure 2) contains a look-up table in EPROM, that gives the revolution frequency corresponding to the instantaneous B field totalled in a B train counter. The same table is used for different ions, changing the rate of the B train in proportion to the charge/mass ratio (Rate Multiplier in Figure 1). The output data are transferred synchronously with the common 10 MHz clock.

A summing input (16 bits) is provided to introduce specific frequency corrections, e.g. for adiabatic capture of the linac beam in the CERN PS Booster (PSB).

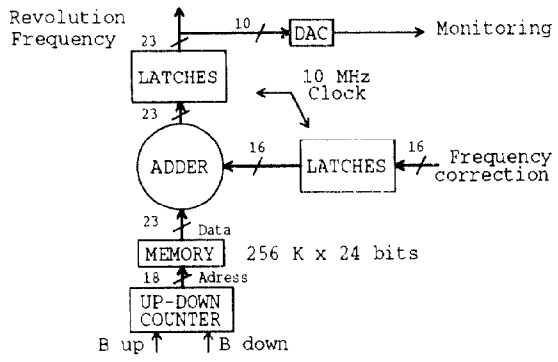

Figure 2. Digital Frequency Programme.

3.2 Digital Arithmetic Unit (DAU)

The correction coming from the Digitizing Recorder is added directly to the revolution frequency word, making it independent of the harmonic number (Figure 3). The modified frequency is then multiplied by the harmonic number (monitored by a local display), the result being the RF frequency. In remote mode, it is entered as a 16-bit word on a multi-pin connector. In local mode, two values (integers) are selectable.

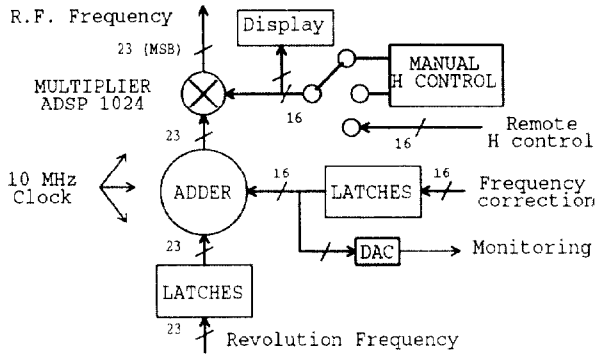

Figure 3. Digital Arithmetic Unit.

3.3 Digital Loop Processor (DLP)

The analogue error signal of the beam phase loop is converted by a 10 Ms/s ADC into a 12-bit word (Figure 4). Gain control is provided in steps of 6 dB, by shifting the weight of the bits. A digital adder sums the result with the nominal RF frequency word delivered by the DAU.

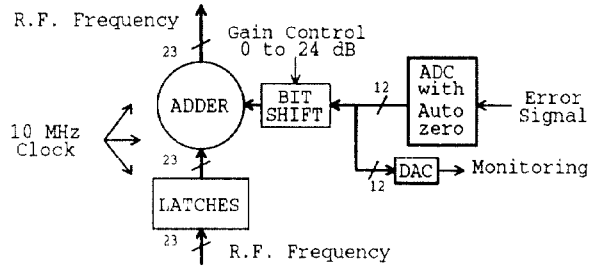

Figure 4. Digital Loop Processor.

Internal logic gates the injection of the error signal, and triggers an auto-zero process during dead times.

3.4 Direct Digital Synthesizer (DDS) (Figure 5)

A commercial integrated circuit (Qualcomm Q2220) implements the direct digital synthesis technique [3]. The RF sine wave is obtained by digital-to-analogue conversion of its 10-bit output. The distributed 10 MHz clock is multiplied by 4 to provide the internal clock required for the generation of sine waves up to 14 MHz.

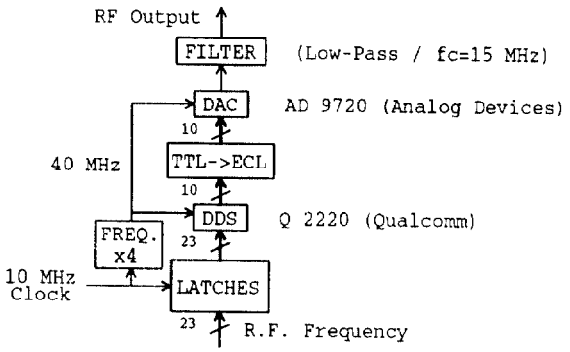

Figure 5. Direct Digital Synthesizer.

3.5 Digitizing Recorder (DR)

The DR (Figure 6) has 2 modes of operation. In the "Learn" mode (beam phase loop "on"), it records the error signal fed into the DLP, at a memory address given by the B train counter. Nothing is sent to the DAU. In the "Replay" mode, the recorded data are sent into the frequency correction input of the DAU. With beam phase loop "off", and for the same magnetic conditions, beam position in the vacuum chamber is the same in "Replay" mode as it was when the "Learn" mode was triggered.

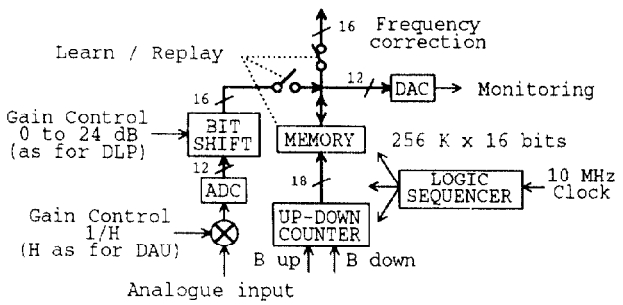

Figure 6. Digitizing Recorder

The analogue input signal is converted by a 12-bit ADC, and scaled to the beam revolution frequency using the harmonic number applied in the "Learn" phase and the setting of the DLP gain. The resulting digital word is stored in memory when in "Learn" mode.

4. Experience and Forecast

4.1 LHC injectors' test and other applications

New low level RF systems for the PSB and for the PS were built for the needs of the LHC injectors' test at the end of 1993, using the new standard modules and based on the "generic beam control" described in section 2.1. The "main" harmonic number was 1 in the PSB (0.6 to 1.8 MHz) and 16 in the PS (~ 7.6 MHz). Additional capabilities were implemented (1) in the PSB to drive the 2nd harmonic cavity for bunch lengthening and the 9th harmonic cavity for controlled blow-up, and (2) in the PS to provide both harmonic 8 and 16 for bunch splitting and acceleration.

The new hardware performed reliably in all these uses, and contributed in a decisive way to the success of the test [4, 5].

Other applications are being treated, like the beam controls for lead ion acceleration in the PSB and the upgrade of existing systems in the PS. The number of modules built is now greater than 200.

4.2 Future evolution

The present frontier between analogue and digital technologies was dictated by the limitation in resources. The intention is to evolve in the direction of digital technology, but in progressive steps, when clear advantages can be expected, and at a rhythm governed by the means available.

An obvious first candidate for such an evolution is the synchronization loop, where flexibility in the implementation of non-linear transfer functions is very important and where digital technology can drastically reduce the amount of hardware. Promising results have already been obtained, using developments done for the low level RF of SSC injectors [6].

5. References

[1] D. Warner (editor), "CERN Heavy-Ion Facility Design Report", CERN 93-01.

[2] The LHC Study Group, "Design Study of the Large Hadron Collider (LHC)", CERN 91-03.

[3] S. Turner (editor), "RF Engineering for Particle Accelerators" (CAS), CERN 92-03, pp. 435-438.

[4] R. Cappi, R. Garoby, M. Martini, J.P. Riunaud, K. Schindl, "The PS as LHC Proton Source: Results of the Two-week Beam Test in December 93", These Proceedings.

[5] R. Garoby, S. Hancock, "New Techniques for Tailoring Longitudinal Density in a Proton Synchrotron", These Proceedings.

[6] L.K. Meshta, V. Brouk, R.C. Webber, J. Mangino, T. Uher, "A Digital Beam Phase Loop for the Low Energy Booster", Proceedings of the 1993 Particle Accelerator Conference, May 1993, pp. 2382-2384.