Bunch-by-Bunch Longitudinal Feedback System for PEP-II

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Abstract

This paper describes the implementation of the bunch-by-bunch longitudinal feedback system for the PEP-II *B* Factory. Bunch spacing down to 2 ns is achieved using 500 Megasamples per second A/D and D/A converters, and AT&T 1610 Digital Signal Processors are integrated to run a downsampled feedback algorithm for each bunch in parallel. This general purpose programmable system, packaged in VXI and VME, is modular and scalable to offer portability to other accelerator rings. The control and monitoring hardware and software architecture have been developed to provide ease of operation as well as diagnostic tools for machine physics.

1. INTRODUCTION

The PEP-II *B* Factory will achieve its high luminosity goal by populating many bunches at high current [1]. This high beam current in the PEP-II rings can provide strong excitation of high order modes and generate voltages which drive coupled-bunch instabilities. In PEP-II the beams are made up of 1658 bunches which can be thought of as 1658 weakly coupled harmonic oscillators, resulting in a system with 1658 normal modes. Some of these modes are unstable and cause the energy of the particle to diverge from the design goals [2].

The PEP-II longitudinal feedback system is based on a time domain approach which damps the energy oscillation of each bunch individually. The main feature of this approach is that the feedback acts to damp any disturbance to the bunch since no assumption is made about the nature of the driving term.

2. PRINCIPLE OF OPERATION

The longitudinal feedback process consists of measuring the instantaneous phase of each bunch with respect to the ring oscillator and provide a correction voltage for each bunch via a kicker structure. As this process only uses the information from a particular bunch to compute the feedback signal for that bunch a parallel processing scheme is feasible with many processors, each processing a fraction of the total bunch population and keeping track of a group of bunches. However, if one wants to measure the phase and compute a new correction value for each bunch on every revolution around the ring, the system grows in size and complexity because many processors are required and the data movement bandwidth becomes a bottle-neck. We take advantage of the fact that the sampling frequency (revolution frequency) is greater than the synchrotron frequency. This inherent oversampling allows the use of a downsampled process [3,4] in which the information about a bunch's oscillation is used only every n revolutions and the kick updated every n turns resulting in a reduction of the number of processors needed by a factor n. In PEP-II the downsampling factor has been selected to be four.

Figure 1 shows the conceptual design of the longitudinal feedback system. The phase of each bunch is measured and a feedback correction signal for each bunch is computed and applied via the kicker [5]. The downsampler allows the processing element to handle a greater number of bunches, while the hold-buffer repeats the most recent kick for a bunch until a new one is computed.

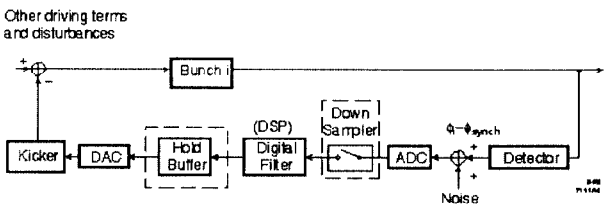

Figure 1. Conceptual bunch-by-bunch, downsampled feedback

3. SYSTEM ARCHITECTURE

Figure 2 shows the essential components of the longitudinal feedback system. The bunch phase signal is derived from a detector which consists of four button pickups (Beam Position Monitor electrodes) connected to a comb generator (a passive structure with periodically coupled microstrips). The comb generator structure generates an eight cycle tone burst at the sixth harmonic of the ring RF frequency for each bunch passing by the pickup, this tone burst must be short enough to make unambiguous measurements for individual bunches, that is less than 4.2 ns in PEP-II.

The tone burst from the comb generator is mixed with a 2856 MHz signal from a master oscillator phased locked to the ring RF. The choice of a 2856 MHz operating frequency allows a phase processing range of $\pm 15^{\circ}$ at the 476 MHz frequency of the RF system with a resolution better than 0.5°. A filter on the output of the mixer limits the bandwidth for noise reduction.

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The digitizer converts the phase-error signal from the mixer at the bunch crossing frequency. Based on the revolution number the downsampler selects which bunches' data are sent to the processors.

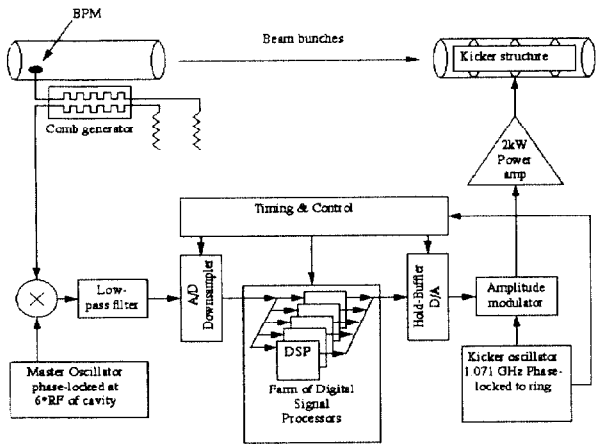

Figure 2. Block Diagram of the PEP-II Longitudinal feedback System

Since the synchrotron frequencies are audio frequencies, components developed for audio and speech applications are well matched to perform the longitudinal feedback computation. The PEP-II longitudinal feedback system is designed as a digital processing system which takes advantage of the recent development in Digital Signal Processors (DSP) used for communications.

The hold buffer stores the latest phase correction value calculated for each bunch. The buffer output drives a fast DAC which converts at the bunch crossing frequency. The calculated output is a baseband correction signal, while the longitudinal kicker structure is designed to operate in the range of 1.00 to 1.25 GHz. The amplitude modulator transfers the base-band DAC signal into modulation on a kicker oscillator signal [6].

The power amplifiers are commercial products which operates at 1-1.25 GHz with an output power of 2.0 kW.

4. IMPLEMENTATION

We chose to implement the PEP-II longitudinal feedback system using VXI and VMEbus standards as shown in figure 3. The front-end and the back-end elements of the system are packaged within a VXI C size mainframe which provides good electromagnetic shielding, cooling and system power for the high speed cicuitry. VXI also offers wide modules to accommodate large RF and analog components as well as large heat sinks required for some ECL circuits. The processing engine of the system uses a typical multi-processor architecture based on the VME bus. However one of the challenges we had to meet in this system is the data rate imposed by the high bunch crossing rate; even with a downsampling factor of four in PEP-II the data rate to and from the processing farm is nearly 120 Mbytes per second. The approach taken groups the phase measurement data from four successive bunches to form 32 bit words and distributes these data words over up to four VME backplanes.

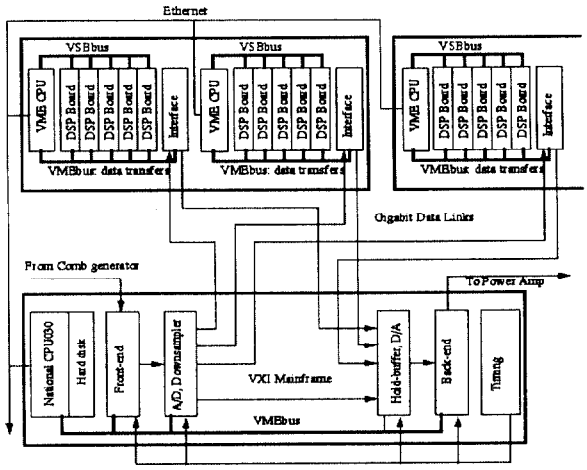

Figure 3. System implementation

4.1 System control

The longitudinal feedback uses commercially available embedded computers running the VxWorks (Wind Rivers Systems) real time operating system to initialize, control and monitor the system. The operator interface is based on the EPICS control system tool kit from LANL/ANL. The VXI based computer which has a hard disk also serves as the system console. The VME based computers have a VSBbus interface which is used to communicate with the DSP boards while the feedback is running, since the VME traffic cannot be interrupted during operation. Of course the VSB bus limits the number of DSP boards within one backplane to five, however this limitation does not hamper the efficiency of the system since the VME bus bandwidth is reached with only that number of DSP boards. We install two VME ten slot backplanes within one VME chassis each with its own VME/VSB embedded computer to implement the DSP processing crate. All computers are linked via an Ethernet connection

4.2 Timing module

This module receives the RF signal and a revolution harmonic. It generates all the timing signals required and distributes them throughout the system. It generates the revolution fiducial and ECL bunch clock to the downsampler, the 2856 MHz for the front-end and the 1071 MHz signal for the back-end modulator. The VMEbus is used to control the phase of critical timing signals, to read back levels and error conditions such as missing or extra revolution fiducial, and to turn the clock on and off.

4.3 Front-End

The baseband phase error signal for each bunch is generated in this module. The VME bus controls an input gain used to compensate for overall ring current, and a reference phase adjustment to center the bunches' synchronous phase in the linear range of the phase detector.

4.4 Downsampler

The distribution of the data is accomplished in the ADC/-Downsampler module where the phase error of each bunch is digitized by an eight bit ADC (Tektronix TKAD10C). The downsampler is implemented as a table driven system in which a memory is used as a look-up table to control the distribution of phase error signals and collection of phase correction signals. It is programmed at system initialization via the VME bus to execute an n turn downsampling sequence. While running the look up-table memory is read at 1/4 the bunch frequency. Each cycle, the content is interpreted to latch the data from selected groups of four consecutive bunches on a specific revolution. The content of the latch is then directed to one of four serial data link connected to an interface board in a VME backplane. The information sent over the data links contains the phase error data of four successive bunches, the bunch-group identification, the DSP board address, the hold-buffer memory address and status information. The transfer rate over the serial links is 1,200 Mbits per second.

4.5 Serial links to VME interface

Once enabled by the local VME computer this interface becomes bus master to establish the links between the downsampler, the DSP boards and the hold buffer. It performs Read-Modify-Write cycles to access the DSP boards. Data previously computed for phase correction of four bunches is read from a DSP board and sent via a second serial link to the hold buffer along with its memory address received from the downsampler. The incoming data from the downsampler is then written into the addressed DSP board. Since each DSP computes the phase correction for several bunches the system is pipelined. Therefore, the data out of a DSP board is not the phase correction for the group of bunches who's phase information is coming from the downsampler

4.6 DSP board

Each DSP board supports four AT&T 1610 Digital Signal Processors having a 25ns cycle time. Each byte of the 32 bit VME bus is connected to the upper eight bits of the Parallel I/O port of one DSP via a simple interface, and the lower eight bits of the PIO receive control information from the VME address bus. The VSBbus side of the board is connected to dual ported memories used to download the filter algorithm to the DSPs, and to exchange data between the DSPs and the VME computer for monitoring and diagnostic purposes. The interrupt handling between the VME computer and the DSPs, is also routed via the VSBbus [7]. In addition a JTAG interface to the front panel of the module can be used for code development.

4.7 Hold Buffer

The phase correction computed by the DSP is received by the hold-buffer via the serial link and written to a memory location corresponding to the bunch to which it applies. The hold buffer memory is a self-timed SRAM (Synergy SY101492) with a hidden write cycle timing, that is, while the memory is continuously being read out at 1/2 the bunch crossing frequency it is possible to write into it at a different address location. The read address is provided by a bunch counter and the write address comes from the downsampler memory via the VME interface. This offset between the read and write addresses allows the kicker to be located at any point in the ring. The output of the hold buffer drives a DAC (Triquint TQ6122) converting at the bunch crossing frequency.

4.8 Back-End

The back-end receives the correction signal from the hold buffer DAC and generates the kicker correction signal for the power amplifier. The RF carrier at 2.25 times the RF from the timing module is Quad Phase Shift Keyed (QPSK modulated) at the RF clock rate to generate a kicker drive signal. The kicker signal is amplitude modulated by the hold buffer output signal. The VME interface allows the feedback loop to be opened or closed and the drive level to the power amplifier to be adjusted.

5. CONCLUSION

A general purpose programmable and modular longitudinal feedback system is being designed with completion of a full scale prototype planned during the summer of 1994. As of this conference the DSP boards are in production, and the downsampler and hold buffer modules are being tested. The prototype will be installed and tested at the Advanced Light Source at LBL. The operational principles have been very successfully demonstrated using a quick prototype [8]. Due to its flexibility the system described herein can be used in many rings without any modifications.

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