A Low Power RF System for the PLS Cavity Test Facility

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Abstract

A low power RF system for use in the Pohang Light Source (PLS) cavity test facility has been designed and constructed at Daresbury Laboratory. A VME solution using an OS-9 real-time operating system has been selected for the control and monitoring of parameters. Details of system components and commissioning experience will be reported. The system has now been delivered to the PLS site.

1. INTRODUCTION

Daresbury Laboratory won the competitive tender to design and construct the low power RF system for the Pohang Light source (PLS) cavity test facility. According to the terms of the contract, Daresbury staff designed and supervised the construction of the system by two Pohang engineers based at Daresbury.

The system provides all the low power equipment to drive the power source (a TV transmitter supplied by Harris TVT) and cavity control. Monitor and control of all essential parameters is by a VME based system using a OS-9 real-time operating system.

The agreement was specifically for the test facility, but the system was designed so that it could be used in the storage ring RF system, and it could be expanded to incorporate more cavities and klystron.

2. SYSTEM REQUIREMENTS

The system consists of two parts:

1. The computer control system, and
2. Low level RF hardware.

3. COMPUTER CONTROL SYSTEM

The system chosen was VME based, using a Motorola MVME147 single board computer [1] and OS-9 Real-time Operating System [2] for two reasons: it allowed compatibility with the planned control system for the Pohang Light Source; and a similar system was being developed for the SRS RF Cavity Test Facility. The full details of the latter are described elsewhere [3] and so a summary will be given here. The MVME147 is a 68030 based computer optimised for VMEBus control, with 4MByte RAM, a maths co-processor and a wide range of interfaces, including SCSI (for linking to disk drives) and ethernet. OS-9 is a powerful operating system which is multi-tasking and real-time, that is, it can run processes and perform actions at user specified times, rather than at the next available timeslot. Thus making it ideal for machine control applications.

A large number of control and monitor points were required to be connected to the control system, but the method of interfacing had to be flexible, allowing for both re-configuration and expansion. Dedicated single function VME boards, which would be ideal for an large scale operational system, for a storage ring as an example, can be expensive and too rigid for a test facility. It was decided to use the IndustryPack™ (IP) [4] modular plug-in system for interfacing. IP's are small (credit-card sized), self-contained boards, each one providing a specific function. A 6U VME card provides a "motherboard" for up to four of these IP "daughter boards", and the functions of the four IP's can be mixed. The PLS specification called for 28 Analogue Monitor, 5 Analogue Control, 50 Digital Monitor and 16 Digital Control channels, as well as GPIB (IEEE-488) capability, to drive the master RF source. This was implemented as two IP carrier cards, which were addressable by the OS-9 drivers as IP0 and IP1, each with four slots available. The allocation of interfaces is shown below.

SLOT	IP0	IP1
A	48 Line Digital I/O	20 Channel 12-bit ADC
B	32 Line Digital I/O	20 Channel 12-bit ADC
C	48 Line Digital I/O	6 Channel 12-bit DAC
D	GPIB Bus Driver	

The OS-9 drivers purchased for the system allowed very easy access to the hardware interfaces, so that if a analogue control channel was to be written to, a file named "/ip1c" was open in write mode and a link was then made to the IP module.

The heart of the software system, which was written in 'C', is the database module. This is an OS-9 data module incorporating a binary 'C' structure. The data module facility provides a method for the sharing of data between several processes, but with built-in security and error checking so that simultaneous calls to the same information are correctly handled.

The database module is easily created because a database generator program has already been implemented on the SRS, for the upgraded beam steering system which is VME based [5]. This allows allocation of input and output devices to their parameters to be input as a text source file, then compiled for use.

The software modules comprising the PLS RF Test System are shown in Figure 1.

The main control program was designed to be used on any console that could support vt-100 terminal emulation. This would allow PLS engineers to run the system locally, via a serial link, or remotely using the OS-9 ethernet terminal facility. The package produced at Daresbury included a Macintosh LC computer for use as a console, with an ethernet card fitted for use on the PLS system network. A sample of

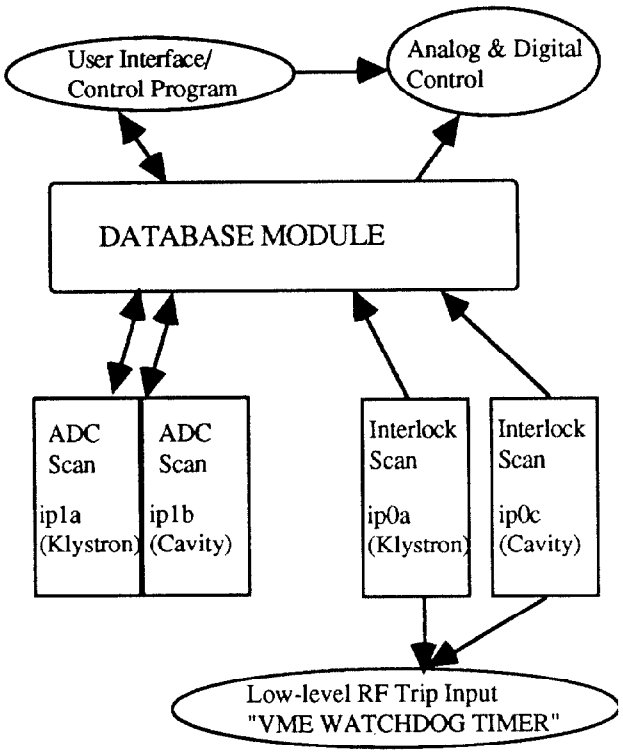

Figure 1. Layout of the RF Control System Programs

the user interface program output obtained at Daresbury prior to shipment is shown in Figure 2. The parameter names are chosen to reflect the section of the system: TX=Klystron Transmitter; CAV=RF Cavity; and RF=Low Level RF.

As can be seen, the interfacing of the digital monitoring for the Klystron (TV Transmitter) and Cavity (including low-level RF circuits) was carried out using separate software modules. This was partly because it was easiest to produce a program handling one IP package at a time, and also because the PLS engineers requested that special attention be paid to the software and hardware for the transmitter interface, including full digital and analogue signal isolation and conditioning. This proved useful, however, to provide a watchdog timer signal for the low level trip detector circuit. This was required so that in the event of a VME system crash, the RF would trip to a safe condition, and was realised as a 1 second period square-wave on a digital output pin, where the two interlock scan modules set and re-set the line. If either program halted the line would remain in the same state for longer than it should and the trip initiated.

The basic software system was shipped to PLS where we understand it is working well. Updates to the software have been sent to PLS as a matter of courtesy as further work continues on the SRS RF VME system.

TX.DRIVE.01	3.00	W		
TX.KHTV.01	4.00	kV	OFF	MAIN I/L FAIL
TX.FWDP.01	4.00	kW		
TX.REVP.01	4.00	kW		
TX.KHTI.01	4.00	A	OFF	READY
TX.PHASE..01	-4.00	Degr		
CAV.GAPVOLTS.01	4.00	kV	OFF	ARC 1
CAV.AUTOTUNE.01	**0.00**	**Degr**	**ON**	
CAV.TPOS.01	4.00	mm	OFF	AUTOTUNE ON
CAV.FWDP.01	-4.00	kW	OFF	READY
CAV.REVP.01	-8.00	kW		
CAV.WIN_TEMP.01	-4.00	DegC		
CAV.TUN_TEMP.01	-4.00	DegC		
CAV.I/P_TEMP.01	-4.00	DegC		
CAV.O/P_TEMP.01	-4.00	DegC		
CAV.O/P_TEMP.02	-4.00	DegC		
CAV.O/P_TEMP.03	-4.00	DegC		
CAV.BODYTEMP.01	2.00	DegC	OFF	OVERTEMP
CAV.BODYTEMP.02	4.00	DegC	OFF	OVERTEMP
CAV.BODYTEMP.03	4.00	DegC	OFF	OVERTEMP
CAV.BODYTEMP.04	4.00	DegC	OFF	OVERTEMP
CAV.BODYTEMP.05	4.00	DegC	OFF	OVERTEMP
RF.PHASE.01	-4.00	Degr		
CONTROL>				

Figure 2. Typical Control Program Output.

4. LOW LEVEL RF HARDWARE

A block diagram of the basic low level system is shown in figure 3. The system was constructed in 3U height Eurocard with the more critical sections shielded with strips of double sided PCB material on these cards. Basic operation of the system is as follows:

On the first card the 500MHz master oscillator is amplified then low pass filtered and finally power split eight ways, each output power is 10 dBm. Only one output is used in the cavity test area system, and this enters a trip card used for klystron protection.

The trip system card consists of a PIN diode and two miniature RF relays in series followed by a coupler used as a two way power splitter. The PIN diode trip control is managed by an EPLD (Erasable Programmable Logic Device.) Logic within the EPLD traps the first trip to occur and latches any other trips which may occur. The trip information and the resetting of the trip logic is controlled by the VME system. In fact, one of the trips is a watchdog timer which if not updated by the VME system microprocessor on a regular basis indicates a system failure and would trip the PIN diode protection system.

The two RF outputs from the PIN diode cards go to an electronic phase shifter which uses quadrature hybrids, electronic attenuators and a combiner. One of the phase

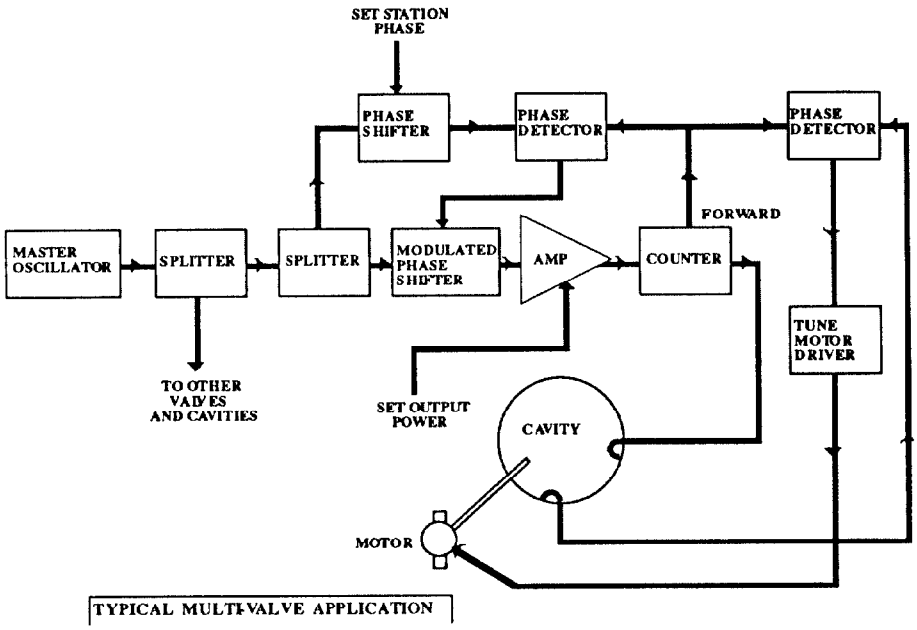

Figure 3 Simple block diagram of RF system

shifters is used to adjust the phase of the forward power to the cavity relative to Master Oscillator phase (station phase). The second phase shifter is electronically modulated by the output of the Station Phase phase detector to set the correct output phase (Station Phase).

Within this phase control loop is the card controlling output power level so that any phase change as power is raised due to the power control element is automatically corrected for by the station phase detector loop.

The required RF power level enters the card as a 0 to +10v signal from a VME DAC and this can be open loop or closed loop servo on forward power or Cavity power level.

RF outputs and DC Monitoring are made for forward and reverse power and cavity power. Temperature compensated diode detectors are used to give a 30dB range.

The Cavity tuner is driven by a stepper motor. The motor may be set to a particular tune position using a feedback signal from a reference potentiometer, or driven by the cavity auto tune loop phase detector. The VME system can select autotune but if for any reason the cavity power reduces below minimum threshold the cavity reverts to tuner position setting.

The phase detectors [6] used in this equipment use synchronous mixing techniques and the actual phase comparison takes place at 2MHz. An edge sensitive phase detector with no deadband is programmed within an EPLD and is crucial to the high precision of the phase detector. The station phase changed by less than 0.2° for a 20 dB change in output level. Similarly the cavity detune angle changed by less than 0.2° over the same 20 dB range.

5. SYSTEM PERFORMANCE

The system fully met the specification and has been shipped to Pohang, where after commissioning is in use in the RF Test Facility.

6. ACKNOWLEDGEMENTS

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