A ZVT CONVERTER FOR SUPERCONDUCTING CORRECTOR MAGNET APPLICATIONS

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Abstract

The aim of the present paper is the description design considerations and presentation of experimental results of a high current (1.000A) and low voltage (up to 15V) converter for the excitation of a superconductive magnet in particle accelerators. The power source, which is based on a ZVT converter, presents high efficiency, small output ripple, excellent line regulation and fulfilment of EMC regulations.

1. INTRODUCTION AND BACKGROUND

The current tendency in particle accelerators is the construction of the magnets for particles acceleration by means of superconducting materials. By using this type of magnets, magnetic fields near 10T can be reached, a value impossible to reach with traditional technologies of magnets. This change of tendency impacts on the type of source to use for the excitation of them. While with the traditional magnets medium voltage and medium current power supplies were required, with the new superconducting magnets low voltage and high current sources are needed. Moreover, following the nowadays power electronics trends for minimising size while improving efficiency, it is desirable to provide galvanic isolation by using high frequencies rather than the classical, and low efficient, 50 Hz isolation.

The present paper describes a prototype for output voltages between 0 and 15 V and currents between 0 and 1000 A. The design is based on a ZVT converter with isolation in high frequency. The load is a superconducting magnet of 0.2 H and 5 mΩ.

In order to fulfil the above mentioned requirements, and specially to have high efficiency, a full bridge IGBT topology featuring ZVT has been chosen. Figure 1 shows the simplified electrical schema of the power section. The input section consists basically on a non controlled rectifier fed by the three phase 400V network and with input inductors designed to met VDE 0160 low frequency harmonic regulations. This inductors, and the output capacitors of the rectifier, implement a DC filter with 42Hz cut-off frequency that satisfies jointly with the dynamic response of the ZVT converter the audiosusceptibility specification (< 40mV ripple).

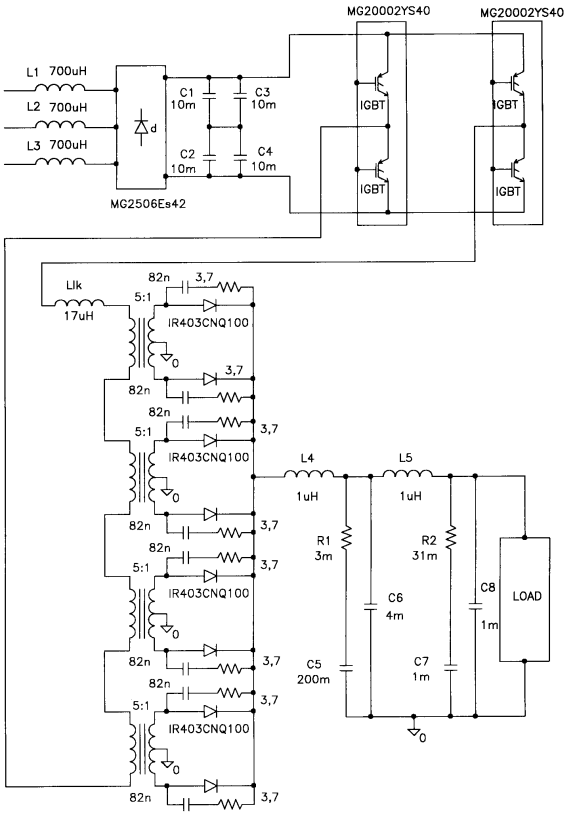

Figure 1: The converter described in the text.

2. DESCRIPTION OF THE CONVERTER

The HF inverter section consists on a water-cooled ZVT IGBT converter with no snubber followed by a high current transformer, a rectifier and a filter. Power regulation is achieved by means of phase shifting as is usually done in a ZVT converter. The operating frequency has been set to 35kHz in order to trade off between losses and a reasonable size for the transformer.

The leakage inductance, Llk, has been selected with a value of 17uH. For that value, the range of ZVT operation begins around 250A. This inductance is performed with the leakage inductance of the ZVT transformer and an added inductance. The high

frequency transformer, that provides the galvanic isolation needed, has been implemented by means of four transformers with the primaries in series and the secondaries in parallel having each transformer a transformation ratio 5:1. The transformers are water cooled both in the primaries and in the secondaries. On the other hand, the connections have been carried out by means of bus-bar of very small inductance (less than 20nH).

In order to decrease losses, for each set transformer plus rectifier stage, we have chosen a centre-tapped configuration at the secondaries that employs high current (400A) and high voltage (100V) shottky diodes. A simple low power RC network is enough to damp the parasitic oscillations between the transformer leakage inductance and the capacitance of the diodes. Due to the voltage levels handled at the output, it is not necessary the use of an active clamp.

To maintain the switching ripple into the desired levels a fourth order filter with cut-off frequencies 320Hz and 20kHz has been used. Air core inductors have been implemented for this task.

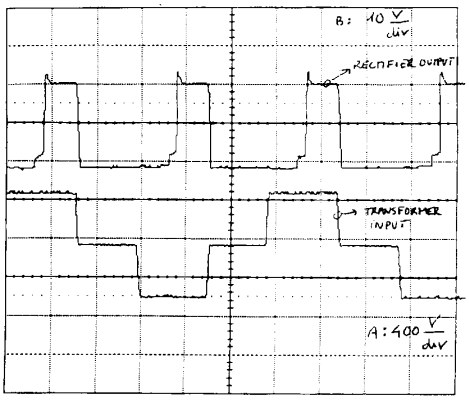

Figure 2. Detail of duty cycle loss when Llk equals 56μH.

3. DESIGN CONSIDERATIONS

The inductance Llk is a critical parameter on the design of the ZVT power section. The selected value, as mentioned before, has been selected as 17 uH Bigger values of this inductance lead to a wider range of ZVT operation. Further, bigger Llk values lead to softer commutations and therefore to a reduction in EMI. Moreover, high values of Llk decrease the effective duty cycle (see figure 2) reducing the possibility of obtaining the desired output voltages. In this case lower transformer turns ratio should be selected in order to obtain the desired output voltage and consequently higher voltage ratings Schottky diodes. Also due to the decrease of the effective duty-ratio the input current has to increase reducing consequently the overall efficiency. Small inductance values lead to the achievement of the ZVT condition at higher current values with the inherent decrease in the overall efficiency. In order to achieve the desired inductance value the transformer has to be carefully designed .In our first design, with only one transformer with turns-ratio 20:1 the stray inductance was 56uH. By splitting the transformer in four transformers with turns-ratio 5:1 each, the total leakage inductance was reduced to 6uH, so an additional external series inductance has been added in order to get the desired 17uH. The transformer is a secondary centre-tap one and water-cooled with the primary series connected and the secondaries parallel connected.

Referring to the dead time for triggering for the lagging switches, this should be equal to ¼ of the oscillating period given by the resonance between the Llk inductance, the capacitance's of the IGBT¨s and snubber capacitance and the parasitic inductance and parasitic capacitance of the transformer. On the other hand, in the leading switches the charge of the IGBT output capacitance can be approximated by a linear charging with a constant current.

The dynamic response has been adjusted in order to have 1kHz bandwidth with reasonable phase and gain margins: 75 deg and more than 10 dB respectively. The control employs an UC 3875 integrated circuit to implement the error amplifier and driving circuits. The block diagram of the controlled converter is given by:

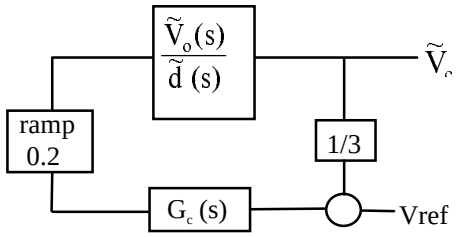

Figure 3. Control block diagram.

Where $\frac{\tilde{V}_o(s)}{\tilde{d}(s)}$ is the transfer fuction of the converter and $G_c(s)$ the transfer function of the compensator, which is given by:

$$T(s) = \frac{3000\left(1+\frac{s}{1600}\right)}{s\left(1+\frac{s}{200000}\right)} \quad (1)$$

4. EXPERIMENTAL RESULTS

Figure 4 shows the voltage and current in the primary of the transformer.

The output voltage ripple is shown in figure 5, it is less than 20 mV. Figure 6 shows the conducted noise at the output of the converter and the limits that define the standard VDE 087A. The theoretical and experimental

transfer function in open loop are shown in the figures 7 and 8 respectively. Finally, line regulation has been tested with input variations ranging from 300V and 390V and has been under all conditions less than 0.06%.

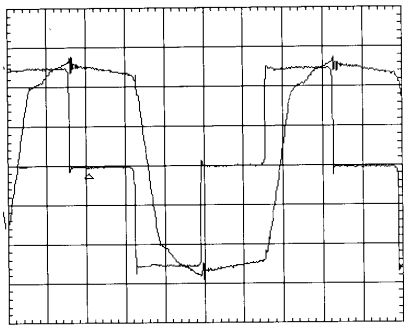

Figure 4. The voltage (200V/div) and the current (20A/div) in the transformer

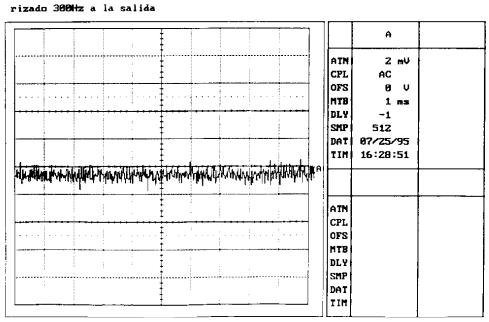

Figure 5. Output voltage ripple.

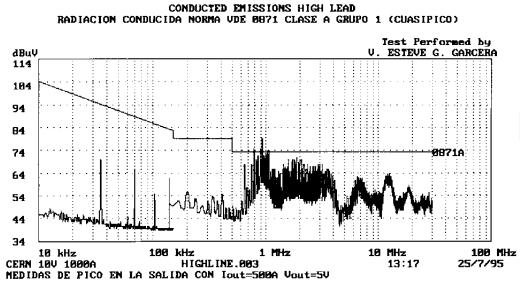

Figure 6. Output voltage noise and limits defined by the normative

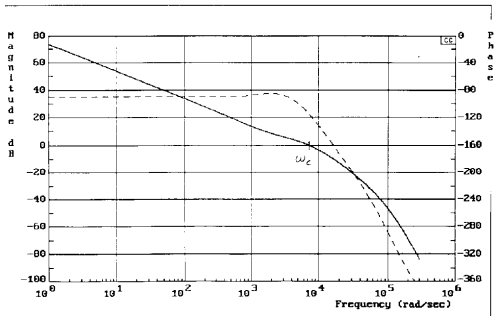

Figure 7. Representation of Aol(s) for the theoretical circuit.

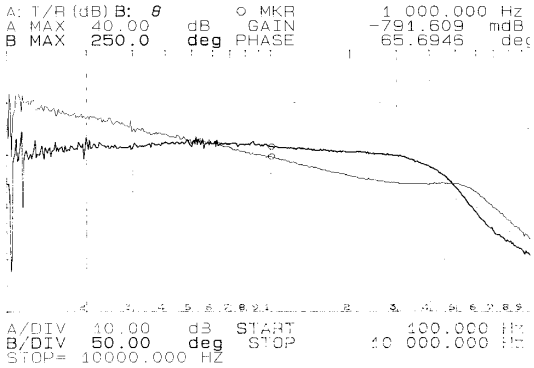

Figure 8. Representation of Aol(s) for the practical circuit implemented.

The efficiency of the converter for 5 and 15V output is shown on figures 9 y 10.

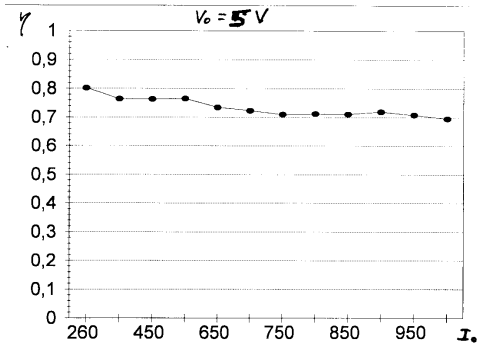

Figure 9. Efficiency at 5V output

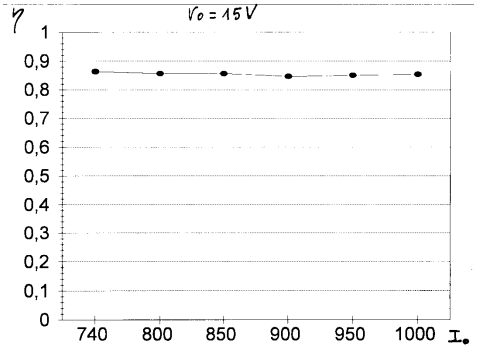

Figure 10. Efficiency at 15V output

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[2] Vlatkov Vlatkovic, “Small Signal Analysis of the Phase Shifted Zero Voltage Switched PWM Converter”, Thesis, Virginia Power Electronics Centre.