THE DAΦNE TIMING SYSTEM

A. Drago, G. Di Pirro, A. Ghigo, F. Sannibale, M. Serio
INFN-LNF, Frascati, Italy

Abstract

DAΦNE is a Φ-factory, presently under construction at INFN-LNF in Frascati. The electron / positron injection in the two main rings is performed through a Linac and an intermediate damping accumulator ring. The DAΦNE Timing System has been developed in the Frascati National Laboratory to synchronize many different devices distributed in more than 100^2 square meters area. The goal is to generate, under control of the general control system, the injection and extraction triggers related to the destination RF bucket in the main rings. All these outputs must have very low jitter. They are distributed to slow and fast pulsed devices such as, for example, Linac, injection / extraction kickers, diagnostic instrumentation and magnets. The timing system generates also the accumulator ring radiofrequency driver and various triggers for the detectors. Components and technologies used, modules description, control software and performances are presented.

1 INTRODUCTION

DAΦNE [1] is a Φ-factory, expected to be completely assembled in the Frascati National Laboratory (LNF) at the end of 1996. It consists of an 800 MeV electron (550 MeV positron) Linac, of a 32 m long damping/storage ring (Accumulator) and of two 100 m long main rings.

The DAΦNE Timing System has been developed in the Frascati National Laboratory to synchronize many different devices distributed in a more than 100^2 square meters area. Goal of this system is to generate, under control of the general control system, all the injection and extraction triggers related to the destination RF bucket in the main rings.

All these outputs must have very low jitter. They are distributed to slow and fast pulsed devices such as, for example, Linac, injection/extraction kickers, diagnostic instrumentation and magnets. The timing system generates also the accumulator ring radiofrequency driver and various triggers for the detectors.

Many different frequencies are involved in the DAΦNE accelerator: they are all generated from two main frequencies: 50 Hz and radiofrequency (around 368 MHz). From these, the other frequencies are derived and/or combined by digital hardware and software control devices. For every frequency it is possible also a phase control and this is performed through the software operator interface.

2 COMPONENTS AND TECHNOLOGIES

The Timing System is set up by more than half-dozen of different boards all designed at the LNF.

The higher frequency signals are managed through advanced ECL integrated circuits by the Motorola Eclinps (ECL in PicoSeconds) logic family [2]. These commercially available components have performances up to 1.1 GHz, very good stability in temperature and good compatibility with the other ECL logic families. Digital programmable delay components with steps of about 20 psec are included in this logic family: this is a flexible way to manage high frequency signals clocking flip-flops and latchs.

The lower frequencies signals are managed by TTL/CMOS logic family integrated circuits. VME bus interfaces [3], to the DAΦNE control system, permit to generate signals with different frequencies and phases from the software. These derived frequencies and all the enable/disable control bits are still locked with the master frequencies generators.

The shift in phase, both for the higher and lower frequencies, can be set by the software. This is done without missing trigger, i.e. in one revolution period. The synchronization between the high level software and the master frequency is performed through the low level timing software based on the AT&T DSP1610 [4], a 16 bits digital signal processor that is clocked at 80 MHz and can be used also as single-chip controller.

The distribution to local and remote devices is performed through 8-wires RS-485 synchronous connections transmitting 1 Megabit per second; with this speed it is possible to connect all the interested area without any auxiliary repeaters.

At crate level the synchronous transmission of the commands is made in compatibility with the VXI specification [5] through a local bus which uses the A and C rows of the lower 96 pins VME connectors.

In this way, it is possible to avoid the VME handshaking in order to minimize the jitter when the commands are released, and it is possible to simplify the receiving interface.

Large part of the printed circuit boards are designed with controlled impedance techniques, i.e. considering the wires as microstrip lines.

The PCB dielectric is FR4 (a low cost insulator) and the PCB conductors are copper based. Almost all the boards are multilayer, with up to eight layers; the CAD for the PCB design used can reach one thousandth of inch of precision in the trace layout.

3 MODULE DESCRIPTIONS

Many different frequencies are necessary in the DAΦNE accelerator: they are all generated from the two main frequencies: the 50 Hz, that is the external power supply frequency, and the RF (the Radio Frequency at around 368 MHz), that is the two main ring cavities frequency.

The first module is the master 50 Hz board: this is a device which, from the external 50 Hz frequency of the 220 Volts power supply, generates four master 50 Hz signals locked in phase with the external reference. This is made through a 74HCT4046 PLL (Phase Locked Loop). The four 50 Hz signals are 90 degree delayed each other and they are called Ø1, Ø2, Ø3 and Ø4. The 20 msec time slot is the discrete time unit which any timed operation in the accelerator must be performed in. Having four delayed timing signals is useful to timing slow devices on different 5 msec time subslot trigger. For example the injection kicker is charged itself on phase Ø1 and discharges itself on phase Ø4.

The second module is a fan out board that can accept four different TTL or differential ECL signals and fans them out through 4 TTL and 4 differential ECL output port for each input. The signals can be synchronized by an other external clock with frequency up to 100 MHz. This module is replicated in different zones of the plant to give remote triggers to many devices. Typically this module is useful to merge the low frequencies (50 Hz and 1 Hz) with one of the higher frequencies (RF/120 or RF/40).

Taking the main RF signals from a commercially available synthesizer, the fiducial generator module simply divides the frequency by 120 that is the harmonic number of the DAΦNE main rings. At full current it is expected that the machine will have 120 electron bunches and 120 positron bunches. The fiducial generator module is a RF/120 oscillator that give a trigger reference useful to label a bucket as the first bucket. The output signal levels are differential ECL and NIM.

The RF divider and bucket selector (or "fast timing") is a programmable module; it takes the RF as input and divides it by a dip-switch programmable value. In this way it is possible to produce three useful frequencies that are RF/120, RF/40 and RF/5.

All the modules accept the fiducial reference as input to synchronize the bucket count each other. To select the bucket the boards accept, through the local bus, a bucket number that is interpreted as a phase shift equal to the RF period times the input value. The phase shift is very critical and the error must be minimized to insure correct injection time to every bunch. The output levels are differential ECL and NIM.

The RF synch and fan out gives better RF synchronization and fans the signals out by four with differential ECL and NIM levels.

The connection with the control system is made by the state word dispatcher module that is provided by a VME bus A16 / D16 slave interface. This VME board is designed around an AT&T DSP1610 processor that makes very flexible the timed exchange of information between the timing system and the DAΦNE control system. This module takes as input two 50 Hz signals (Ø1 and Ø2) and it is provided, besides the VME interface, with a 1 Mbit/s RS-485 serial transmitter unit to broadcast the state word, a 31 bits pattern that contains the bucket number and the enable/disable bits for all the timed devices. The state word can be renewed every 20 msec and it is read from the control system that keep memory sequences of them stored in disk files (see Table 1). This module has also other interfaces as the local bus interface modelled on the local bus VXI specification, the JTAG interface to debug the software module and an auxiliary serial interface for remote serial connections, remote abort and remote reset.

Table 1 - DAΦNE timing state token

TOKEN	DESCRIPTION	APPLIES TO
LTO	Linac triggers off	Linac
LSB	Linac stand by	Linac
LSP	Beam from Linac to Spectrometer	Linac
LBT	Beam Linac to BTF	Linac
LAC	Beam Linac to Accumulator ring	Linac
AST	Accum.ring stored beam	Accumulator ring
AEX	Accumulator extraction	Accumulator ring
AMR	Accumulator extraction and main ring injection	Accumulator ring
EMS	Electron main ring stored beam	Electr. main ring
PMS	Positron main ring stored beam	Positr. main ring
VMP	Pulsed Magnet triggers	Various
VCA	Calibrations	Various
E+/E-	Electron/Positron	All
BCK	Bucket number selected	All

A twin module of the dispatcher is the state word receiver that receive remotely the state word and a 50 Hz phase trigger through the RS-485 serial link. This VME slave module is based on a DSP1610 and writes the state word to the local bus. The receivers are located in racks close to the devices to be controlled. Other modules have been designed in Frascati National Laboratories to receive the state word from the local bus and to execute the timed commands, for example to generate frequencies lower than 50 Hz and controlled in phase and duty cycle.

4 CONTROL SOFTWARE

The DAΦNE timing system software is composed by the low level software stored on eproms and by the high level software stored on the control system mass memory; they have assigned different tasks.

The low level software is a real time code that runs on the AT&T DSP1610 and it is written in assembler language. It consists of the state word dispatcher program that runs on one module and of the state word receiver program that runs on up to 128 connected modules. The dispatcher software is designed as a 4 state finite machine that switches from a state to the next one every 5 msec according to the 50 Hz input level signals phase Ø1 and phase Ø2. This finite state machine generates a two bits semaphore and puts it in the VME interface register. In this way, it is possible to synchronize the data flow from the control system. On the green light the control system writes the current 31 bits word, on the red light it retrieves the new word from a sequential table, checking an external condition and waiting.

The receiver real time software is also written in DSP1610 assembler, it is a two state finite machine based on the 50 Hz phase received from the RS-485 serial link together with a state word. It performs a delayed and timed writing on the VME interface and on the local bus to activate the command execution with a low jitter.

The high level software runs on commercial Apple MacIntosh computers and on special MacIntosh machines with a VME interface. Large part of the code is written in LabView, a language developed by National Instruments.

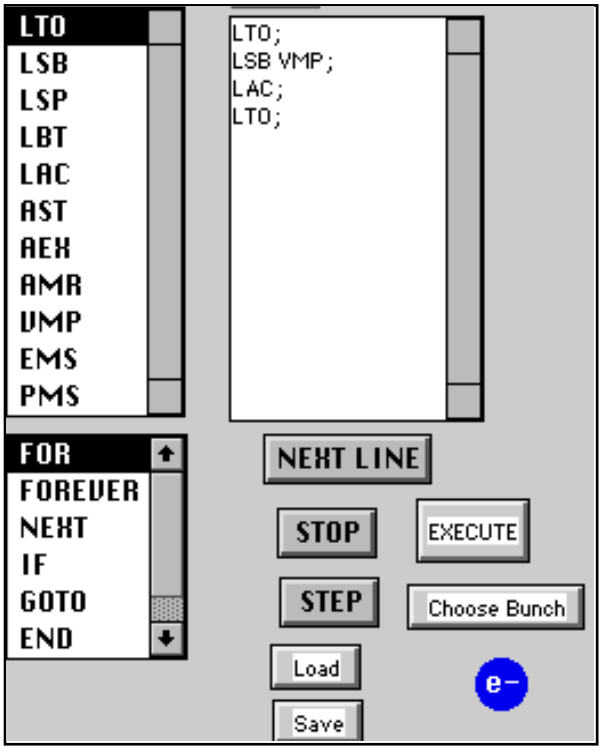

Figure 1 : Development of timing sequence.

The main task of the high level software is to create, to edit , to store and to retrieve different table files. These data are used for different injection and/or extraction schemes or for test and calibration purposes.

5 PERFORMANCES

The performances of the system have been measured in the laboratory, the main goals have been, at low frequency, to minimize the jitter on the remote distribution of state word, and, at high frequency, to minimize the displacement of the phase shift relatively to the bucket chosen.

Regarding to the first test, all the transmission chain of the state word from the operator interface to the remote devices has a measured jitter of 500 nsec without transmission errors over 128000 patterns.

The high frequency tests have been done in the laboratory using the automatic test set shown in Fig. 2.

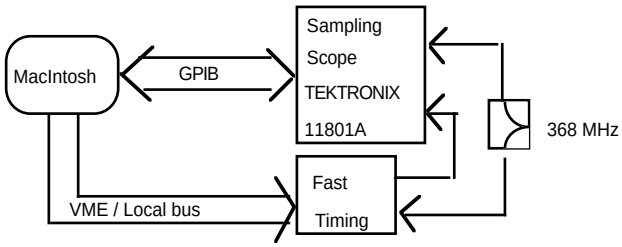

Figure 2 : Bucket phase shift test set.

Through the VME and the local bus interfaces it has been possible to modify the programmable delay in the fast timing module to best fit the desired output triggers. In this way it has been possible to reach for the 120 buckets selector a standard deviation of 1.6 picosec for the displacement from RF.

6 CONCLUSIONS

It has been presented an overall description of the DAΦNE timing system, that has been installed during the April 1996 on the DAΦNE complex.

All the laboratory tests are completed and the integration with the other accelerator subsystems is in progress.

REFERENCES

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[2] "Motorola ECLinPS Data", Motorola Inc., 1991.

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[4] "WE DSP 1610 Digital Signal Processor Information Manual", AT&T Microelectronics, 1991.

[5] "VXI bus System Specification revision 1.4", VXIbus Consortium Inc., 1992.