CONTROL SYSTEM FOR ACCELERATOR WITH DISTRIBUTED INTELLIGENCE BASED ON A "FAMILY OF SMART DEVICES".

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Abstract

Presented approach for construction of accelerator control system is based on a few basic ideas: 1) system intelligence responsible for the handling of the control tasks should be spread as even as possible; 2) as much as possible feedback control loops should be closed locally and digitally; 3) interfaces for interconnection of the system levels should be as standard as possible; 4) all components of the system should be control oriented and 5) price/performance ratio should be optimized. "Family of Smart Devices" based on digital signal processors and RISC-based microcontrollers forms hardware core for the components of the system. An idea of "shared memory" is used for construction of low level software and access to the controlling object from a top level of the system. Standard high level software for control database and man-machine interface support are used.

1 INTRODUCTION

The dream of universal tools for different control applications is taking on new life with a recent appearance of low cost high performance microprocessors and new architectural solutions. In large experimental installations as particle accelerators control tasks are very complicated and could be splitted up between several processes with different control tasks. According to this division different types of hardware and software are used in the same system. It is resulted in very heterogeneous in software, hardware tools for system creating and maintenance. Time of the system development increases and price of control system reaches 20% of overall price of a project [1].

New approach is a further attempt to simplify and to be a help in a sever process of control system development. It is based on shared memory concept as general architectural principle that defines structure of application software. We expect to reduce complexity of application software due to development of this idea. To provide maximum hardware support the family of smart devices has been designed on the base of digital signal processing (DSP) technology [2,3].

Designing of smart devices become possible today due to the progress in electronic technology. The progress is reflected in dramatically increasing of microprocessor performance, reducing of the prices, wide spread of such devices like FPGA and increasing of popularity and accessibility of DSP technology.

Our approach is based on the belief that:

- control handling intelligence should be uniformly distributed throughout the system;
- feedback control loops should be closed locally and digitally wherever possible;
- interfaces connecting system levels should be as standard as possible;
- all system components should be control oriented and
- system price/performance should be optimized.

Homogeneity of hardware and unification of software and special software features will decrease difficulties of system creating and maintenance.

2 GENERAL ARCHITECTURE

Idea of shared memory implemented in smart devices could be complited in the framework of the common general architecture - distributed multilevel hierarchical system. The Open Systems concept requires that interconnection between components should be made via the standard interfaces only. Due to a high level of scalability smart devices could cover middle and low levels of multi-layer control system. On the figure 1 example of possible architectural solutions with smart devices is shown.

3 SHARED MEMORY FOR CONTROL

Application of shared memory is a common way for many existing multiprocessor computational systems. We propose to implement this approach specially for control application. According to this approach, high level application software knows nothing about structure of low level hardware. Application software operating on certain level accesses right to the shared data reflected in the memory of the level. Moreover, application software does not check data integrity, and could be sure that data are ever corresponding with current state of control object. These data are the result of software operation on the lower level formed by smart devices. The data are transmitted by task oriented fieldbus, which support data integrity in the memory of the higher level of the system. On the first stage of designing we use MIL-STD-1553B interface. But conceptually our approach is independent on the fieldbus type. Due to architectural features we follow the statement that all the data reflecting the state of control object are processed and transmitted for storing and supervising with the rate of its physical generation. And vice verse, during the direct control operation, the system generates the action, writes it to memory and forgets, because it could be sure that

action will influence in time in right place. It is necessary to know only a real physical nature of receiving and transmitting (controlling) signals.
By using shared memory model we try to avoid message-passing method of data exchange between subsystems in spite of high popularity of this method. Very often message-passing mechanism is observed as integral part of multiprocessor approach. At the same time the use of message-passing to link the microkernel with the rest of the OS is the architecture's major drawback [4]. The architecture slows the system down, loads the network and data flows are full of service information surrounding message body. One of the alternative approach was recently presented under project Libra by Digital Equipment Corp. [5]. According to the project the alternative to asynchronous message-passing in distributed system will be the remote procedure call. Our approach of shared memory ensures dynamic control and loading of procedures (processes) and true multiprocessor operation oriented on the control problems. The general structure of software support is shown on the figure 2. The regions of memory 1~.. N~, which are placed in subsystems are mirrored to the 1.. N regions of host level of control system. The destination of memory sharing is to close mechanism of data exchange and structure of hardware. Instead, the process of control is realized in data manipulating in regions of shared memory. The following principles should be implemented due to the shared memory approach:
- to allow application programmers to keep up away from the concrete hardware structure of control system and to have centred on control object features;
- to provide current set of operational parameters reflecting the state of control object to man-machine interface;
- to ensure transparent and simple access to data and program codes for global and local control algorithms.

4 APPLICATION OF DSP TECHNOLOGY

Modern technology of digital signal processing has received powerful impulse with growing popularity of DSP technology and wide spread not only for traditional military applications but in consumer, control and telecommunication products. It was resulted in DSP IC market growing more than twice as fast as the several semiconductor markets [6].
High computational performance, additional on chip peripherals and other advantages of DSP ensure us an ability to establish even distribution of intellectual resources. Modern algorithms for data processing and control have been implemented. Well known that, tuning and controlling of particle accelerators are expensive and time consuming. Two typical scenarios for the problem of RF linac control could be pointed out: beam transport and RF system tuning. Nonlinear nature of the dynamical process necessary to control poses major problems for automated tuning and control. The result is constant and expensive monitoring of human operator. In recent years with different scale of success modern control theories have been applied to the modern control systems. As a rule these attempts are implemented in high level software and serve only for processing slow general algorithms with time constant about a few seconds or mseconds. This approach requires centralized CPU with very high performance and wide networks for data flow with high loading. It is a result of that front-end subsystems do not perform control action. In many cases VME based front-end subsystems with very high performance are used not for control as is but mainly for real time operational system support and partially for implementation of control algorithms, so main part of front-end intelligence is spent for OS support but not for control.
Our approach allows to implement modern control algorithms in low level micro software of DSP processors. So, it will be possible to reach system's reply time for local feedback loops as few hundred mkseconds [7]. In comparison with traditional architecture we are decreasing the loading of top level and volume of data flows between up and down levels.

5 CURRENT RESULTS

Systems based on ideas described above could be used in following applications: distributed control systems for complex experimental installations; systems for data acquisition and processing with low and middle data rates; industrial automation; stand alone industrial controllers.
On the base of described hardware and software approaches computer control system of industrial accelerator CWELL 0.6/6.0 have been designed and implemented [8]. This accelerator consists from one CW section loaded by one klystron with operational frequency 2450 MHz and 20 kW of output power. Output energy of continuos electron beam is 0.6 MeV and output beam power is 6.0 kW. The structure of the control system is shown on figure 3.
Performance of one smart device is quite enough for implementation of all hard real time algorithms. Direct digital feedback loops of high voltage stabilizing and rf-power stabilizing are implemented. The PC-compatible computer is used for man-machine interface support and storing of operational data.
According to the future projects of our laboratory, two sections prototype of industrial accelerator will be used as injector to the electron linac with high power output beam. Therefore all ideas and technical decisions adopted in industrial accelerator control system will be used for developing control system of future electron linac. This linac will be based on equipment of racetrack microtron injector [9]. This injector is under operation now and is controlled by the computer system [10,11] which will be upgraded on the base of our approach.

6 CONCLUSIONS

Our approach for control systems construction will fill a current void between high-cost high-performance crate based systems and low-price low-performance PLC based systems. We believe our scaleable architecture and original hardware devices (e.g., our smart devices family) supported by software can fill this void. With our smart devices family we will not only construct control systems for research accelerators but also for time critical hard real-time applications, industrial processes, generic data acquisition tasks, and so on.

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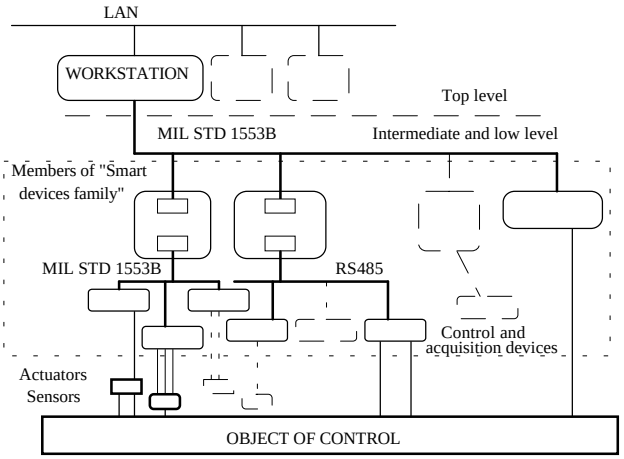

Figure 1. Location of the smart devices family in standard control system architecture.

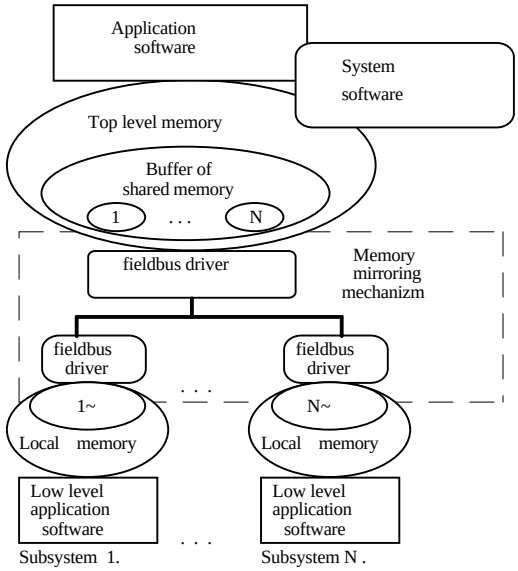

Figure 2. Structure of software with shared memory for control applications.

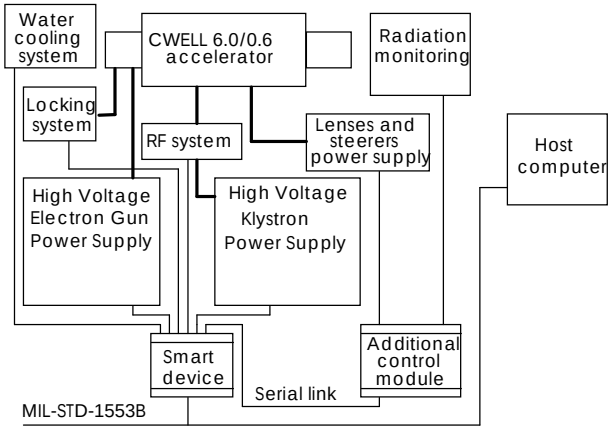

Figure 3. Structure of industrial accelerator control system.