THE NEW TIMING SYSTEM FOR THE ELETTRA LINAC

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Abstract

Embedded in the new Control System under design for the ELETTRA LINAC [1], there is a new Timing System, which will provide the necessary set of delayed trigger pulses for each power plant of the LINAC. To obtain high stability of these trigger pulses, a set of new delay boards were developed in-house. In doing so, also the interlock functions will be hardware implemented. Furthermore the new software, for both the low-level processes and the user interface, greatly contribute to a fast and reliable operation.

1 BACKGROUND

1.1 The present LINAC Control System

The LINAC plant was a turn key device delivered by CGRMeV, including also the Control and the Timing Systems. The LINAC Timing System was later integrated in the Machine Timing System, which was developed in-house.

The Control System presently in operation at the LINAC is composed of one Local Process Computer (LPC) and four Equipment Interface Units (EIU). One of the EIUs generates the trigger pulses for the LINAC sections (9 in total): each section needs a set of 5 pulses to operate the RF system. Each set of pulses is delayed with respect to the previous set in order to have on each LINAC section the optimum accelerating phase.

Presently, each section is fed by 5 different delay boards as each board generates 9 delayed replicas of the same type of pulse.

1.2 Main problems of the present LINAC Timing System

Some seriuos problems jeopardize the correct and reliable generation of the pulses.

The pulses suffer from a not negligible jitter (<10ns). As a consequence, the otpimum accelarating phase cannot be maintained which leads to energy fluctuations. The major part of the jitter is due to the 83.3 MHz clock which is not in phase with respect to the Start Injection signal (SI). Furthermore it is badly distributed to the delay boards. The SI signal comes from the MACHINE Timing System and is in phase with the 500 MHz generated by the master RF oscillator.

The interlocks which should prevent that the RF system operates under dangerous conditions, are implemented via software on the EIU processor. Therefore reaction times are not deterministic and potentially dangerous situations may arise.

The Control System of the LINAC is not integrated in the Machine Control System. Presently the LINAC operation is controlled by means of dedicated terminals located in the LINAC Control Room.

2 SYSTEM REQUIREMENTS

The main requirements of the new LINAC Timing System (LTS) are:

- to provide jitter free pulses (<1 ns);
- to operate properly in a noisy environment;
- to assure reliable interlock operation;
- to allow flexible setting of the pulse set-up;
- to minimize the connection cables;
- to be fully integrated in the Machine Control System.

Due to the very noisy Electro-Magnetic (EM) environment of the LINAC, the LTS has been designed to minimize disturbances due to noise.

Special attention has been payed to design a flexible and simple User Interface.

The minimization of the number of connection cables avoids mis-connection and improves noise rejection.

To facilitate LINAC maintenance one single board generates all the pulses for one section. As a consequence any Trigger Board can be substituted without stopping the whole plant.

3 DESCRIPTION OF THE SYSTEM

The LTS is composed of a single Clock Board, up to 10 Trigger Boards (fig. 1) and a single Interlock Board (to be developed). The Clock Board (CB) generates the 50 MHz clock for all the Trigger Boards (TB). There is one TB for each section of the LINAC. Each TB has eight output channels; five of them are actually used for the LINAC section, three are spare.

All the boards are housed in a VXI crate equipped with a 68030 CPU. The VXI crate gives high noise immunity, high backplane resources and a larger board area.

The 50 MHz clock and the Start Injection SI signal (10 Hz) are distributed to the TB via the backplane lines of the VXI crate. This feature enhances the global system reliability reducing the number of cables.

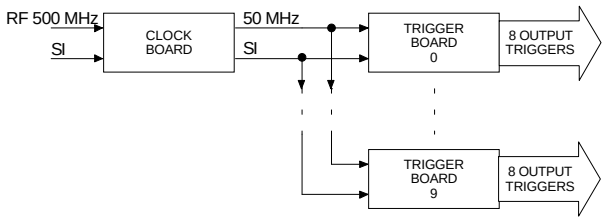

Figure: 1 The new LINAC Timing System.

Each trigger output is optically converted and sent to the LINAC section via a fiber optic.

The system design was entirely developed in OrCAD environment [3] (Schematic Entry, Digital Simulation and Printed Circuit Board (PCB) layout). A wide use of Field Programmable Gate Arrays (FPGA) has been done in order to improve system flexibility and to minimize the discrete Integrated Circuit count. The Xilinx FPGA and EPLD families were chosen [4] due to their high density, high clock speed and ease of programming via on-board EPROM. The Xilinx development system is integrated with OrCAD. The resulting uniform development environment gives us all tools of interest and speeds up the design development.

4 CLOCK BOARD

4.1 Design

The CB receives as input the 500 MHz RF and the SI signal. The RF is divided by 10 by means of an SP8680A divider (Plessey). To avoid jitter between the generated 50 MHz clock and the low frequency SI signal, the divider is reset at each SI occurrence.

4.2 Hardware

Particular attention was paid to the 500 MHz section of the board (from the input connector to the output of the divider). The high speed components were carefully placed closed together.

The 50 MHz clock (ECL level) is distributed to the TB via the dedicated ECL lines of the backplane. The SI signal is distributed via a TTL line of the backplane.

Attention was paid to the impedance matching of the lines that carry these signals through the board up to the backplane lines.

5 TRIGGER BOARD

5.1 Design

The TB is a VXI board with 24/16-bit addressing/data capability. One TB generates all the triggers necessary for one section of the LINAC.

Actually this board can be considered as a programmable pattern generator: each trigger corresponds to the scan of a single bit of a fast memory. A 16 bit counter, running at 50 MHz, scans all the addresses of a 64Kx8 fast SRAM (UMC UM61512, access time=15 ns). By means of High Level (UNIX) software routines we can modify the memory locations to obtain on each output the desired binary sequence. Although we have a 20 ns clock period, we obtain a 10 ns resolution latching the output byte either on positive or negative edge of the 50 MHz clock. Like the divider in the CB, the counter is reset at each SI occurrence in order to avoid jitter between the SI and the output pulses.

The memory programming pattern is first written to a mirror memory (another 64Kx8 UM61512), directly accessible from the VME bus. Then the whole mirror memory content is copied to the fast memory. This procedure allows not to interfere with the scan of the fast memory while changing the output pattern from the High Level processes. After each “fast scan” cycle, the operator can copy the mirror memory to the fast one (while the TB is waiting for the next SI).

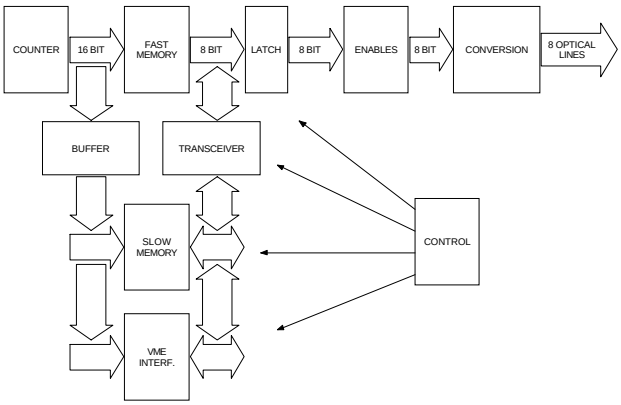

Figure: 2 The Trigger Board.

A state machine has been hardware implemented to perform the above mentioned operations (fig. 3).

A section of the TB (Enable section) provides the following safety controls on each output:

- compliance of the time priorities between triggers;
- automatic trigger generation (within specified time interval) on memory output fault;
- inhibition of the output after first pulse occurrance (to avoid multiple pulses during one SI period);
- fast inhibition of the appropriate outputs due to interlock intervention.

The interlock signals are received on the backplane P2 connector. A dedicated decode logic analyses the interlock signal status and generates the appropriate inhibition signals.

All data exchange between the TB (read/write of the memory, read/write of the registers, write of the commands) and the master CPU are done via a VME interface, also in-house developed on a FPGA.

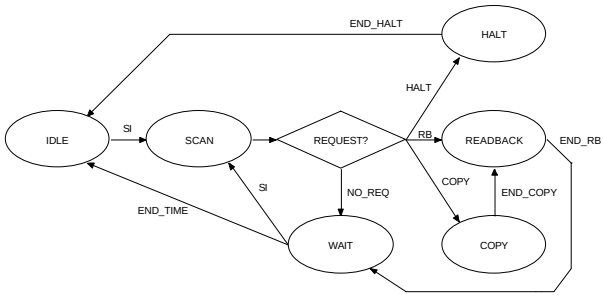

Figure: 3 The state machine of the Trigger Board.

5.2 Hardware

A four layers PCB was realized. The first internal layer is a ground plane, while the second one is a power supply plane. This gives low impedance paths both on ground and power, avoiding voltage drops and consequently noise margin reduction.

All signals on the board are at TTL levels. The selected logic family is ACT, due to its velocity and low power consumption.

The 50 MHz clock is received from the VXI connector by an MC10H125 (ECL to TTL converter). It is distributed through the board by a 50 Ohm coaxial cable in order to avoid the generation of EM noise on other lines of the board.

Three Xilinx FPGA XC3130 and one Xilinx EPLD XC7336 are used to implement four logic sections:VME Interface, Memory Control, Enables and Interlocks. This gives us great flexibility in the implementation of the board functionality and assures the board to be flexible for future upgradings.

All the outputs are electro-optical converted before being sent to the LINAC plant. High bandwidth leds are used: the 1A301 ABB HAFO model has been chosen (350 MHz Bandwidth, 1 ns rise time)

6 INTERLOCK BOARD

This board pre-processes all interlock signals from the field, 3 for each LINAC section (vacuum, high voltage and one spare). With a maximum number of 10 TB, a total number of 30 interlock signals have to be distributed. Due to un-sufficient number of backplane lines, the distribution is accomplished by encoding the signals on 5 lines.

7 TESTS

7.1 Clock Board

One prototype of the CB has been successfully tested in our laboratory. The performances of the board are in good agreement with what we expected.The divider and the generated 50 MHz clock showed a very low jitter (≈200 ps).

We had some problems due to the 50 MHz clock path through the board. 50 MHz noise has been measured on the power supply lines. An improved filtering of the power supply lines (C-L) solved the problem.

The differential transmission of the 50 MHz clock via the backplane shows good performances: on the TB, after backplane distribution and ECL/TTL conversion, we have measured sharp edges (<1ns) and very low ringing (<2%).

7.2 Trigger Board

The TB is currently under test. During this phase, the on-board programmability of the FPGAs allows us to immediately evaluate the modifications applied.

The newly developed VME interface FPGA is working and the whole board will be tested by July, this year.

8 SOFTWARE

The software developed for the control of the new Timing System module, is based on the Microware OS/9 Real-Time Operating System. A device driver has been developed to support all the functions of the new board.

During the startup phase, a low level process is responsible for the system configuration.

Just after the startup the system goes in stand-by mode waiting an operator command. The operator is allowed to change the delays and to enable or disable a section. A background running process periodically checks the system status.

A specialized set of RPC calls has been developed to allow the communication between the field and the presentation layer; these calls are based on the CERN NC/RPC package.

A specialized GUI has been developed and as any other control panels of the ELETTRA Control System it is based on the X11/Motif standard.

9 CONCLUSION

The new Linac Timing system has been presented: with a carefull design of the new trigger boards a global improvement of the system will be achieved which will contribute to a more reliable Linac operation.

REFERENCES

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[3] Xilinx: The Programmable Logic Data Book, 1994