

Synchronizing System with Intelligence *,
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PAL-POSTECH - The operation of the PLS accelerator requires that a large number of events occur following the instruction with a relatively high degree of precision. To orchestrate ingeniously these events an intelligent synchronizing system is required. The rf system of the storage ring operates at 500.082 MHz which provides the fiducial trigger and a divide by harmonic number divider generates the revolution clock on SR, which is the main trigger pulse of the PLS accelerator complex. For the control of bunch by bunch and single bunch operation, system specification is satisfied with accuracy less than 100 ps and resolution as 2 ns. H/W system is composed of four VMEbus based modules. To provide remote control from upper-layer computer it is networked to console computer through Ethernet and down loaded the program to local processor. The control is done by the real-time task resident in the local processor. Then event occurs, the trigger interface generates an interrupt, sub-processing task is activated and executes synchronously the instruction.

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