A VERY FAST KICKER MAGNET
- A NEW APPROACH -

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Abstract

A fast kicker has many applications in an accelerator technology. The rise time of a state of the art kicker is currently of the order of several tens of ns. Our design goal is to develop a kicker with a trapezoidal shape of a rise time of 10 ns, and a flat top duration of longer than 100 ns. The rise time is determined by a power supply and a magnet.

With a view to developing a power supply which can obtain an output current with a rise time of 10 ns and a peak of 10 kA, a new pulse-circuit using magnetic switches and a pulse forming line has been designed. It would be possible to adapt a magnetic switch with a hold-off period of less than 100 ns by dividing a pulse forming line into multiple pieces and by charging each circuit in parallel.

Simulations showed the adaptability of magnetic switch respecting the pulse forming line divided into multiple pieces. In experiments using a 1/20 scale model of the final system, the output current with a rise time of 25 ns and a peak of 600 A was achieved. It would be possible to improve the rise time by increasing a core-reset current.

1 INTRODUCTION

Magnetic switches have been used mainly in power supplies for gas lasers[1]. In pulse compression technology, use of several magnetic switches enables an output current with a short pulse duration of less than 50 ns and a peak of several kA to be obtained. The switch has the great advantages of long lifetime and high-repetition-rate operation which discharge-type switches, such as a spark gap switch, lack. The switch has these advantages because it has no consumption parts, such as electrodes[2].

A kicker requires an output current with a long pulse duration and a fast rise time. A magnetic switch has a feature that size and inductance are increased with the required hold-off period which is defined as a period from the beginning of applying voltage to the switching on. In order to use a magnetic switch with a pulse forming line (PFL), the pulse charge duration should be as short as possible so as to reduce the inductance of switch and therefore the rise time. However, charging a PFL in a short period is undesirable from the viewpoint of an output current with a uniform flat top.

To solve the problem, a pulse circuit with a PFL divided into multiple pieces was designed. The characteristics of the improved pulse circuit were simulated, and model experiments using small-scale magnetic switches were carried out.

In this paper, simulated and experimental results are summarized, and the adaptability of the magnetic switch to the fast kicker is discussed.

2 DESIGN AND SIMULATIONS

A basic pulse circuit for a kicker magnet system is shown in Figure 1. A rise time t_r of output current (10-90%) is approximated using a time constantτ, as shown in the following equation:

$$\tau_\rho = 2.2\tau = 2.2(L_s + L_c)/(Z_0 + R) \qquad (1)$$

where L_s : Inductance of switch L_c: Inductance of magnet coil
Z_0 : Characteristic impedance of PFL R: Matching resistance

Figure 2 shows dependence of the rise time on the impedance Z_0 and the total inductance L_t ($=L_s+L_c$). An initial voltage to obtain 10kA output current is simply given by the equation of $V = 2Z_0I$. Taking account of insulation, the maximum voltage across the switch should be 50 kV. Therefore, the figure suggests that the design should be conducted under the condition of $Z_0(=R)$ of less than 2.5 ohm and L_t of less than 22.5 nH.

Assuming that the kicker magnet is excited using four coils in parallel and the switch inductance is less than half of total one, the upper limit of L_s must be less than 45 nH.

The following estimation shows that the above specification is reasonable to design a magnetic switch.

Size of cores in a magnetic switch depends on voltage and hold-off period, as shown in the following equation:

$$(r_{out} - r_{in})\, w p_f = \int V dt / \Delta B \qquad (2)$$

where r_{out} : Outer radius of coil r_{in} : Inner radius of coil
w : Axial length of coil p_f : Packing factor
ΔB : Maximum magnetic flux density

The magnetic switch inductance at the core-saturation is described by the following equation:

$$L_{sat} = \mu_r^{sat} \mu_0 w \ln(r_{out}/r_{in})/(2\pi) \qquad (3)$$

where μ_r^{sat} : Relative permeability of saturated core
μ_0 : Permeability in vacuum

Assuming that amorphous cores are used for magnetic switches under the condition of 100 ns hold-off period and a 50 kV voltage, the optimum core size, which enables the switch inductance to be about 40 nH, can be obtained from equations (2) and (3).

From the above estimations of magnetic switch specifications, circuit parameters were determined as shown in Table1. Figure 3 shows a schematic of a pulse

circuit with a PFL and a magnetic switch. The influence of charging PFL in a short period was estimated using a conventional code for circuit simulation (Micro Cap-V).

Figure 4 shows voltage and current waveforms simulated under the condition of 200 ns pulse-charging period. The voltage on each side of PFL is not in agreement with each other during a charging period. And large fluctuation appears in the top of output current. This suggests that usual PFL can not be charged uniformly under the condition of a short pulse duration, and the magnetic switch with a short hold-off period can not be adapted.

Figure 5 shows a schematic of a PFL pulse-charging circuit, which was modified to overcome the disadvantage of the pulse circuit in Fig.3. The PFL with a propagation time of 120 ns is divided into three pieces, and each PFL unit is charged in parallel. As a result, the voltage distribution along each PFL is expected to be uniform in a charging period of 100 ns.

Figure 6 shows simulated results for the circuit in Fig.5. The voltage on each side of the PFL is in good agreement during the PFL charging period. The flatness of output current is improved.

From these results, it is confirmed that the method of multiple-dividing PFL enables the charging period to be reduced without degrading the shape of the output current.

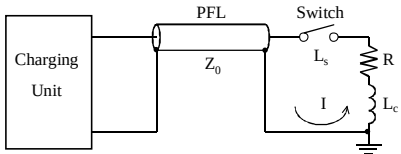

Figure 1. Basic pulse circuit for a kicker magnet system

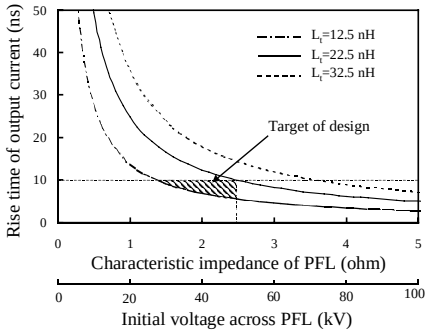

Figure 2. Dependence of rise time on impedance and total inductance

Table1. Circuit parameters for simulations

PFL: Characteristic impedance	Z_0	2.5 Ω
Propagation time	T	60 ns
Current pulse duration	I_1	200 ns
	I_2	100 ns
	I_3	120 ns
Storage capacitance	C_1 (= C_2)	24 nF
Magnetic switch inductance	L_s	10 nH
Kicker magnetic coil inductance	L_c	12.5 nH
Matching resistance	R	2.5 Ω
Input voltage	V_0	50 kV

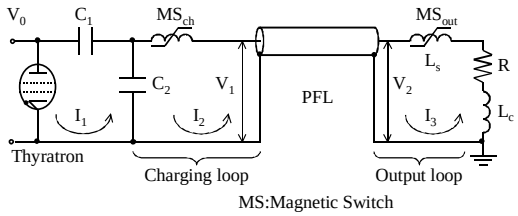

Figure 3. PFL pulse-charging circuit

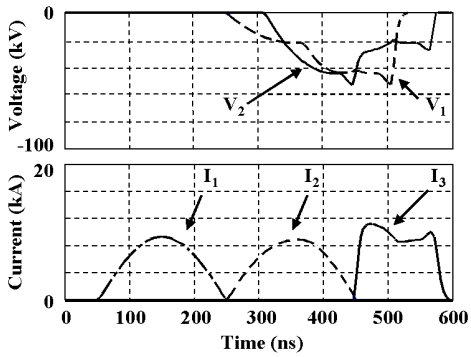

Figure 4. Simulated results of PFL pulse-charging circuit

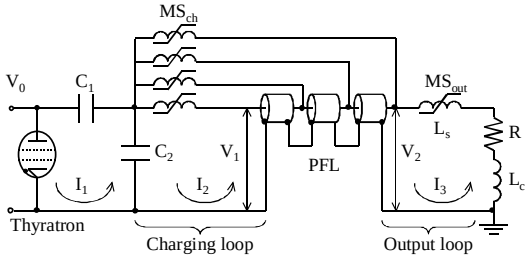

Figure 5. New type of PFL pulse-charging circuit

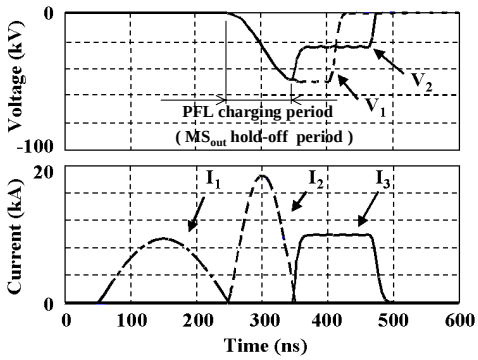

Figure 6. Simulated results of the new circuit

3 EXPERIMENTAL RESULTS

3.1 Experimental circuit

Based on the simulations, experiments to confirm characteristics of the newly designed circuit were performed. Cobalt-based amorphous alloy (Toshiba AMB) cores were used for the magnetic switches to be operated at the frequency of 25 MHz, which is equivalent to the current rise time of 10 ns[3]. A schematic of the magnetic switch is shown in Fig.7. Standard cores with a

diameter of 60 mm and a depth of 11 mm were used for the magnetic switch MS_{out} in the output loop. The same cores were used for the magnetic switch MS_{ch} in the charging loop. It is important for each MS_{ch} to be switched on precisely with a constant delay time, because the current charging each PFL unit should be balanced. The number of cores was adjusted to do this.

Table2 shows the experimental conditions. The maximum voltage of 15 kV was determined by the upper limit of the thyratron. The PFL was manufactured by connecting four 50 ohm coaxial cables in parallel, and divided into three pieces as shown in Fig.5.

3.2 Results

Figure 8 shows the typical current waveforms measured in the pulse-circuit. The output current with a peak of 600 A and a rise time of 25 ns was observed. The waveform of PFL charge current I_2 indicates that each PFL is charged in a period of approximately 100 ns, which is equivalent to the flat top duration of output current. In the output current waveform I_3, considerable amount of ripples is avoided. This result shows the positive effect of multiple-dividing PFL, which is predicted by the simulations.

The initial slow slope of output current I_3 is due to a leakage current of the magnetic switch MS_{out}. The amount was found to be larger than the initial estimation.

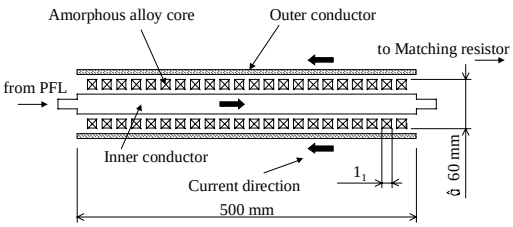

Figure 7. Schematic of the magnetic switch

Table 2. Experimental conditions

PFL: Characteristic impedance	Z_0	12.5 Ω
Propagation time	T	60 ns
Storage capacitance	C_1 (= C_2)	4.7 nF
Matching resistance	R	12.5 Ω
Input voltage	V_0	15 kV
Repetition rate	f	10 Hz

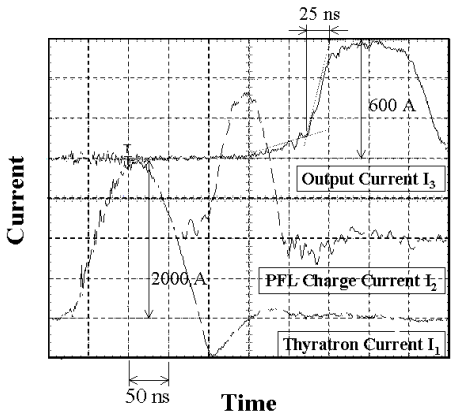

Figure 8. Measured current waveforms

4 DISCUSSION

In the following, the estimations of core-reset effect and the possibility of scale-up to actual output level in a synchrotron are discussed.

The magnetic switch inductance prior to core-saturation is estimated to be 9 μH, from the rise time of leakage current. On the other hand, using the previous equation (3), the inductance of the magnetic switch is calculated to be about 220 nH, because it is experientially known that the relative permeability of an amorphous core is about 2 at the state of core-saturation. The numerical estimation shows the actual relative permeability of the core is about 80 under the condition of core-unsaturation. The relative permeability of unsaturated core material is experimentally confirmed to be nearly 500 under the condition of optimized reset current[3]. The decrease of relative permeability is caused by lack of core-reset. It means that the maximum magnetic flux density in the core decreases.

Substituting equation (2) into equation (3), the inductance given by the equation (3) is described by the following equation:

$$L_{sat}=\mu_r^{sat}\mu_0\ln(r_{out}/r_{in})/(2\pi(r_{out}-r_{in})p_f)\int V\mathrm{d}t/\Delta B \qquad (4)$$

The equation directly shows that the magnetic flux density ΔB maximized by a sufficient reset current is the first priority in order to reduce the inductance.

Scale-up of the pulse circuit is possible by increasing the number of PFL multiple-divided pieces, and therefore by reducing the hold-off period. As shown in equation (2), increase of voltage is canceled by reducing the hold-off period without changing the core size.

In a full-scale model, optimization of core dimension is important to further reduce the inductance of the magnetic switch to keep an insulating distance between coils and cores.

5 CONCLUSIONS

Adaptability of a magnetic switch was investigated for the purpose of developing a fast kicker. A new pulse-circuit with a multiple-divided PFL and magnetic switches was designed.

The simulations and experiments showed that the present method enables a pulse-duration of charging to be reduced without degrading the shape of output current. An output current with a rise time of 25 ns, a peak of 600 A, and a flat top duration of 100 ns was obtained in the newly designed pulse-circuit.

The key point for a scale-up in the future is to optimize the number of multiple-divided PFL units, the core size, and the core-reset current.

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